24AA1026/24FC1026/24LC1026

1024-Kbit I²C Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges
24AA1026	1.7V-5.5V	400 kHz(1)	I
24FC1026	1.8V-5.5V	1 MHz(2)	I
24LC1026	2.5V-5.5V	400 kHz(3)	I, E

Note 1: 100 kHz for Vcc < 2.5V
2: 400 kHz for Vcc < 2.5V
3: 100 kHz for Vcc < 4.5V (E-temp.)

Features

- Low-Power CMOS Technology:
  - Read current: 450 µA, maximum
  - Standby current: 5 µA, maximum
- Two-Wire Serial Interface, I²C Compatible
- Cascadable Up to Four Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- 1 MHz Clock for FC Versions
- Page Write Time 3 ms, Typical
- Self-Timed Erase/Write Cycle
- 128-Byte Page Write Buffer
- Hardware Write-Protect
- High Reliability:
  - More than one million erase/write cycles
  - Data retention > 200 years
  - ESD protection > 4000V
- Factory Programming Available
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C

Packages

- 8-Lead PDIP, 8-Lead SOIC and 8-Lead SOIJ

Description

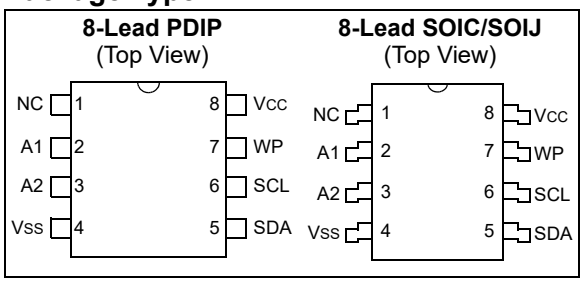
The Microchip Technology Inc. 24XX1026(1) is a 128-Kbit x 8 (1024-Kbit) Serial Electrically Erasable PROM (EEPROM), capable of operation across a broad voltage range (1.7V to 5.5V).

It has been developed for advanced, low-power applications such as personal communications or data acquisition. This device has both byte write and page write capability of up to 128 bytes of data.

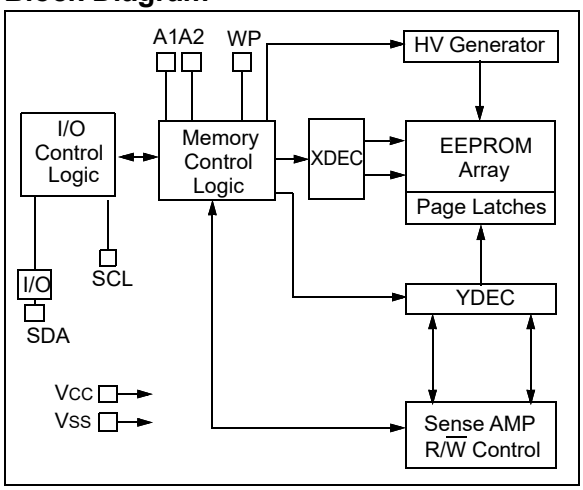
This device is capable of both random and sequential reads. Reads may be sequential within address boundaries 0000h to FFFFh and 10000h to 1FFFFh. Functional address lines allow up to four devices on the same data bus. This allows for up to 4 Mbits total system EEPROM memory.

Note 1: 24XX1026 is used in this document as a generic part number for the 24AA1026/24FC1026/24LC1026 devices.

Package Type



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC+1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied .....-40°C to +125°C

ESD protection on all pins .....≥4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** **Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C** **Extended (E): VCC = +2.5V to 5.5V TA = -40°C to +125°C**			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
D1	VIH	High-Level Input Voltage	0.7 VCC	—	V	
D2	VIL	Low-Level Input Voltage	—	0.3 VCC	V	VCC ≥ 2.5V
				0.2 VCC	V	VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins)	0.05 VCC	—	V	VCC ≥ 2.5V (**Note 1**)
D4	VOL	Low-Level Output Voltage	—	0.40	V	IOL = 3.0 mA @ VCC = 4.5V IOL = 2.1 mA @ VCC = 2.5V
D5	ILI	Input Leakage Current	—	±1	µA	VIN = VSS or VCC VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin Capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V (**Note 1**) TA = +25°C, FCLK = 1 MHz
D8	ICCREAD	Operating Current	—	450	µA	VCC = 5.5V, SCL = 400 kHz
	ICCWRITE		—	5	mA	VCC = 5.5V
D9	ICCS	Standby Current	—	5	µA	SCL = SDA = VCC = 5.5V A1 = A2 = WP = VSS

Note 1: This parameter is periodically sampled and is not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): VCC = +2.5V to 5.5V TA = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	100	kHz	1.7V ≤ VCC ≤ 2.5V
			—	100	kHz	2.5V ≤ VCC ≤ 4.5V, E-temp.
			—	400	kHz	2.5V ≤ VCC ≤ 5.5V
			—	400	kHz	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			—	1000	kHz	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
2	THIGH	Clock High Time	4000	—	ns	1.7V ≤ VCC ≤ 2.5V
			4000	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp.
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			500	—	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
3	TLOW	Clock Low Time	4700	—	ns	1.7V ≤ VCC ≤ 2.5V
			4700	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp.
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			500	—	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
4	TR	SDA and SCL Rise Time	—	1000	ns	1.7V ≤ VCC ≤ 2.5V (**Note 1**)
			—	1000	ns	2.5V ≤ VCC ≤ 4.5V, E-temp. (**Note 1**)
			—	300	ns	2.5V ≤ VCC ≤ 5.5V (**Note 1**)
			—	300	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**) (**Note 1**)
			—	300	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**) (**Note 1**)
5	TF	SDA and SCL Fall Time	—	300	ns	**24AA1026** and **24LC1026** (**Note 1**)
			—	100	ns	1.8V ≤ VCC ≤ 5.5V (**24FC1026**) (**Note 1**)
6	THD:STA	Start Condition Hold Time	4000	—	ns	1.7V ≤ VCC ≤ 2.5V
			4000	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp.
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			250	—	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
7	TSU:STA	Start Condition Setup Time	4700	—	ns	1.7V ≤ VCC ≤ 2.5V
			4700	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp.
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			250	—	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
8	THD:DAT	Data Input Hold Time	0	—	ns	**Note 2**

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but established by characterization.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): VCC = +2.5V to 5.5V TA = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
9	TSU:DAT	Data Input Setup Time	250	—	ns	1.7V ≤ VCC ≤ 2.5V
			250	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp.
			100	—	ns	2.5V ≤ VCC ≤ 5.5V
			100	—	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			100	—	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
10	TSU:STO	Stop Condition Setup Time	4000	—	ns	1.7V ≤ VCC ≤ 2.5V
			4000	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp.
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			250	—	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
11	TSU:WP	WP Setup Time	4000	—	ns	1.7V ≤ VCC ≤ 2.5V
			4000	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp.
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			600	—	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
12	THD:WP	WP Hold Time	4700	—	ns	1.7V ≤ VCC ≤ 2.5V
			4700	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp.
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
13	TAA	Output Valid from Clock	—	3500	ns	1.7V ≤ VCC ≤ 2.5V (**Note 2**)
			—	3500	ns	2.5V ≤ VCC ≤ 4.5V, E-temp. (**Note 2**)
			—	900	ns	2.5V ≤ VCC ≤ 5.5V (**Note 2**)
			—	900	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**) (**Note 2**)
			—	400	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**) (**Note 2**)
14	TBUF	Bus Free Time: bus time must be free before a new transmission can start	4700	—	ns	1.7V ≤ VCC ≤ 2.5V
			4700	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp.
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.8V ≤ VCC ≤ 2.5V (**24FC1026**)
			500	—	ns	2.5V ≤ VCC ≤ 5.5V (**24FC1026**)
15	TSP	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	24AA1026 and 24LC1026 (**Note 1** and **Note 3**)
16	TWC	Write Cycle Time (byte or page)	—	5	ms	—
17	—	Endurance	1,000,000	—	cycles	+25°C, 5.5V, Page Mode (**Note 4**)

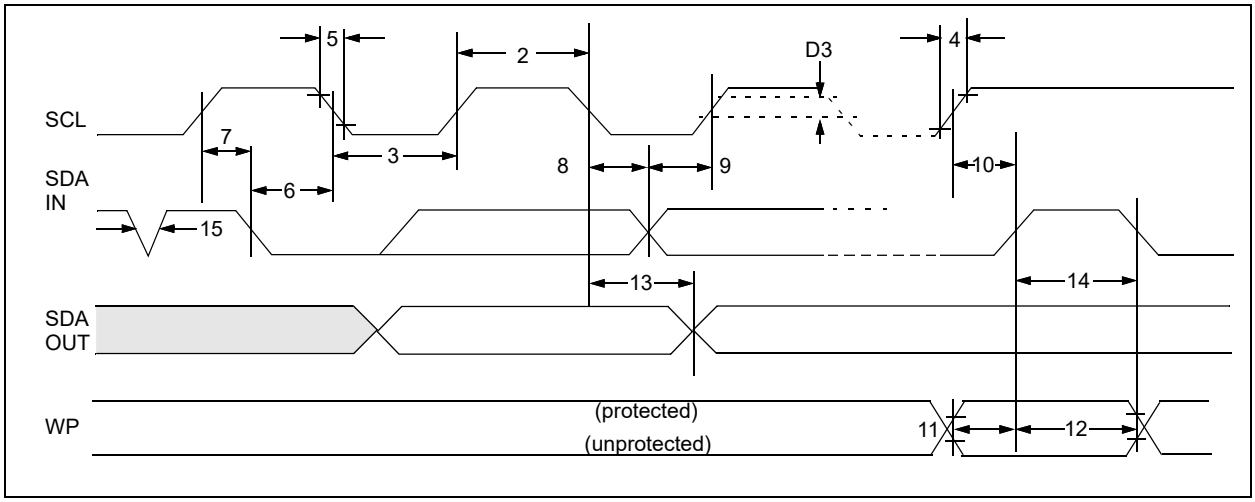
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but established by characterization.

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	SOIJ	Function
NC	1	1	1	Not Connected
A1	2	2	2	Chip Address Inputs
A2	3	3	3	Chip Address Inputs
VSS	4	4	4	Ground
SDA	5	5	5	Serial Data
SCL	6	6	6	Serial Clock
WP	7	7	7	Write-Protect Input
VCC	8	8	8	Power Supply

2.1 Chip Address Inputs (A1, A2)

The A1 and A2 inputs are used by the 24XX1026 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the client address. The chip is selected if the comparison is true.

Up to four devices may be connected to the same bus by using different Chip Select bit combinations. In most applications, the chip address inputs A1 and A2 are hardwired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

2.2 Serial Data (SDA)

SDA is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

2.4 Write-Protect (WP)

The WP pin must be connected to either VSS or VCC. If tied to VSS, write operations are enabled. If tied to VCC, write operations are inhibited, but read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24XX1026 supports a bidirectional Two-Wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, while a device receiving data is defined as a receiver. The bus must be controlled by a host device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX1026 works as a client. Both host and client can operate as a transmitter or receiver, but the host device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined as follows:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (see Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the host device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The host device must generate an extra clock pulse, which is associated with this Acknowledge bit.

Note:	The 24XX1026 does not generate any Acknowledge bits if an internal programming cycle is in progress. However, the control byte that is being polled must match the control byte used to initiate the write cycle.

The device that Acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge-related clock pulse. In addition, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24XX1026) will leave the data line high to enable the host to generate the Stop condition (see Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

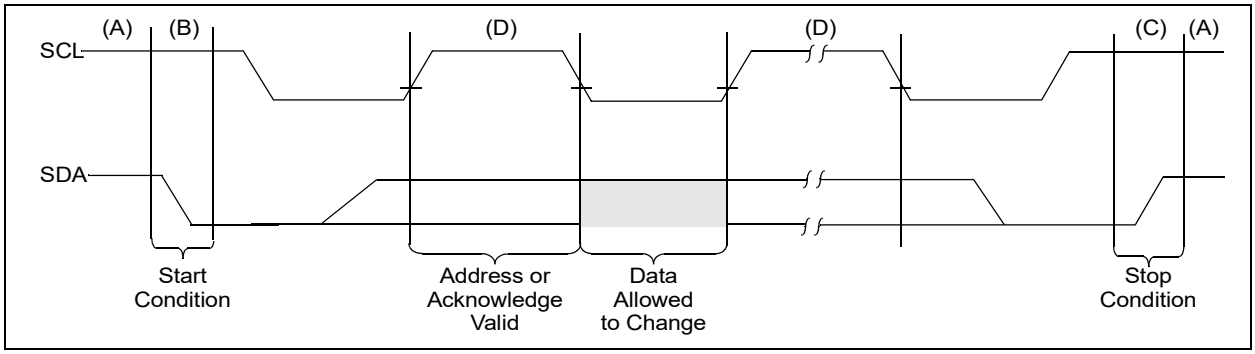
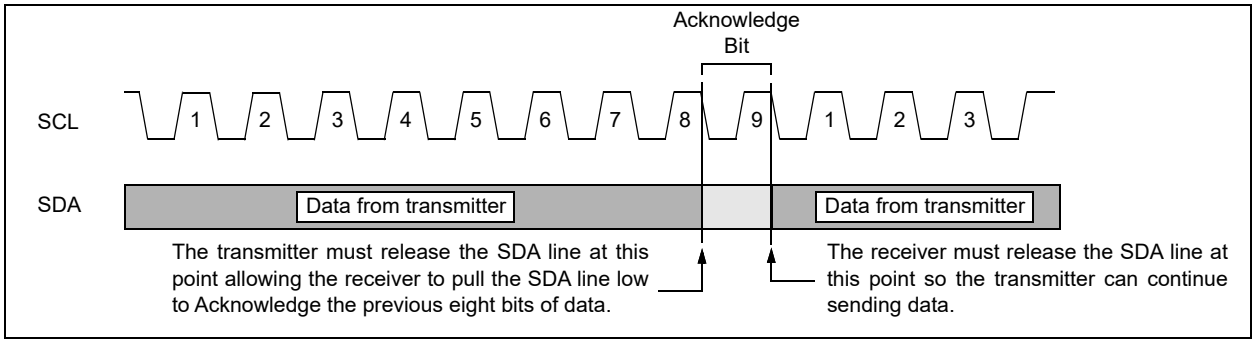


FIGURE 4-2: ACKNOWLEDGE TIMING



5.0 DEVICE ADDRESSING

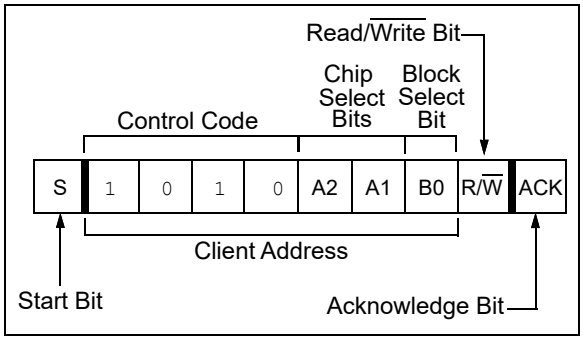
A control byte is the first byte received following the Start condition from the host device (Figure 5-1). The control byte consists of a 4-bit control code. For the 24XX1026, this is set as '1010' binary for read and write operations. The next two bits of the control byte are the Chip Select bits (A2, A1). The Chip Select bits allow the use of up to four 24XX1026 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2 and A1 pins for the device to respond. These bits are, in effect, the two Most Significant bits (MSb) of the word address. The next bit of the control byte is the block select bit (B0). This bit acts as the A16 address bit for accessing the entire array.

The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). The upper address bits are transferred first, followed by the Least Significant bits (LSb).

Following the Start condition, the 24XX1026 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving a '1010' code and appropriate device select bits, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24XX1026 will select a read or write operation.

This device has an internal addressing boundary limitation that is divided into two segments of 512 Kbits. Block select bit 'B0' is used to control access to each segment.

FIGURE 5-1: CONTROL BYTE FORMAT



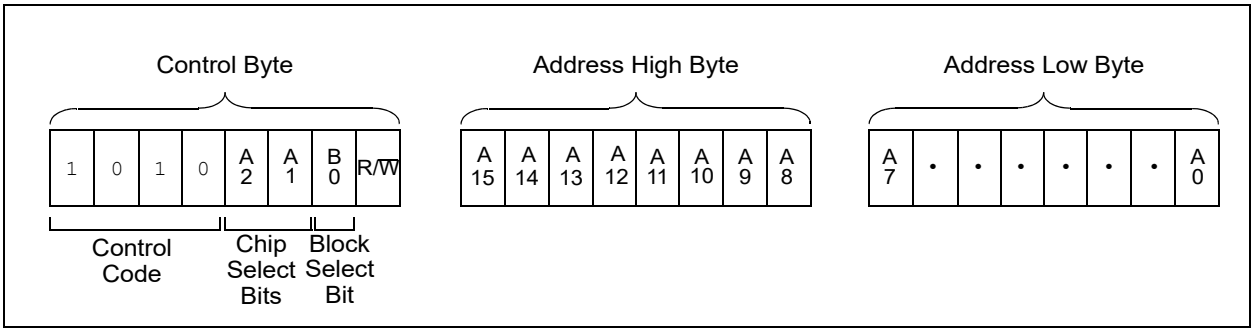
5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2 and A1 can be used to expand the contiguous address space for up to 4 Mbit by adding up to four 24XX1026 devices on the same bus. In this case, software can use A1 of the **control byte** as address bit A17 and A2 as address bit A18. It is not possible to sequentially read across device boundaries.

Each device has internal addressing boundary limitations. This divides each part into two segments of 512 Kbits. The block select bit 'B0' controls access to each "half".

Sequential read operations are limited to 512K blocks. To read through four devices on the same bus, eight random Read commands must be given.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start condition from the host, the control code (4 bits), the Chip Select (2 bits), the block select (1 bit) and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the host transmitter. This indicates to the addressed client receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the high-order byte of the word address and will be written into the Address Pointer of the 24XX1026.

The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX1026, the host device will transmit the data word to be written into the addressed memory location. The 24XX1026 Acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and, during this time, the 24XX1026 will not generate Acknowledge signals as long as the control byte being polled matches the control byte that was used to initiate the write (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will Acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte Write command, the internal address counter will point to the address location following the one that was just written.

Note:	When doing a write of less than 128 bytes, the data in the rest of the page is refreshed along with the data bytes being written. This will force the entire page to endure a write cycle. For this reason, endurance is specified per page.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX1026 in the same way as in a byte write. Instead of generating a Stop condition, however, the host transmits up to 127 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the host has transmitted a Stop condition. Upon receipt of each word, the seven lower Address Pointer bits are internally incremented by one.

If the host should transmit more than 128 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will Acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (00000-1FFFF) when the pin is tied to VCC. If tied to VSS the write protection is disabled. The WP pin is sampled at the Stop bit for every Write command (Figure 1-1). Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

FIGURE 6-1: BYTE WRITE

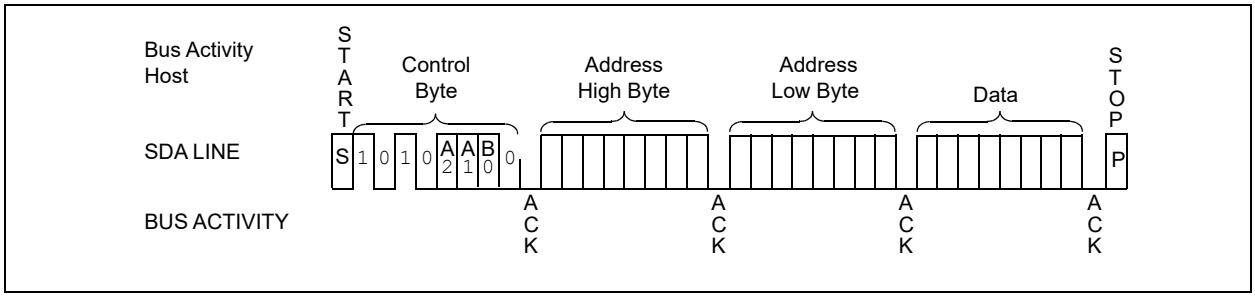
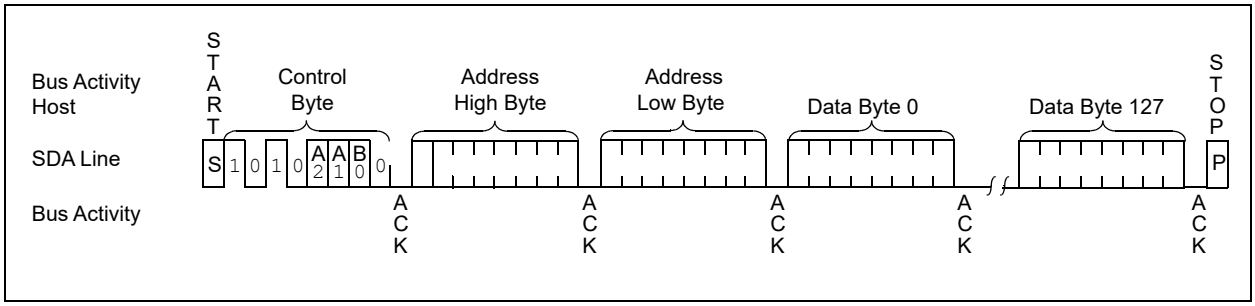


FIGURE 6-2: PAGE WRITE

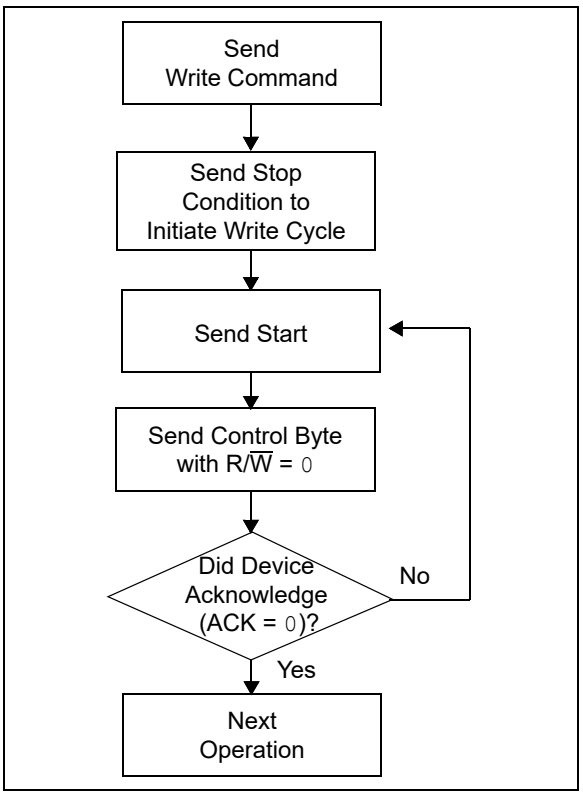


7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, acknowledge polling can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput.) Once the Stop condition for a Write command has been issued from the host, the device initiates the internally-timed write cycle, with ACK polling being initiated immediately. This involves the host sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, no ACK will be returned. If no ACK is returned, the Start bit and control byte must be resent. If the cycle is complete, the device will return the ACK and the host can then proceed with the next Read or Write command. See Figure 7-1 for a flow diagram of this operation.

Note:	Care must be taken when polling the 24XX1026. The control byte that was used to initiate the write needs to match the control byte used for polling.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

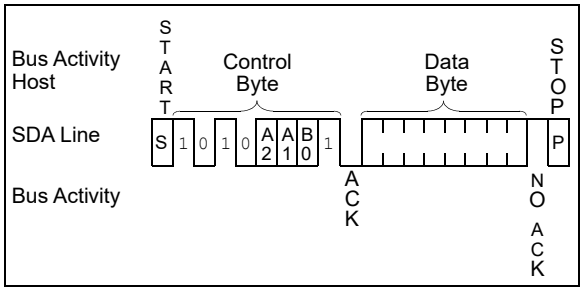
Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX1026 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the 24XX1026 issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24XX1026 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is accomplished by sending the word address to the 24XX1026 as part of a write operation (R/$\overline{W}$ bit set to '0'). After the word address is sent, the host generates a Start condition following the Acknowledge.

This terminates the write operation, but not before the internal Address Pointer is set. Then, the host issues the control byte again, but with the R/$\overline{W}$ bit set to '1'. The 24XX1026 will then issue an Acknowledge and transmit the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition, which causes the 24XX1026 to discontinue transmission (Figure 8-2). After a random Read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as random reads, except that after the 24XX1026 transmits the first data byte, the host issues an Acknowledge as opposed to the Stop condition used in a random read. This Acknowledge directs the 24XX1026 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte being transmitted to the host, the host will NOT generate an Acknowledge, but will generate a Stop condition. To provide sequential reads, the 24XX1026 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows half the memory contents to be serially read during one operation. Sequential read address boundaries are 00000h to 0FFFFh and 10000h to 1FFFFh. The internal Address Pointer will automatically roll over from address 0FFFFh to address 00000h if the host Acknowledges the byte received from the array address, 0FFFFh. The internal address counter will automatically roll over from address 1FFFFh to address 10000h if the host Acknowledges the byte received from the array address 1FFFFh.

FIGURE 8-2: RANDOM READ

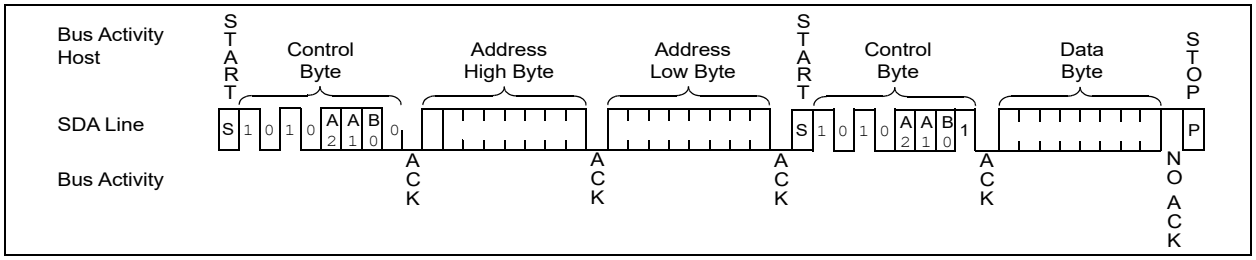
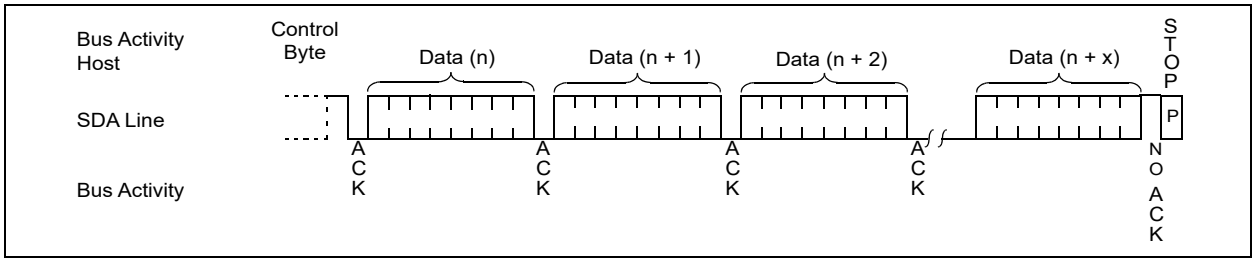


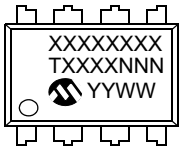
FIGURE 8-3: SEQUENTIAL READ



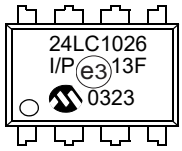
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

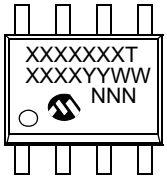
8-Lead PDIP (300 mil)



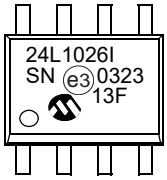
Example



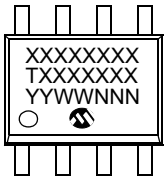
8-Lead SOIC (3.90 mm)



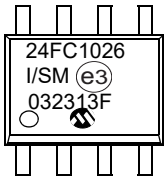
Example



8-Lead SOIJ (5.28 mm)



Example



Part Number	1st Line Marking Codes		
	PDIP	SOIC	SOIJ
24AA1026	24AA1026	24A1026I	24AA1026
24FC1026	24FC1026	24F1026I	24FC1026
24LC1026	24LC1026	24L1026I	24LC1026

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	RoHS-compliant JEDEC® designator for Matte Tin (Sn)

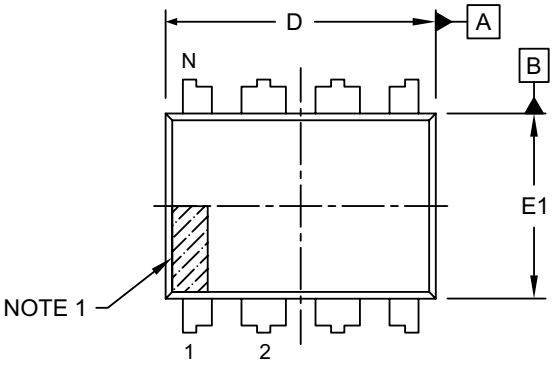
Note: Standard device marking consists of Microchip part number, year code, week code and traceability code (facility code, mask rev#, and assembly code). For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

Note: For very small packages with no room for the RoHS-compliant JEDEC® designator (e3) the marking will only appear on the outer carton or reel label.

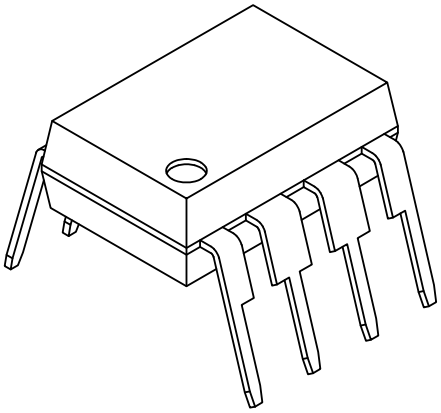
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

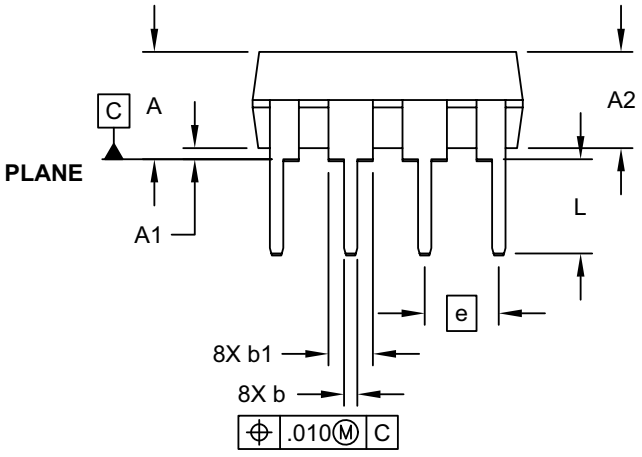
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

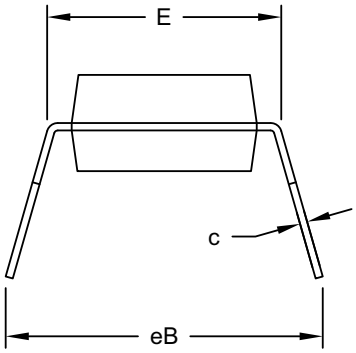


TOP VIEW





SIDE VIEW

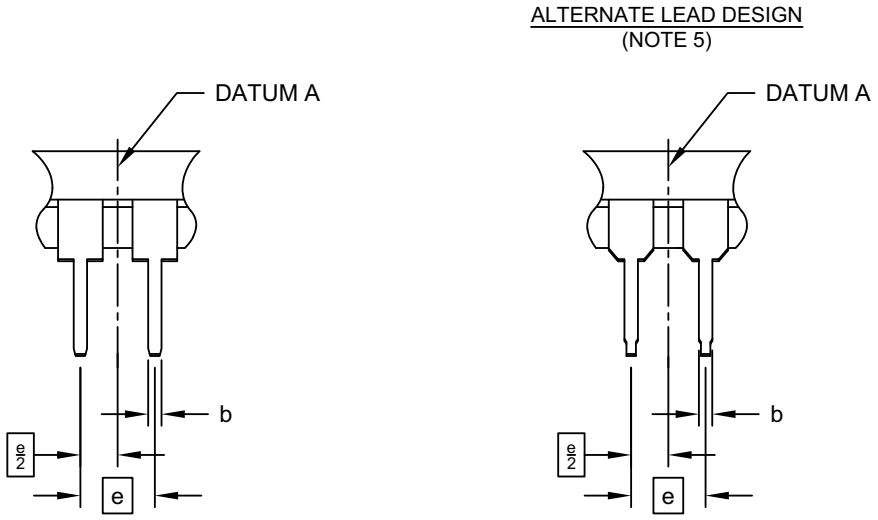


END VIEW

Microchip Technology Drawing No. C04-018-P Rev F Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

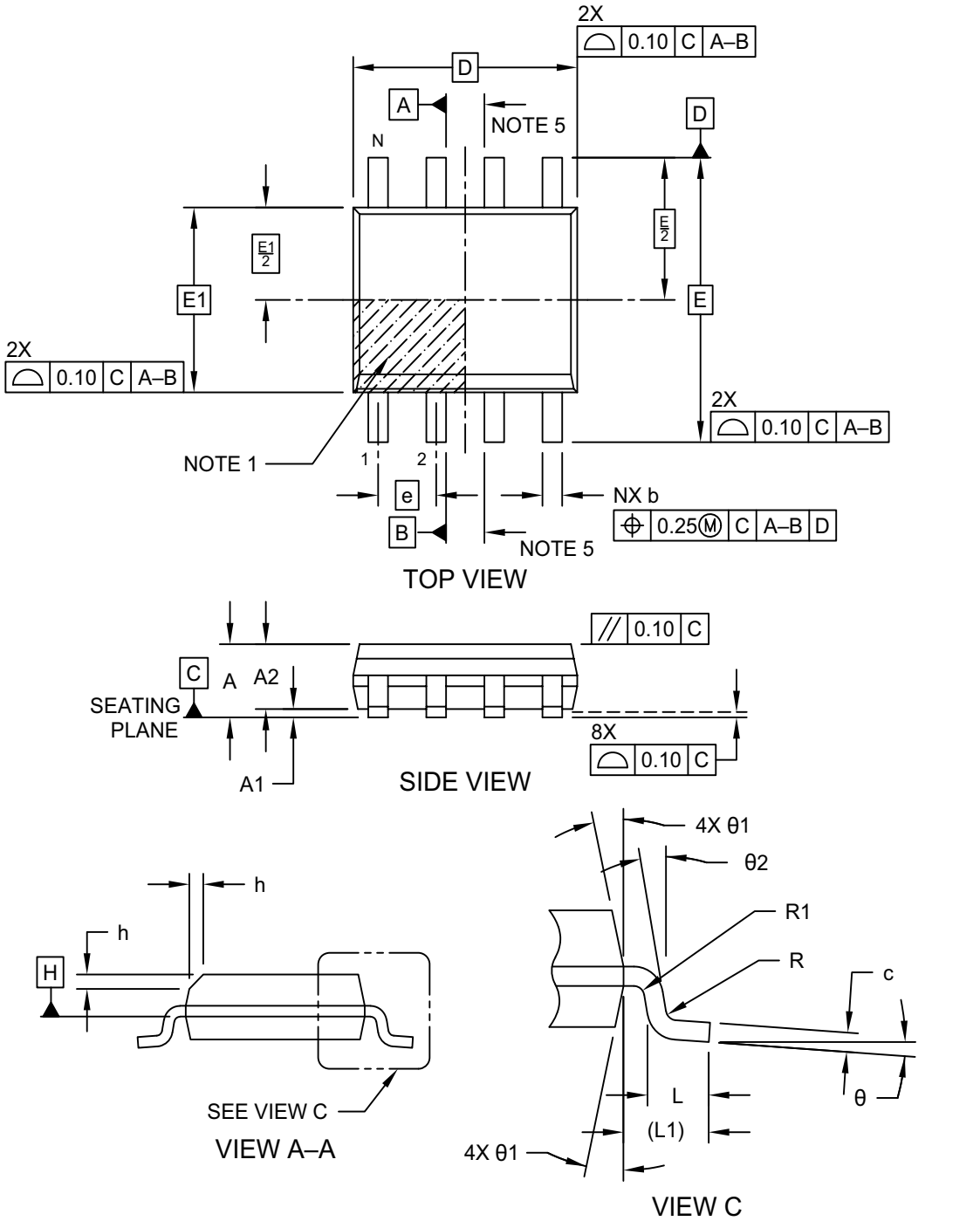
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

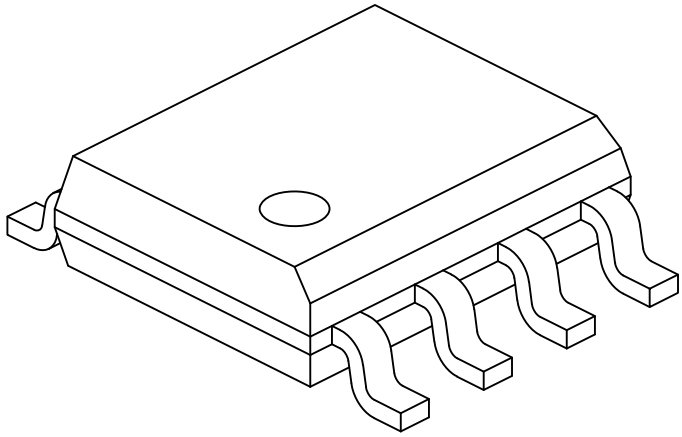
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

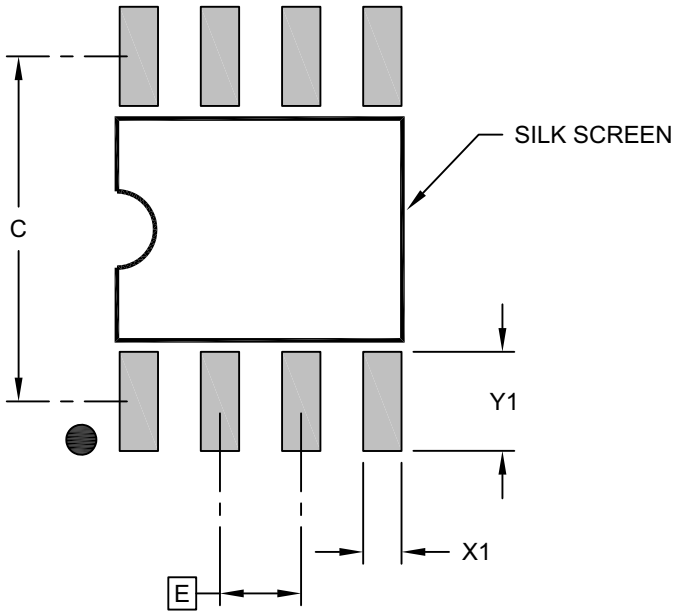
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

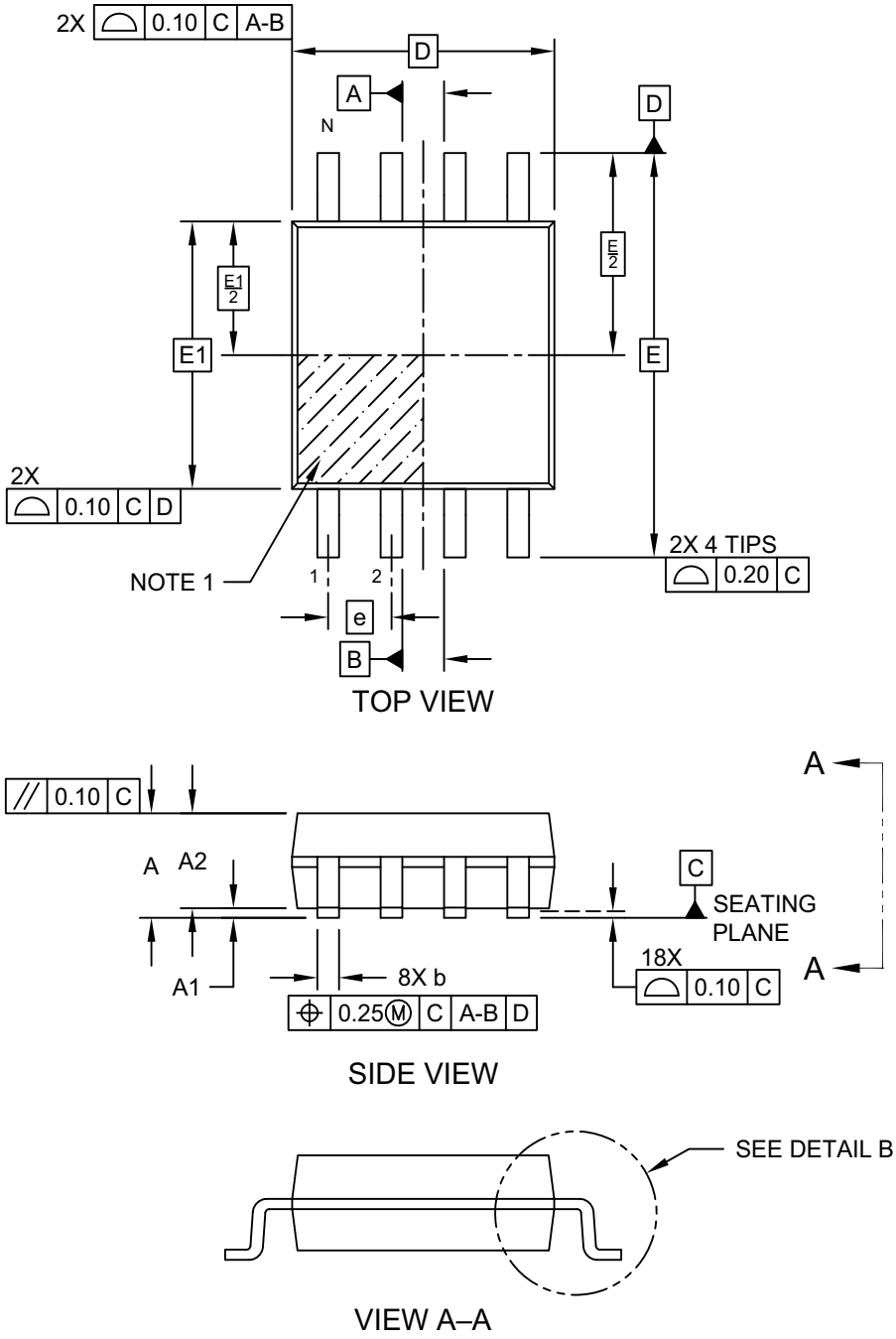
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev K

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

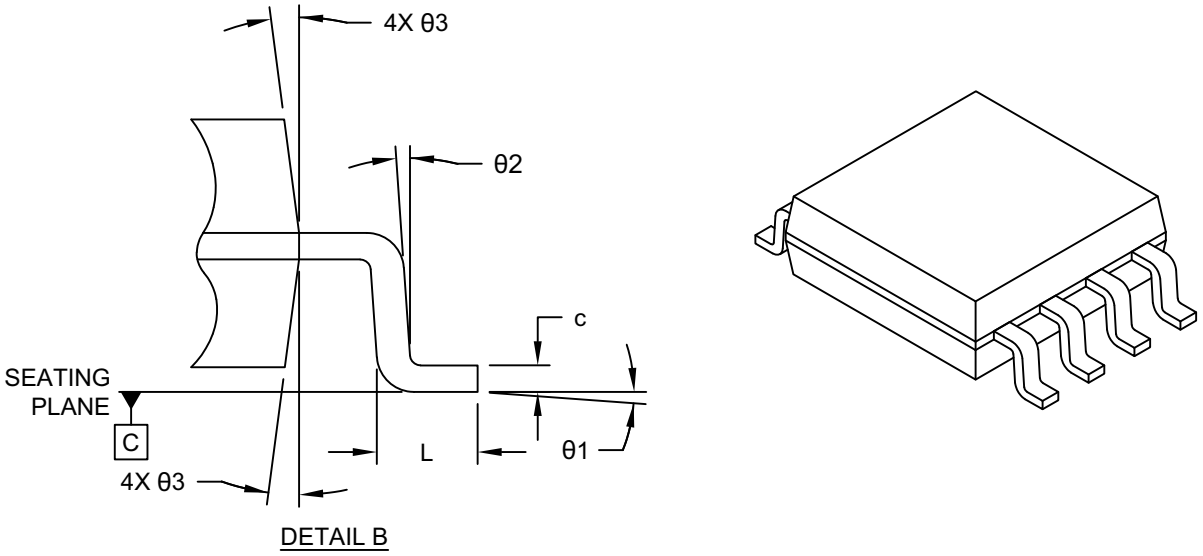
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-056 Rev E Sheet 1 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.77	–	2.03
Standoff §	A1	0.05	–	0.25
Molded Package Thickness	A2	1.75	–	1.98
Overall Length	D		5.26 BSC	
Overall Width	E		7.94 BSC	
Molded Package Width	E1		5.25 BSC	
Terminal Width	b	0.36	–	0.51
Terminal Thickness	c	0.15	–	0.25
Terminal Length	L	0.51	–	0.76
Foot Angle	θ1	0°	–	8°
Lead Angle	θ2	0°	–	–
Mold Draft Angle	θ3	–	–	15°

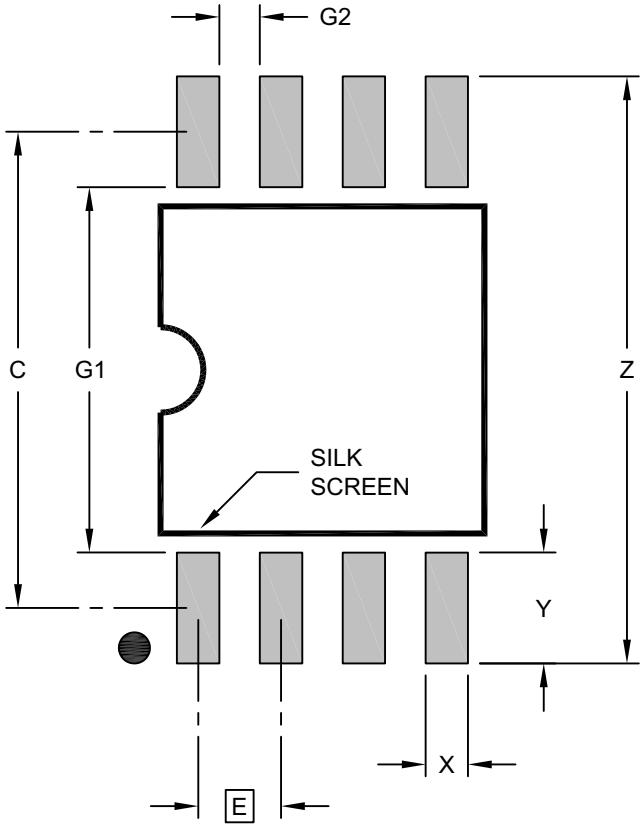
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. SOIJ – JEITA/EIAJ Standard, Formerly called SOIC
3. § – Significant Characteristic
4. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
5. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-056 Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Overall Width	Z			9.00
Contact Pad Spacing	C		7.30	
Contact Pad Width (X8)	X			0.65
Contact Pad Length (X8)	Y			1.70
Contact Pad to Contact Pad (X4)	G1	5.60		
Contact Pad to Contact Pad (X6)	G2	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2056 Rev E

APPENDIX A: REVISION HISTORY

Revision F (05/2023)

Replaced “master” and “slave” terminology with “host” and “client”, respectively; replaced automotive temperature with extended temperature throughout the document.

Revision E (11/2015)

Removed TSSOP package.

Revision D (07/2013)

Added TSSOP package.

Revision C (04/2012)

Revised document title (removed CMOS); Revised Table 1-1, Param D9; Revised Section 5.1.

Revision B (5/2011)

Added Automotive Temperature.

Revision A (01/2011)

Original release of this document.

NOTES:

THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip website at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X] (1)	-X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	24AA1026	= 1024-Kbit, 1.7V I^2C CMOS Serial EEPROM
	24FC1026	= 1024-Kbit, 1.8V I^2C CMOS Serial EEPROM
	24LC1026	= 1024-Kbit, 2.5V I^2C CMOS Serial EEPROM
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel (1)
Temperature Range:	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package:	P	= Plastic Dual In-Line - 300 mil Body, 8-lead (PDIP)
	SN	= Plastic Small Outline - Narrow 3.90 mm Body, 8-lead (SOIC)
	SM	= Plastic Small Outline - Medium 5.28 mm Body, 8-lead (SOIJ)

Examples:

a) 24AA1026-I/P: 1.7V Serial EEPROM, Industrial Temperature, PDIP package.

b) 24AA1026-I/SN: 1.7V Serial EEPROM, Industrial Temperature, SOIC package

c) 24AA1026T-I/SN: 1.7V Serial EEPROM, Industrial Temperature, Tape and Reel, SOIC package.

d) 24AA1026T-I/SM: 1.7V Serial EEPROM, Industrial Temperature, Tape and Reel, SOIJ package.

e) 24FC1026-I/SN: 1.8V Serial EEPROM, Industrial Temperature, SOIC package.

f) 24FC1026T-I/SN: 1.8V Serial EEPROM, Industrial Temperature, Tape and Reel, SOIC package

g) 24LC1026-I/P: 2.5V Serial EEPROM, Industrial Temperature, PDIP package.

h) 24LC1026T-I/SM: 2.5V Serial EEPROM, Industrial Temperature, Tape and Reel, SOIJ package.

i) 24LC1026-E/SM: 2.5V Serial EEPROM, Extended Temperature, SOIJ package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

ISBN: 978-1-6683-2385-4

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820