24AA64F/24LC64F/24FC64F

64-Kbit I²C Serial EEPROM with Quarter-Array Write-Protect

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges	Available Packages
24AA64F	1.7V-5.5V	400 kHz(1)	I	MS, P, SN, ST, MN, OT
24LC64F	2.5V-5.5V	400 kHz	I, E	MS, P, SN, ST, MN, OT
24FC64F	1.7V-5.5V	1 MHz(2)	I	MS, P, SN, ST, MN, OT

Note 1: 100 kHz for Vcc <2.5V.
2: 400 kHz for Vcc <2.5V.

Features

- Single-Supply with Operation Down to 1.7V for 24AA64F/24FC64F Devices, 2.5V for 24LC64F Devices
- Low-Power CMOS Technology:
  - Read current 400 μA, max.
  - Standby current 1 μA, max. (I-temp)
- Two-Wire Serial Interface, I²C Compatible
- Packages with Three Address Pins are Cascadable up to Eight Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- 1 MHz Clock for FC Versions
- Page Write Time 5 ms, Maximum
- Self-timed Erase/Write Cycle
- 32-Byte Page Write Buffer
- Hardware Write-Protect for 1/4 Array (1800h-1FFFh)
- High Reliability:
  - More than one million erase/write cycles
  - Data retention > 200 years
  - ESD protection > 4,000V
- Factory Programming Available
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C

Packages

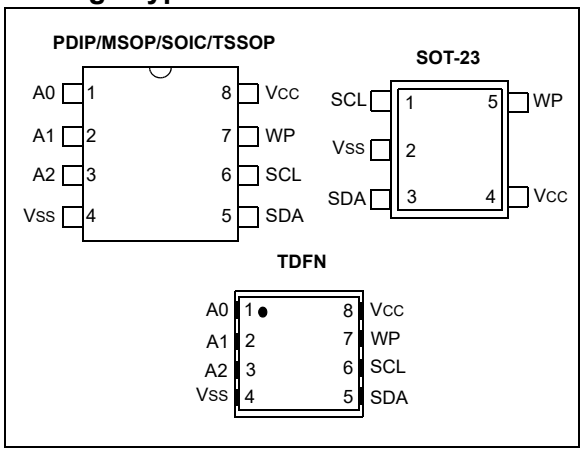
- 8-Lead MSOP, 8-Lead PDIP, 8-Lead SOIC, 8-Lead TDFN, 8-Lead TSSOP and 5-Lead SOT-23

Description

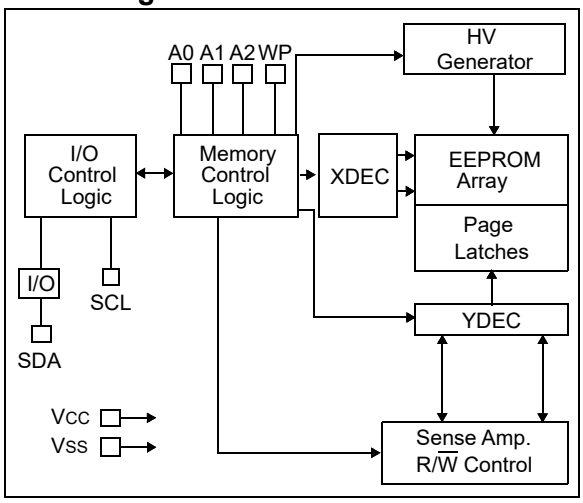
The Microchip Technology Inc. 24AA64F/24LC64F/24FC64F (24XX64F(1)) is a 64-Kbit Electrically Erasable PROM. The device is organized as a single block of 8K x 8-bit memory with a Two-Wire serial interface. Low-voltage design permits operation down to 1.7V, with standby and read currents of only 1 μA and 400 μA, respectively. It has been developed for advanced, low-power applications such as personal communications or data acquisition. The 24XX64F also has a page write capability of up to 32 bytes of data. Functional address lines allow up to eight devices on the same bus, for up to 512 Kbits address space.

Note 1: 24XX64F is used in this document as a generic part number for the 24AA64F/24LC64F/24FC64F devices

Package Types



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.3V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Industrial (I): TA = -40°C to +85°C, VCC = +1.7V to +5.5V Extended (E): TA = -40°C to +125°C, VCC = +2.5V to +5.5V**			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
D1	VIH	High-level input voltage	0.7 VCC	—	V	—
D2	VIL	Low-level input voltage	—	0.3 VCC	V	VCC ≥ 2.5V
			—	0.2 VCC	V	VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 VCC	—	V	VCC ≥ 2.5V **(Note 1)**
D4	VOL	Low-level output voltage	—	0.40	V	IOL = 3.0 mA @ VCC = 4.5V IOL = 2.1 mA @ VCC = 2.5V
D5	ILI	Input leakage current	—	±1	µA	VIN = VSS or VCC
D6	ILO	Output leakage current	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V **(Note 1)** TA = 25°C, FCLK = 1 MHz
D8	ICC Write	Operating current	—	3	mA	VCC = 5.5V, SCL = 400 kHz
D9	ICC Read		—	400	µA	
D10	ICCS	Standby current	—	1	µA	Industrial SDA = SCL = VCC A0, A1, A2, WP = VSS
			—	5	µA	Extended SDA = SCL = VCC A0, A1, A2, WP = VSS

Note 1: This parameter is periodically sampled and is not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock frequency	—	100	kHz	1.7V ≤ VCC < 2.5V
			—	400	kHz	2.5V ≤ VCC ≤ 5.5V
			—	400	kHz	1.7V ≤ VCC < 2.5V **(24FC64F)**
			—	1000	kHz	2.5V ≤ VCC ≤ 5.5V **(24FC64F)**
2	THIGH	Clock high time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC < 2.5V **(24FC64F)**
			500	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC64F)**
3	TLOW	Clock low time	4700	—	ns	1.7V ≤ VCC < 2.5V
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.7V ≤ VCC < 2.5V **(24FC64F)**
			500	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC64F)**
4	TR	SDA and SCL rise time **(Note 1)**	—	1000	ns	1.7V ≤ VCC < 2.5V
			—	300	ns	2.5V ≤ VCC ≤ 5.5V
			—	300	ns	1.7V ≤ VCC ≤ 5.5V **(24FC64F)**
5	TF	SDA and SCL fall time **(Note 1)**	—	300	ns	All except 24FC64F
			—	100	ns	1.7V ≤ VCC ≤ 5.5V **(24FC64F)**
6	THD:STA	Start condition hold time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC < 2.5V **(24FC64F)**
			250	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC64F)**
7	TSU:STA	Start condition setup time	4700	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC < 2.5V **(24FC64F)**
			250	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC64F)**
8	THD:DAT	Data input hold time	0	—	ns	**(Note 2)**
9	TSU:DAT	Data input setup time	250	—	ns	1.7V ≤ VCC < 2.5V
			100	—	ns	2.5V ≤ VCC ≤ 5.5V
			100	—	ns	1.7V ≤ VCC ≤ 5.5V**(24FC64F)**
10	TSU:STO	Stop condition setup time	4000	—	ns	1.7 V ≤ VCC < 2.5V
			600	—	ns	2.5 V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC < 2.5V **(24FC64F)**
			250	—	ns	2.5 V ≤ VCC ≤ 5.5V **(24FC64F)**

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but is ensured by characterization.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
11	TSU:WP	WP setup time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC ≤ 5.5V **(24FC64F)**
12	THD:WP	WP hold time	4700	—	ns	1.7V ≤ VCC < 2.5V
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.7V ≤ VCC ≤ 5.5V **(24FC64F)**
13	TAA	Output valid from clock **(Note 2)**	—	3500	ns	1.7V ≤ VCC < 2.5V
			—	900	ns	2.5V ≤ VCC ≤ 5.5V
			—	900	ns	1.7V ≤ VCC < 2.5V **(24FC64F)**
			—	400	ns	2.5V ≤ VCC ≤ 5.5V **(24FC64F)**
14	TBUF	Bus free time: Time the bus must be free before a new transmission can start	4700	—	ns	1.7V ≤ VCC < 2.5V
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.7V ≤ VCC < 2.5V **(24FC64F)**
			500	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC64F)**
15	TOF	Output fall time from VIH minimum to VIL maximum CB ≤ 100 pF	10 + 0.1CB	250	ns	All except, 24FC64F **(Note 1)**
				250	ns	24FC64F **(Note 1)**
16	TSP	Input filter spike suppression (SDA and SCL pins)	—	50	ns	All except, 24FC64F **(Notes 1 and 3)**
17	TWC	Write cycle time (byte or page)	—	5	ms	—
18	—	Endurance	1,000,000	—	cycles	25°C, VCC = 5.5V, Page Mode **(Note 4)**

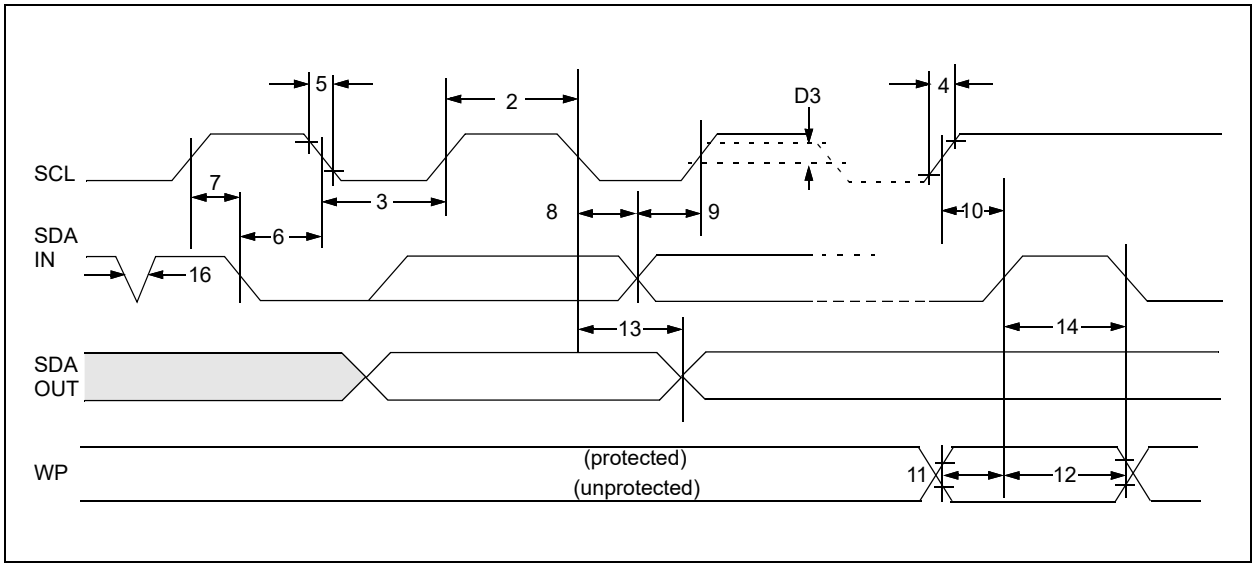
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but is ensured by characterization.

FIGURE 1-3: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-Lead MSOP	8-Lead PDIP	8-Lead SOIC	8-Lead TDFN(1)	8-Lead TSSOP	5-Lead SOT-23	Description
A0	1	1	1	1	1	—	Chip Address Input
A1	2	2	2	2	2	—	Chip Address Input
A2	3	3	3	3	3	—	Chip Address Input
VSS	4	4	4	4	4	2	Ground
SDA	5	5	5	5	5	3	Serial Address/Data I/O
SCL	6	6	6	6	6	1	Serial Clock
WP	7	7	7	7	7	5	Write-Protect Input
VCC	8	8	8	8	8	4	Power Supply

Note 1: Exposed pad on the TDFN package can be connected to VSS or left floating.

2.1 Chip Address Inputs (A0, A1, A2)

The A0, A1 and A2 inputs are used by the 24XX64F for multiple device operation. The levels on these inputs are compared with the corresponding bits in the client address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VCC or VSS.

In most applications, the chip address inputs A0, A1 and A2 are hardwired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed. Address pins are not available in the SOT-23 package.

2.2 Serial Data (SDA)

SDA is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

2.4 Write-Protect (WP)

This pin must be connected to either VSS or VCC. If tied to VSS, write operations are enabled. If tied to VCC, write operations are inhibited for upper 1/4 of the array (1800h-1FFFh), but read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24XX64F supports a bidirectional, Two-Wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a host device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX64F works as client. Both host and client can operate as transmitter or receiver, but the host device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined as follows:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the host device and is theoretically unlimited, although only the last thirty two will be stored when doing a write operation. When an overwrite does occur, it will replace data in a First-In First-Out (FIFO) fashion.

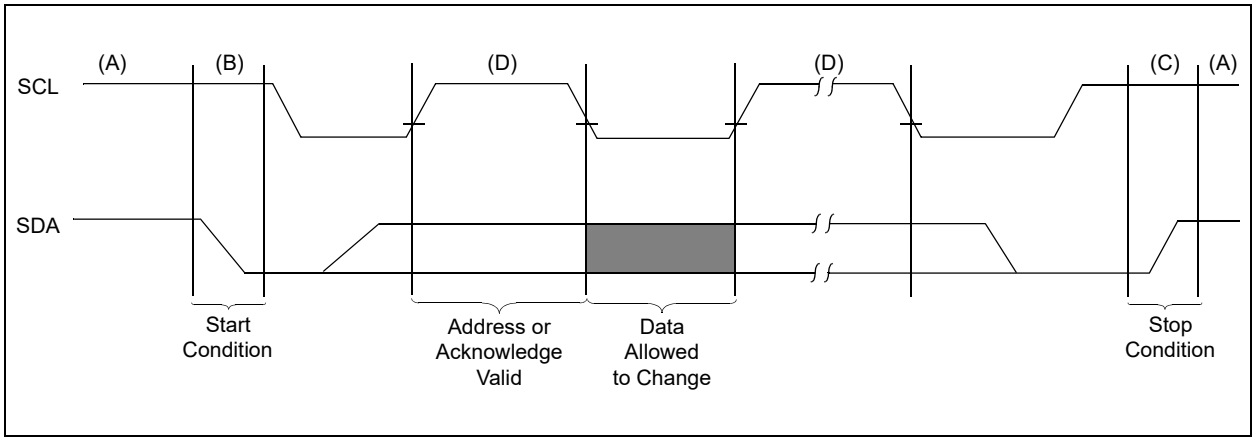
4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. The host device must generate an extra clock pulse, which is associated with this Acknowledge bit.

Note:	The 24XX64F does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. In addition, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24XX64F) will leave the data line high to enable the host to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



5.0 DEVICE ADDRESSING

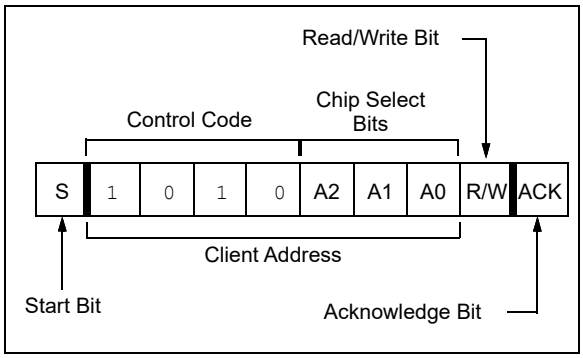
A control byte is the first byte received following the Start condition from the host device (Figure 5-1). The control byte consists of a four-bit control code. For the 24XX64F, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24XX64F devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are, in effect, the three Most Significant bits of the word address.

For the SOT-23 package, the address pins are not available. During device addressing, the A2, A1 and A0 Chip Select bits (Figure 5-2) should be set to '0'.

The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because only A12...A0 are used, the upper-three address bits are "don't care" bits. The upper-address bits are transferred first, followed by the Less Significant bits.

Following the Start condition, the 24XX64F monitors the SDA bus, checking the device-type identifier being transmitted. Upon receiving a '1010' code and appropriate device-select bits, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24XX64F will select a read or write operation.

FIGURE 5-1: CONTROL BYTE FORMAT

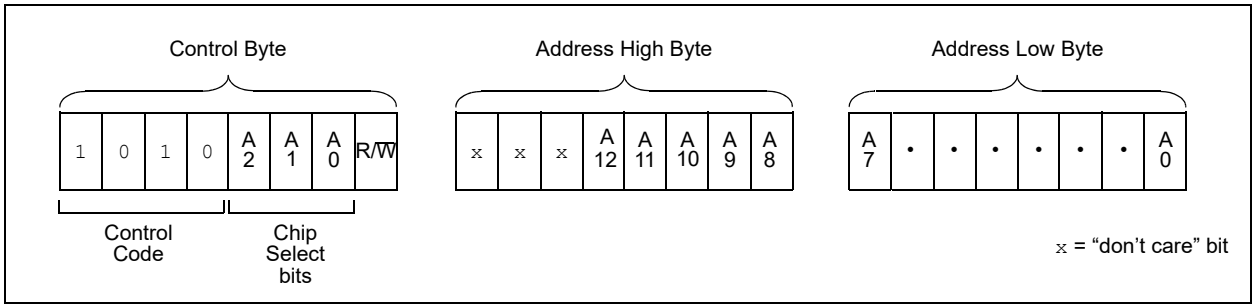


5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 512 Kbits by adding up to eight 24XX64F devices on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14 and A2 as address bit A15. It is not possible to sequentially read across device boundaries.

The SOT-23 package does not support multiple device addressing on the same bus.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start condition from the host, the control code (4 bits), the Chip Select (3 bits) and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the host transmitter. This indicates to the addressed client receiver that the address high byte will follow once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the high-order byte of the word address and will be written into the Address Pointer of the 24XX64F.

The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX64F, the host device will transmit the data word to be written into the addressed memory location. The 24XX64F acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and, during this time, the 24XX64F will not generate Acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte Write command, the internal address counter will point to the address location following the one that was just written.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX64F in the same way as in a byte write. Instead of generating a Stop condition, however, the host transmits up to 31 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory once the host has transmitted a Stop condition. Upon receipt of each word, the five lower Address Pointer bits are internally incremented by one.

If the host should transmit more than 32 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

6.3 Write Protection

The WP pin allows the user to write-protect 1/4 of the array (1800h-1FFFh) when the pin is tied to VCC. If tied to VSS, the write protection is disabled. The WP pin is sampled at the Stop bit for every Write command (Figure 4-1). Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

FIGURE 6-1: BYTE WRITE

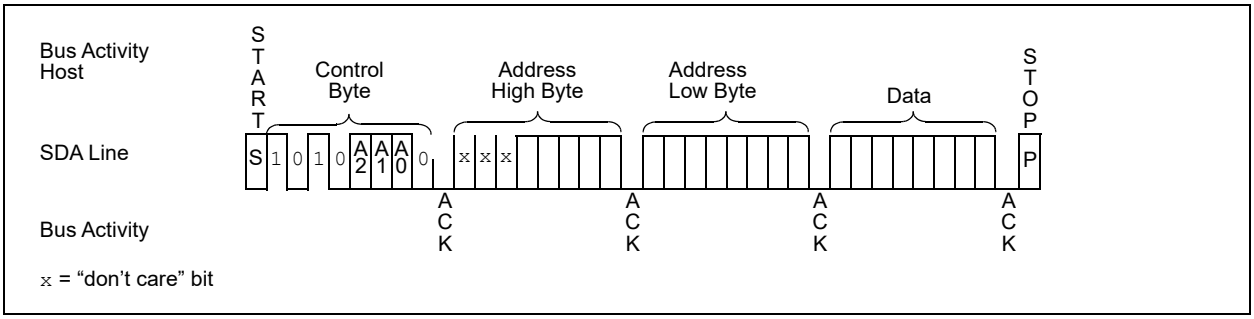
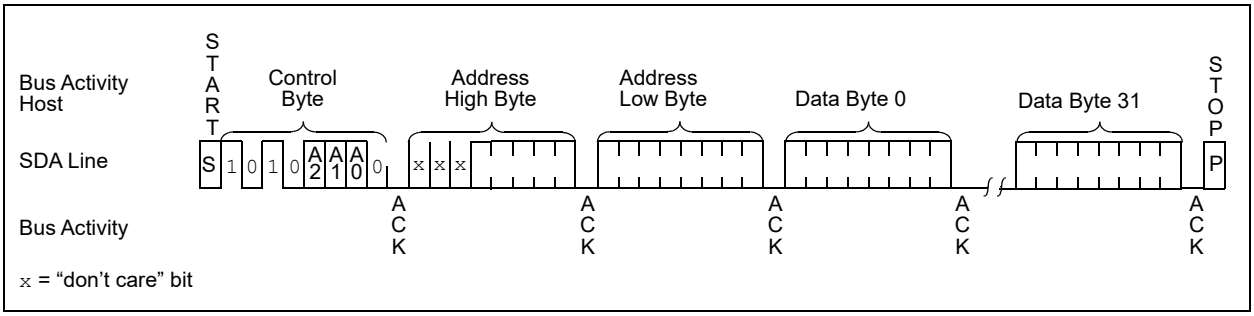


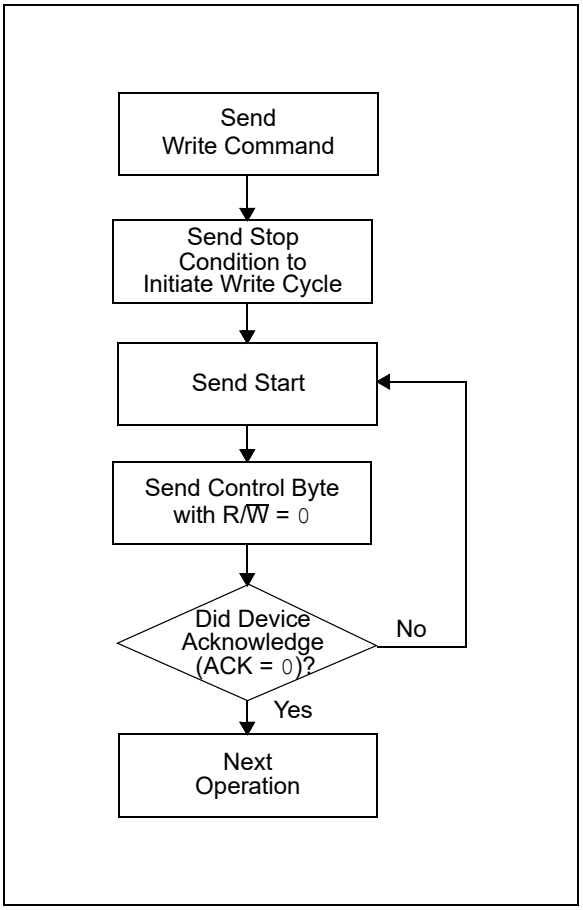
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, acknowledge polling can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the host, the device initiates the internally-timed write cycle and ACK polling can then be initiated immediately. This involves the host sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, the device will return the ACK and the host can then proceed with the next Read or Write command. See Figure 7-1 for a flow diagram of this operation.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX64F contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address 'n' (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the 24XX64F issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24XX64F discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24XX64F as part of a write operation (R/$\overline{W}$ bit set to '0'). Once the word address is sent, the host generates a Start condition following the Acknowledge.

This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again, but with the R/$\overline{W}$ bit set to '1'. The 24XX64F will then issue an Acknowledge and transmit the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition, which causes the 24XX64F to discontinue transmission (Figure 8-2). After a random Read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as random reads, except that once the 24XX64F transmits the first data byte, the host issues an acknowledge as opposed to the Stop condition used in a random read. This Acknowledge directs the 24XX64F to transmit the next sequentially-addressed 8-bit word (Figure 8-3). Following the final byte being transmitted to the host, the host will NOT generate an acknowledge, but will generate a Stop condition. To provide sequential reads, the 24XX64F contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address 1FFF to address 0000 if the host acknowledges the byte received from the array address 1FFF.

FIGURE 8-1: CURRENT ADDRESS READ

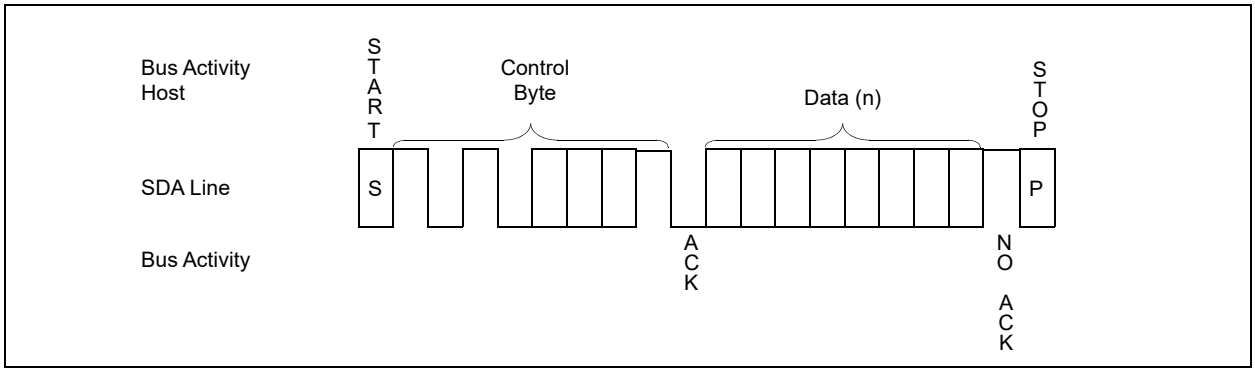


FIGURE 8-2: RANDOM READ

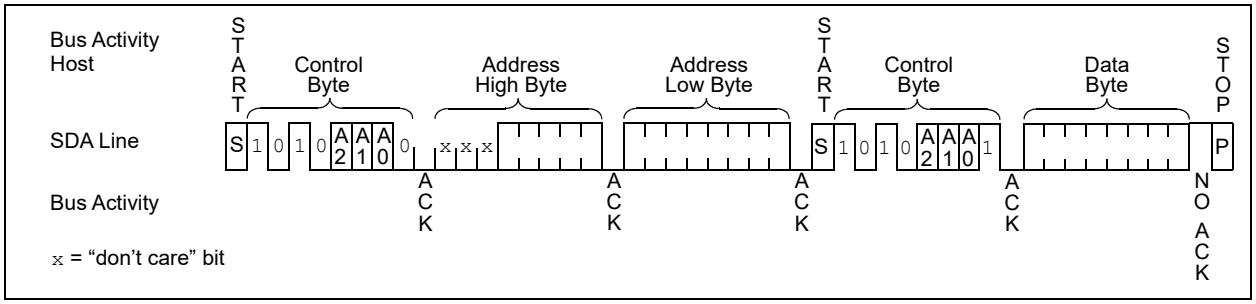
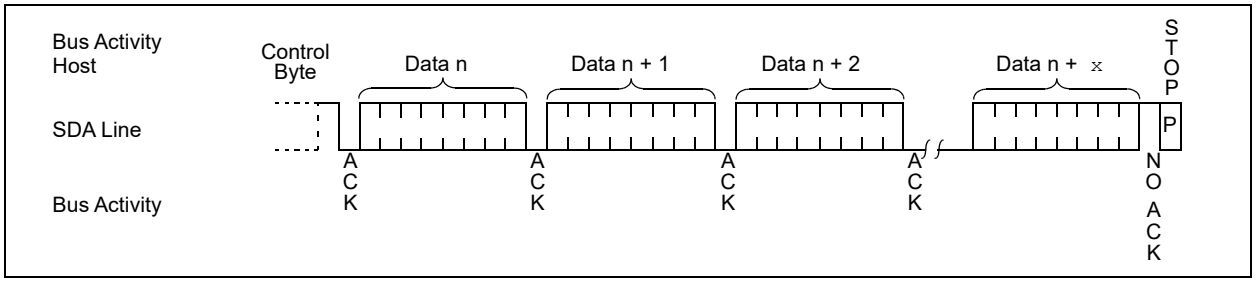


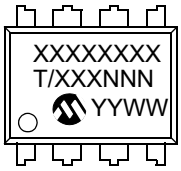
FIGURE 8-3: SEQUENTIAL READ



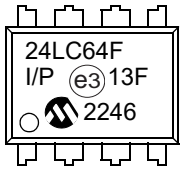
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

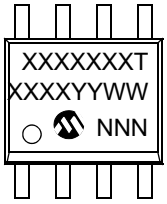
8-Lead PDIP (300 mil)



Example:

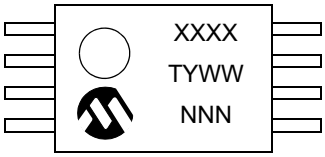


8-Lead SOIC (3.90 mm)

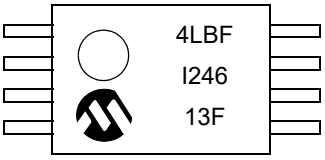


Example:

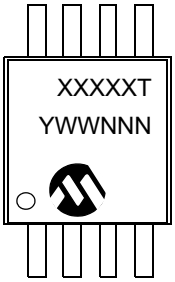
8-Lead TSSOP



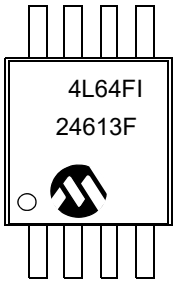
Example:



8-Lead MSOP

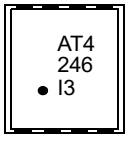


Example:

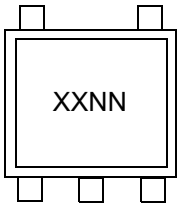


8-Lead 2x3 TDFN

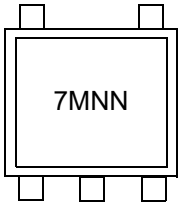
Example:



5-Lead SOT-23



Example:



Part Number	1st Line Marking Codes							
	MSOP	PDIP	SOIC	TSSOP	TDFN		SOT-23	
					I Temp.	E Temp.	I Temp.	E Temp.
24AA64F	4A64FT	24AA64F	24AA64FT	4ABF	AT1	—	7MNN	—
24LC64F	4L64FT	24LC64F	24LC64FT	4LBF	AT4	AT5	7QNN	7RNN
24FC64F	4F64FT	24FC64F	24FC64FT	4FBF	A7D	—	7UNN	—

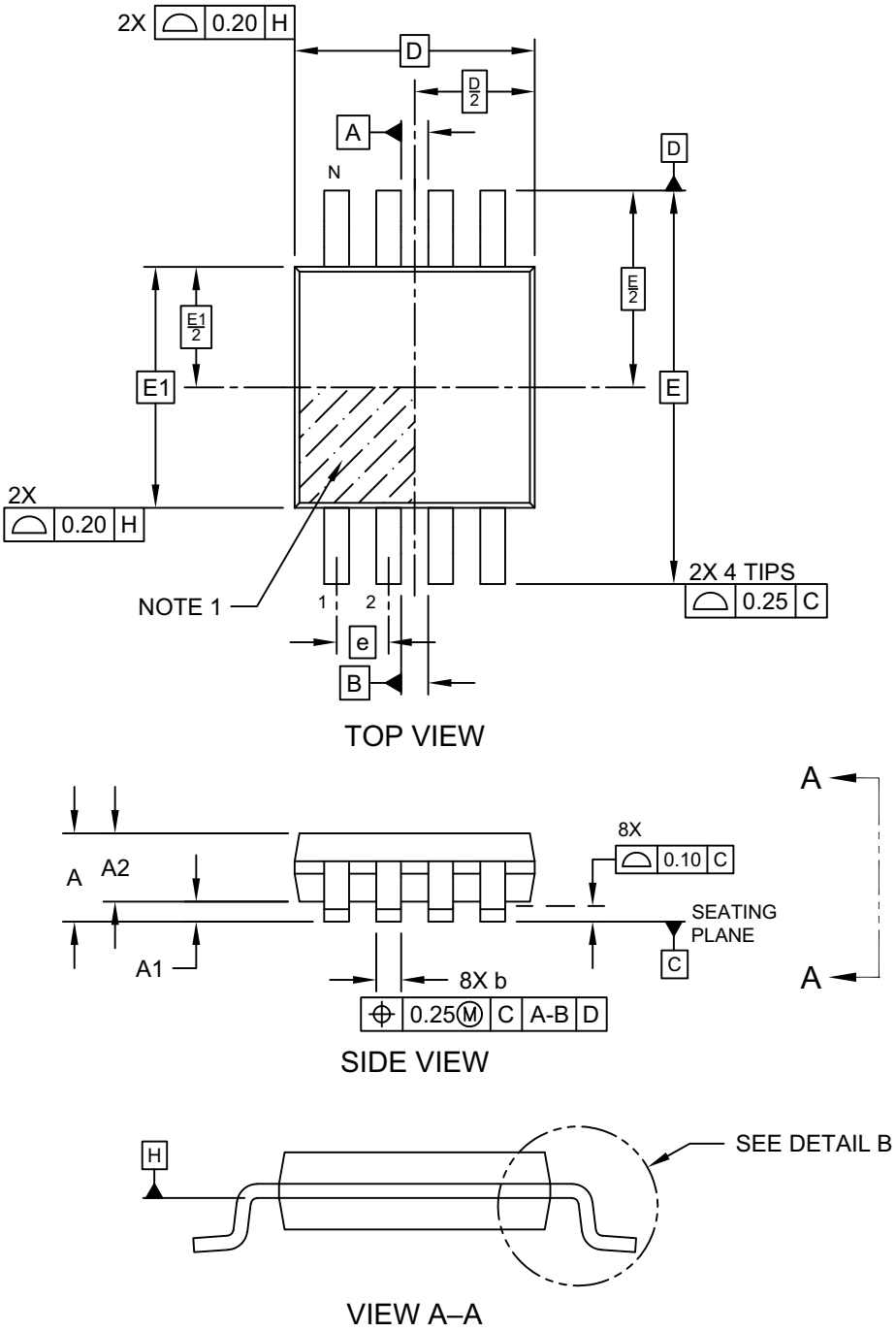
Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	ROHS-compliant JEDEC® designator for Matte Tin (Sn)

Note: For very small packages with no room for the ROHS-compliant JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

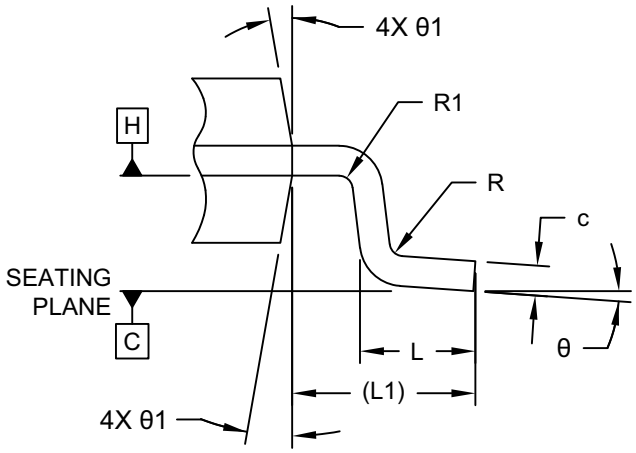
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



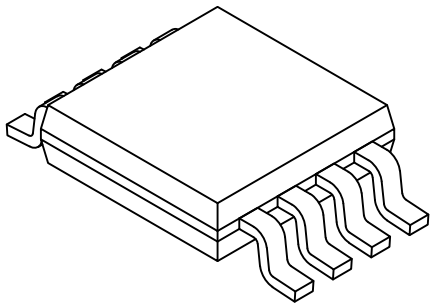
Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

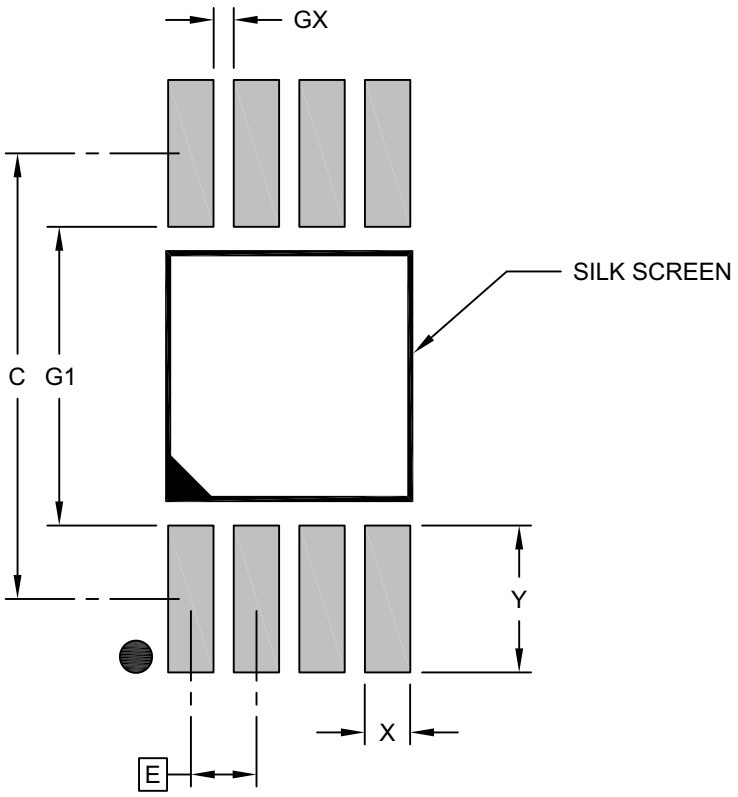
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

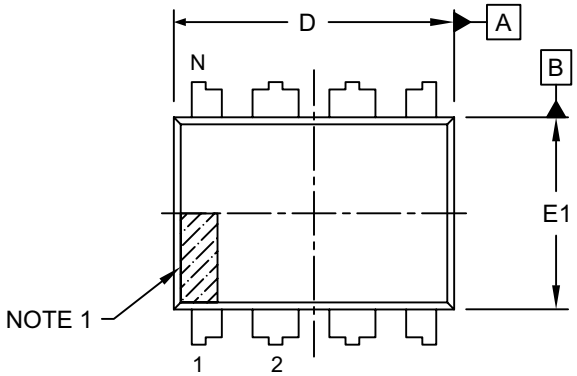
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

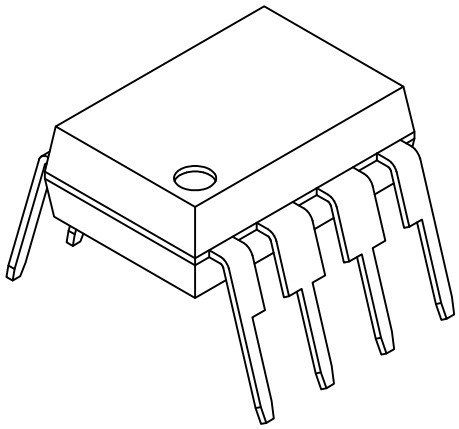
Microchip Technology Drawing C04-2111-MS Rev F

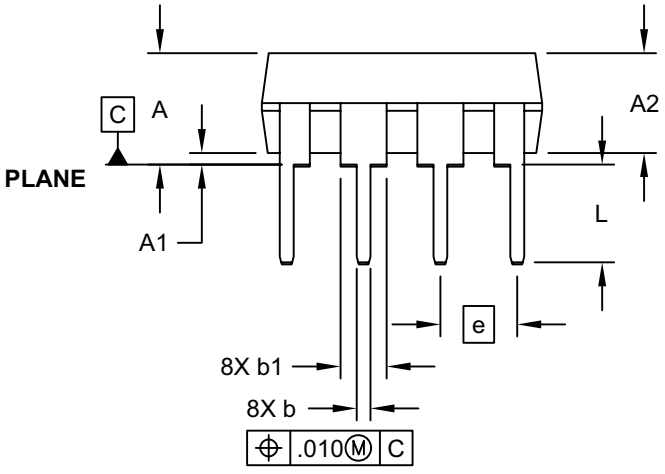
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

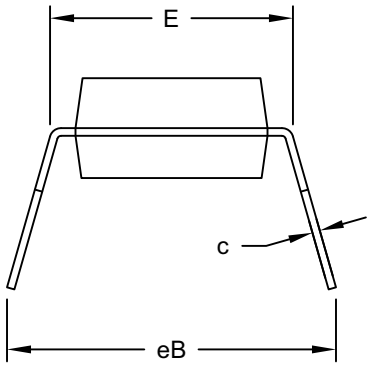


TOP VIEW





SIDE VIEW

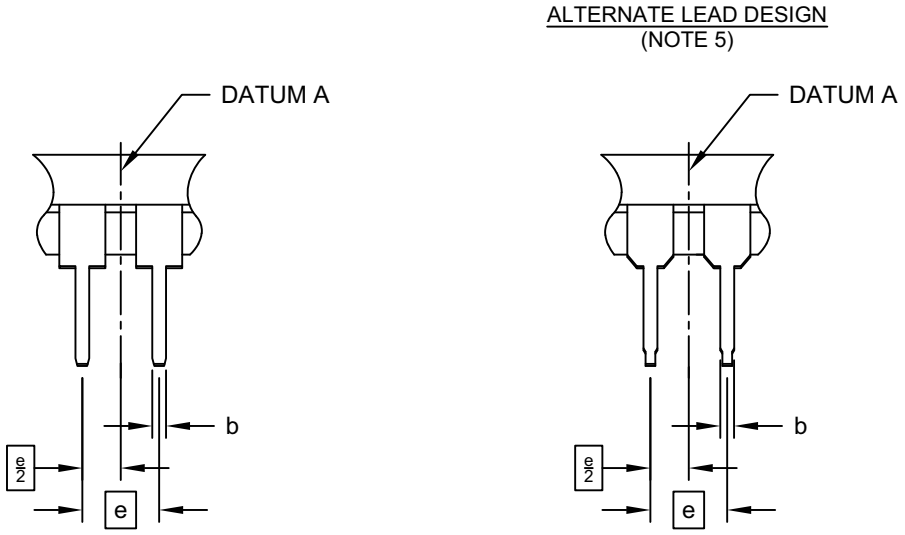


END VIEW

Microchip Technology Drawing No. C04-018-P Rev F Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

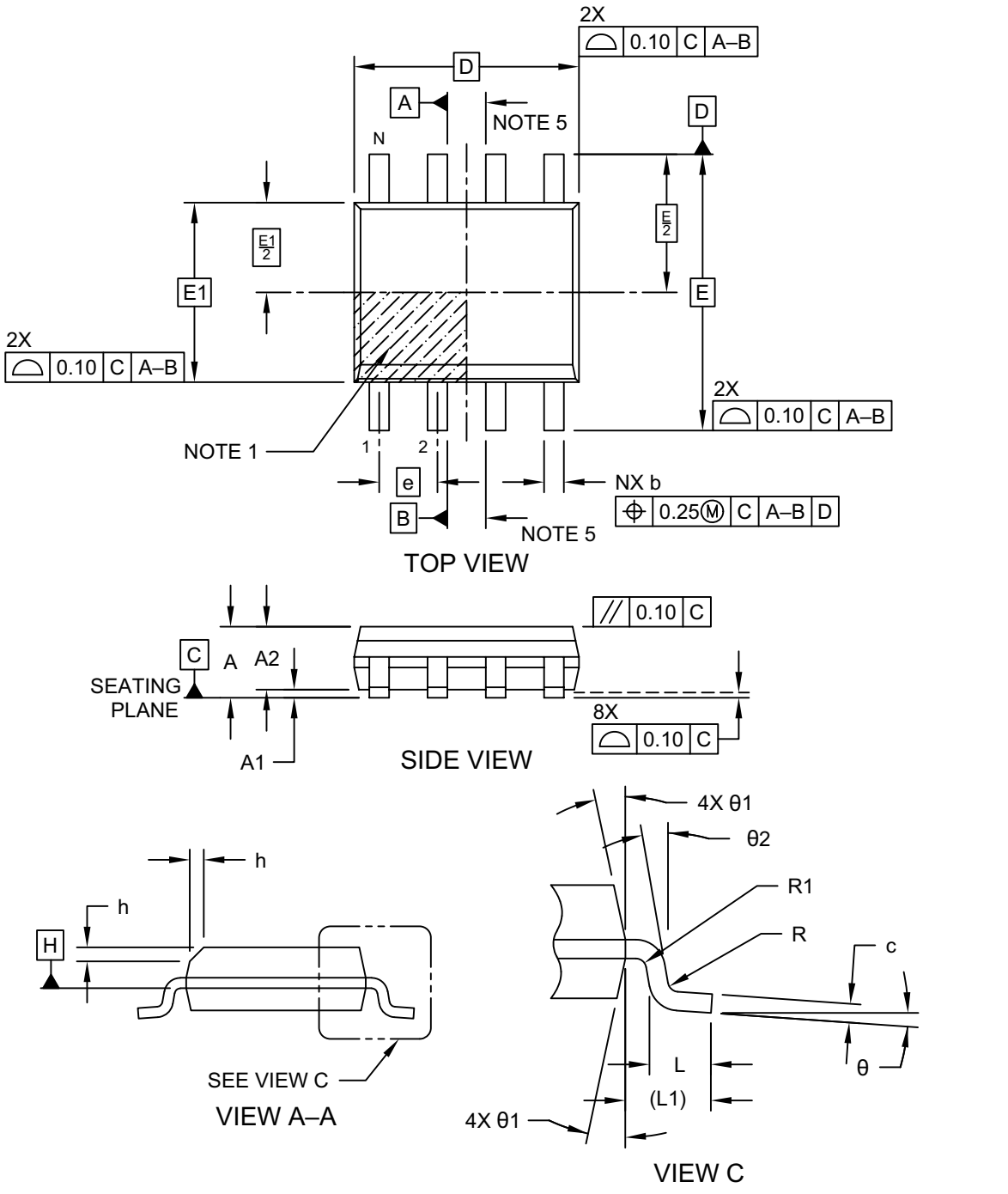
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

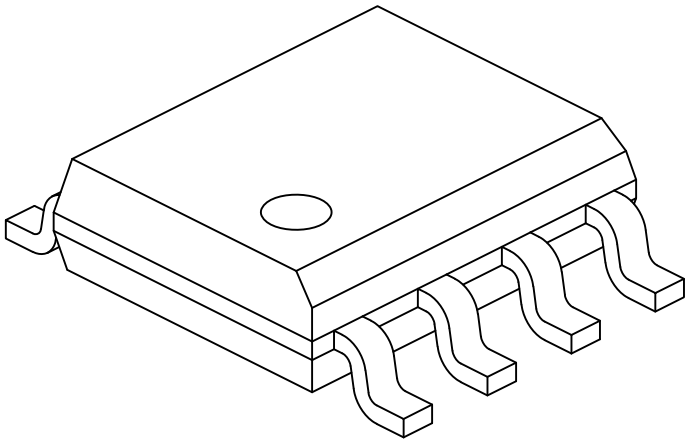
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

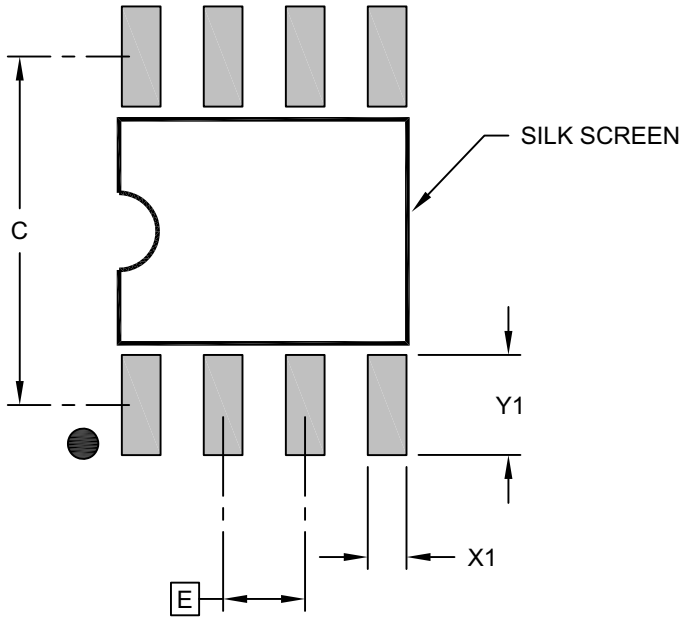
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

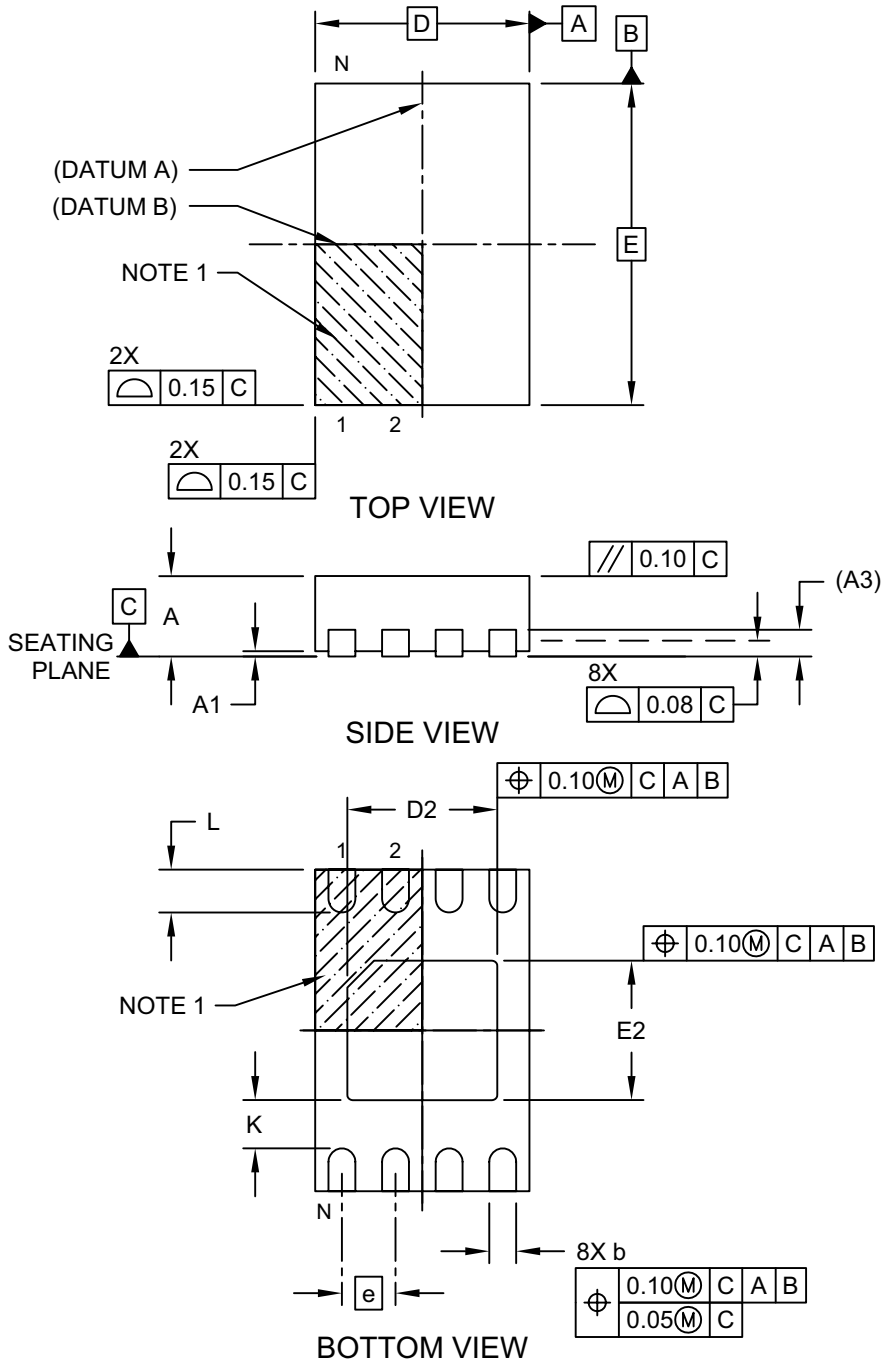
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev K

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]
With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

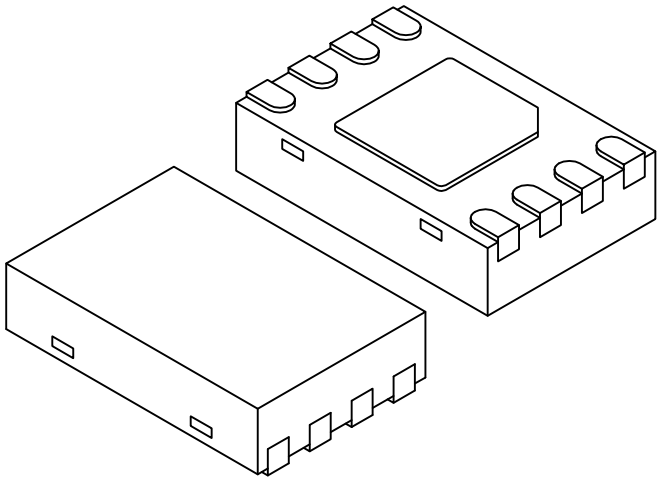
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Exposed Pad Width	E2	1.25	1.30	1.35
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

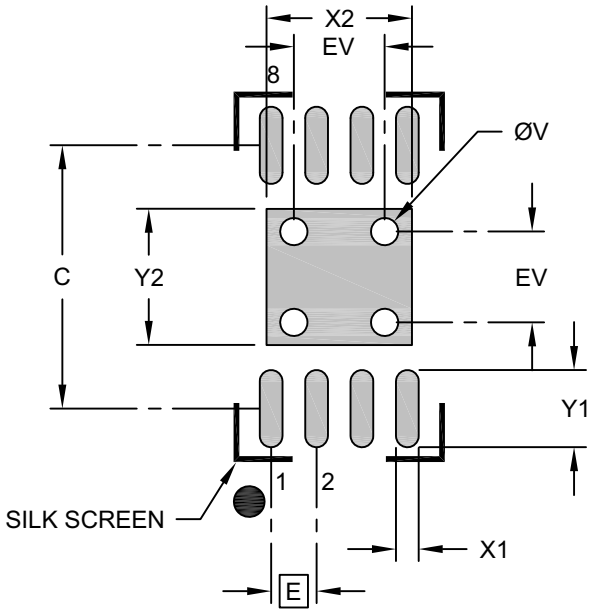
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.50
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.25
Contact Pad Length (X8)	Y1			0.85
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

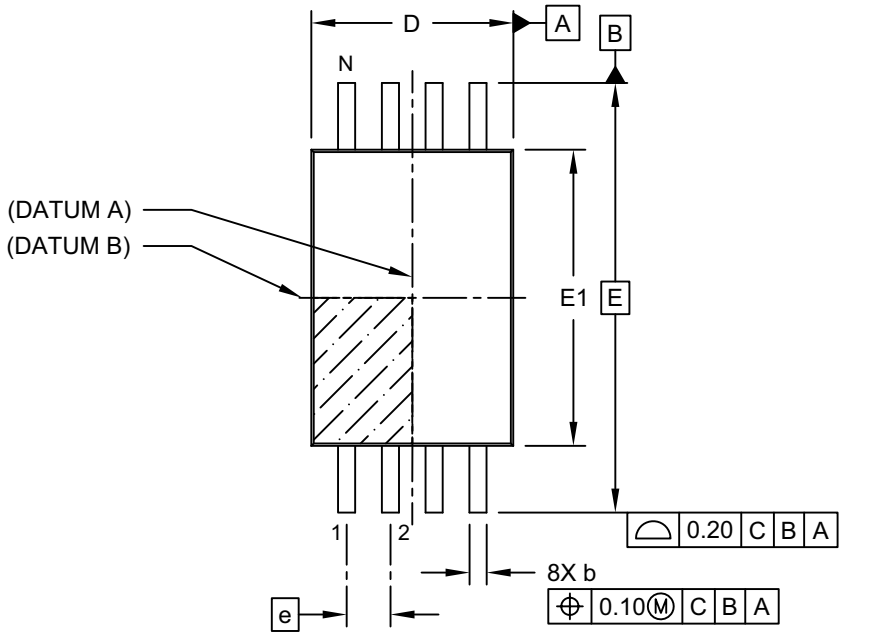
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

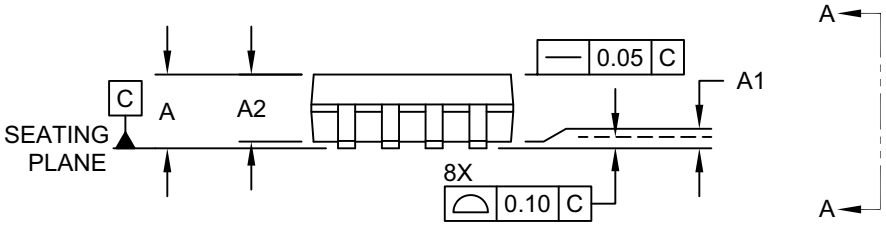
Microchip Technology Drawing No. C04-129-MN Rev. B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

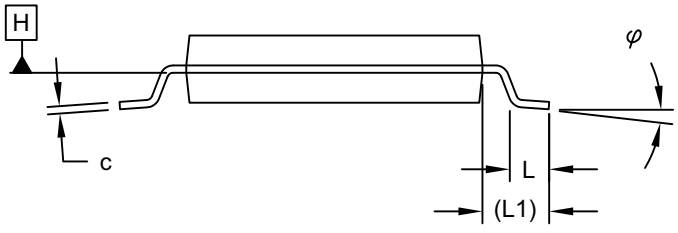
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

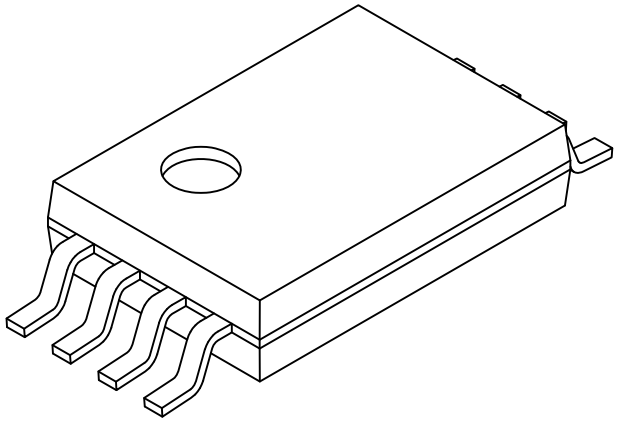


VIEW A-A

Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	-
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

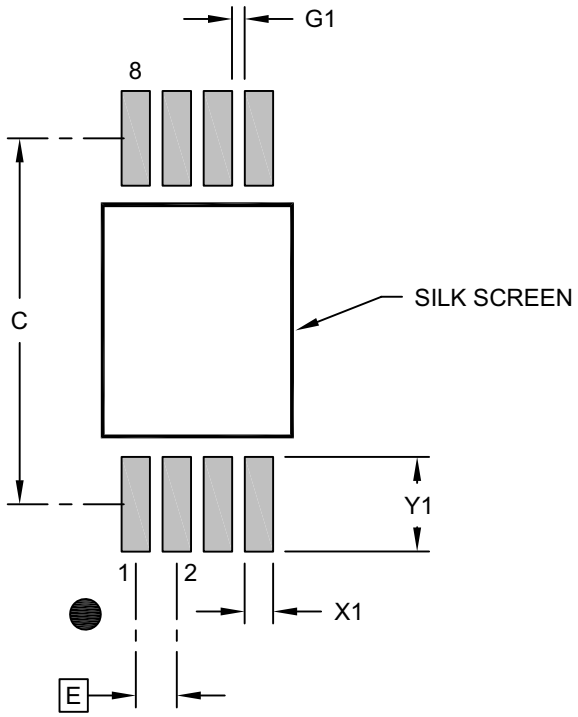
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

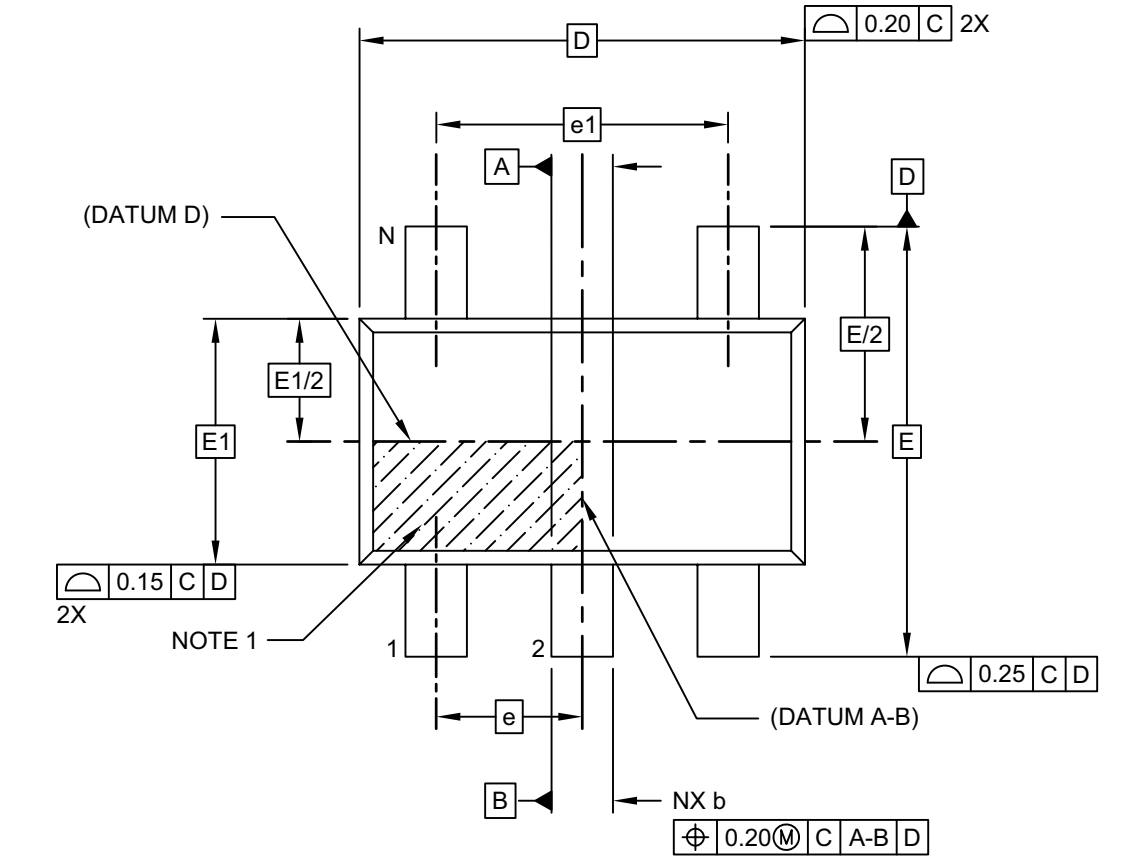
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

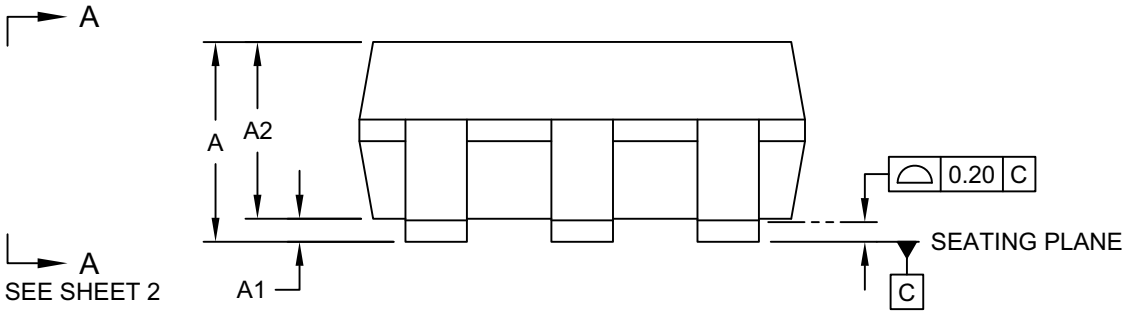
Microchip Technology Drawing C04-2086 Rev B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

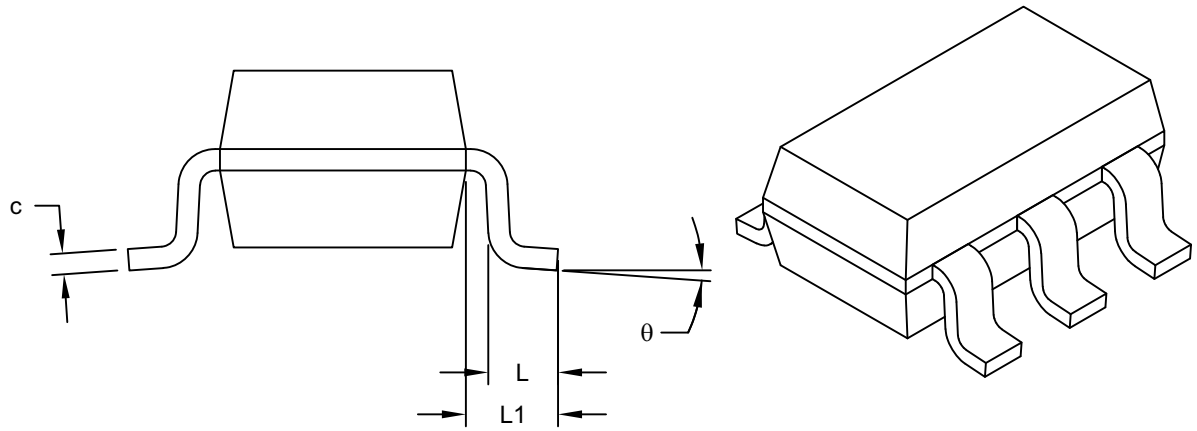


SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

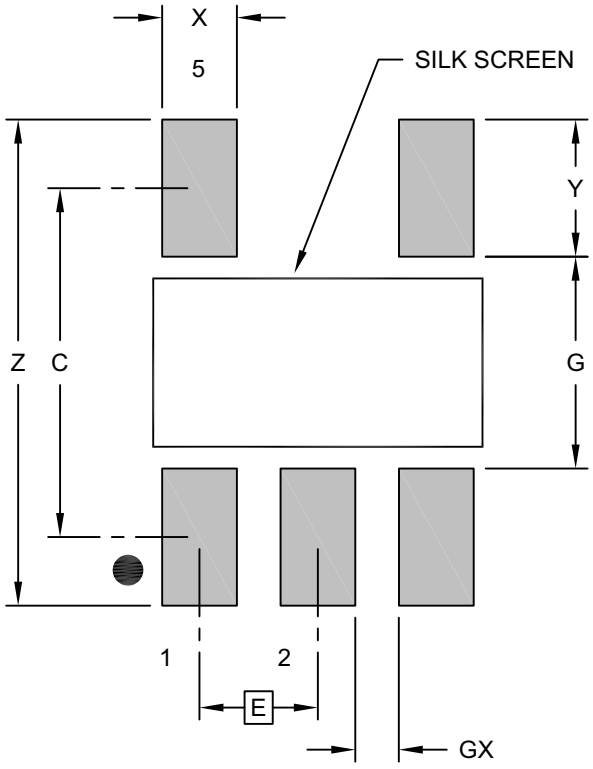
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev H

APPENDIX A: REVISION HISTORY

Revision C (01/2023)

Updated formatting to current template; Replaced terminology “Master” and “Slave” with “Host” and “Client” respectively.

Revision B (04/2012)

Added 24FC64F part.

Revision A (05/2009)

Initial Release.

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PART NO.	[X](1)	-X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	24AA64F:	1.7V, 64-Kbit I^2C Serial EEPROM
	24LC64F:	2.5V, 64-Kbit I^2C Serial EEPROM
	24FC64F:	1.7V, 64-Kbit I^2C Serial EEPROM
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	T =	Tape and Reel(1)
Temperature Range:	I =	-40°C to +85°C (Industrial
	E =	-40°C to +125°C (Extended)
Package:	P =	Plastic Dual In-Line - 300 mil Body, 8-Lead (PDIP)
	SN =	Plastic Small Outline - Narrow 3.90 mm Body, 8-Lead (SOIC)
	ST =	Plastic Thin Shrink Small Outline - 4.4 mm, 8-Lead (TSSOP)
	MS =	Plastic Micro Small Outline Package, 8-Lead (MSOP)
	MNY(2) =	Plastic Dual Flat, No Lead Package - 2x3x0.75 mm body, 8-Lead TDFN (Tape and Reel only)
	OT =	Plastic Small Outline Transistor, 5-Lead SOT-23 (Tape and Reel only)

Examples:

a) 24AA64F-I/P: 1.7V Serial EEPROM, Industrial Temperature, PDIP package

b) 24AA64F-I/SN: 1.7V Serial EEPROM, Industrial Temperature, SOIC package

c) 24AA64FT-I/ST: 1.7V Serial EEPROM, Industrial Temperature, Tape and Reel, TSSOP package

d) 24LC64F-I/P: 2.5V Serial EEPROM, Industrial Temperature, PDIP package

e) 24LC64F-E/MS: 2.5V Serial EEPROM, Extended Temperature, MSOP package

f) 24LC64F-I/OT: 2.5V Serial EEPROM, Industrial Temperature, SOT-23 package

g) 24FC64FT-E/MNY: 1.7V Serial EEPROM, Extended Temperature, Tape and Reel, TDFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

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