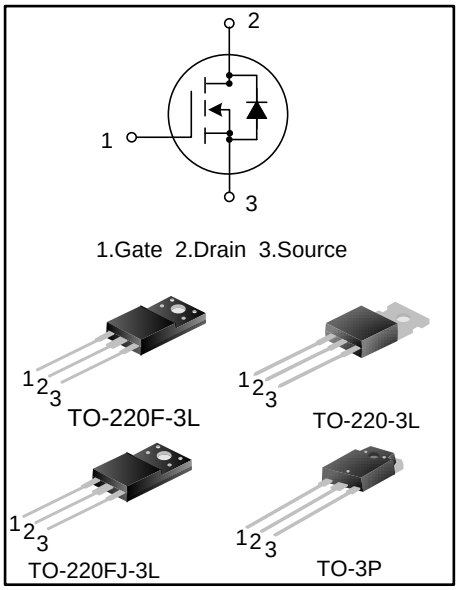
24A, 600V DP MOS POWER TRANSISTOR

GENERAL DESCRIPTION

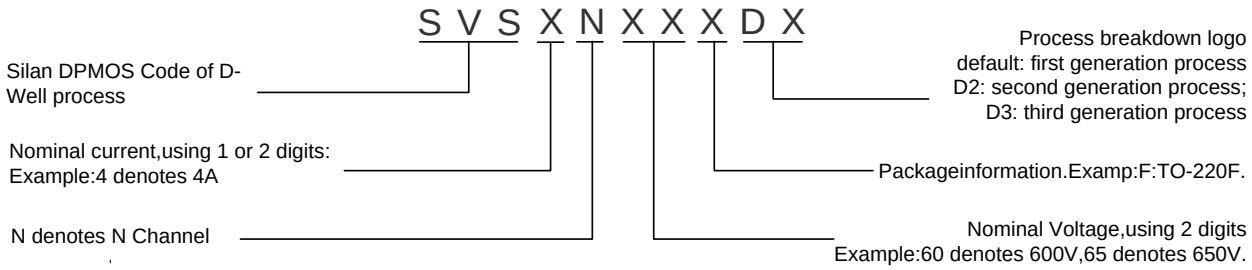
SVS24N60F(FJ)(PN)(T)D2 is an N-channel enhancement mode high voltage power MOSFET produced using Silan's DP MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, for example. it is suitable for hard and soft switching topologies.



FEATURES

- 24A, 600V, $R_{DS(on)(typ.)}$=0.14Ω@V_{GS}=10V
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVS24N60FJD2	TO-220FJ-3L	24N60FJD2	Halogen free	Tube
SVS24N60FD2	TO-220F-3L	24N60FD2	Halogen free	Tube
SVS24N60PND2	TO-3P	24N60PN	Pb free	Tube
SVS24N60TD2	TO-220-3L	24N60TD2	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise noted)

Characteristics		Symbol	Ratings			Unit
			SVS24N60F/FJD2	SVS24N60PND2	SVS24N60TD2	
Drain-Source Voltage		V_{DS}	600			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	24			A
	T_C=100°C		15			
Drain Current Pulsed		I_{DM}	96			A
Power Dissipation(T_C=25°C)		P_D	47	240	208	W
-Derate above 25°C			0.38	1.92	1.7	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	1062			mJ
Reverse Diode dv/dt (Note 2)		dv/dt	15			V/ns
MOSFET dv/dt Ruggedness (Note 3)		dv/dt	50			V/ns
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value			Unit
		SVS24N60F/FJD2	SVS24N60PND2	SVS24N60TD2	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.66	0.52	0.6	°C/W
Thermal Resistance, junction-to-Ambient	$R_{\theta JA}$	62.5	50	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V，I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V，V_{GS}=0V	--	--	1.0	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V，V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}，I_D=250μA	2.0	--	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V，I_D=12A	--	0.14	0.16	Ω
Gate resistance	R_g	f=1.0MHz		2.6		Ω
Input Capacitance	C_{iss}	V_{DS}=100V，V_{GS}=0V，f=1.0MHz	--	1480	--	pF
Output Capacitance	C_{oss}		--	84	--	
Reverse Transfer Capacitance	C_{rss}		--	4.8	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V，V_{GS}=10V，R_G=25Ω，I_D=24A (Note 4,5)	--	21	--	ns
Turn-on Rise Time	t_r		--	74	--	
Turn-off Delay Time	$t_{d(off)}$		--	213	--	
Turn-off Fall Time	t_f		--	65	--	
Total Gate Charge	Q_g	V_{DD}=480V，V_{GS}=10V，I_D=24A (Note 4,5)	--	49	--	nC
Gate-Source Charge	Q_{gs}		--	12	--	
Gate-Drain Charge	Q_{gd}		--	25	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	24	A
Pulsed Source Current	I_{SM}		--	--	96	
Diode Forward Voltage	V_{SD}	I_S=24A，V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	V_{DD}=50V，I_F=24A，dI_F/dt=100A/μs	--	442	--	ns
Reverse Recovery Charge	Q_{rr}		--	7.0	--	μC

Notes:

1. L=79mH，I_{AS}=4.8A，V_{DD}=100V， R_G=25Ω， starting T_J=25°C;
2. V_{DS}=0~400V,I_{SD}<=24A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

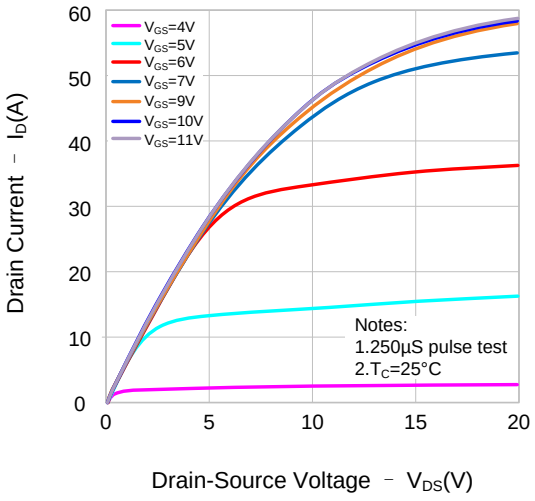


Figure 2. Transfer Characteristics

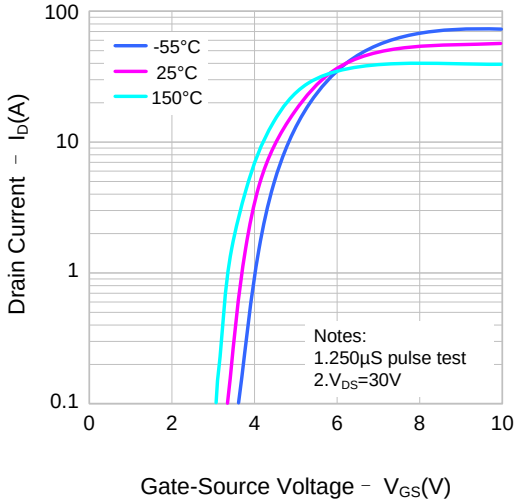


Figure 3. On-Resistance Variation vs. Drain Current

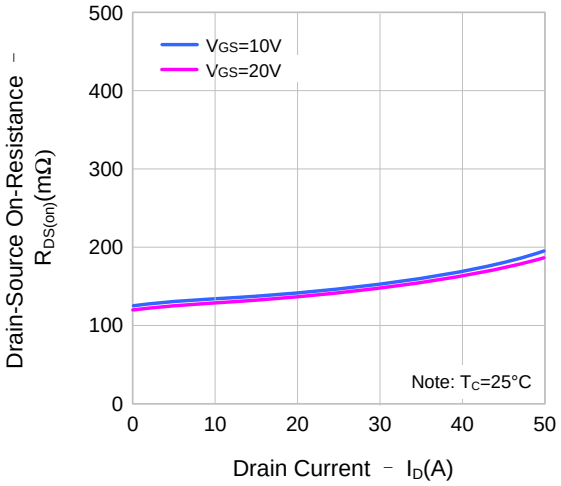


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

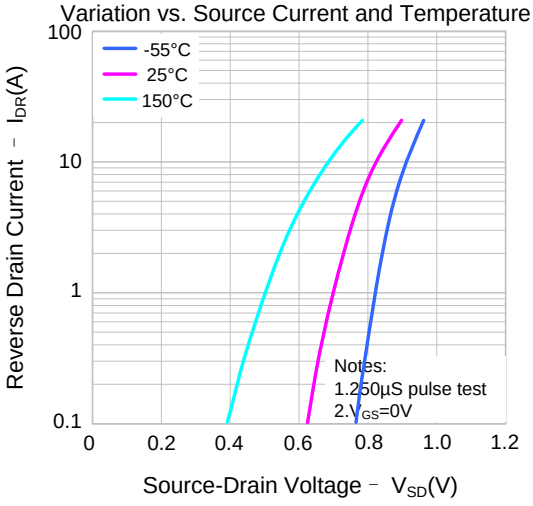


Figure 5. Capacitance Characteristics

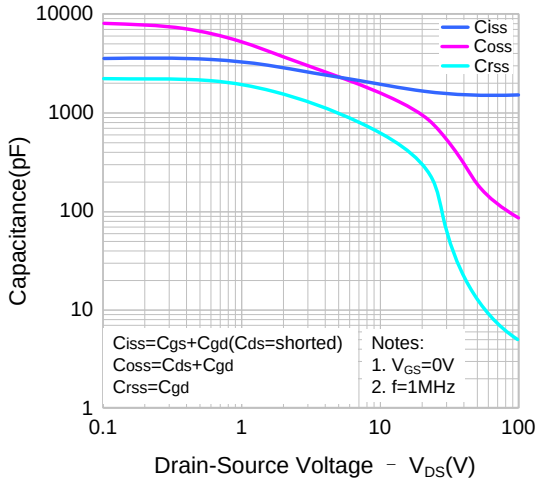
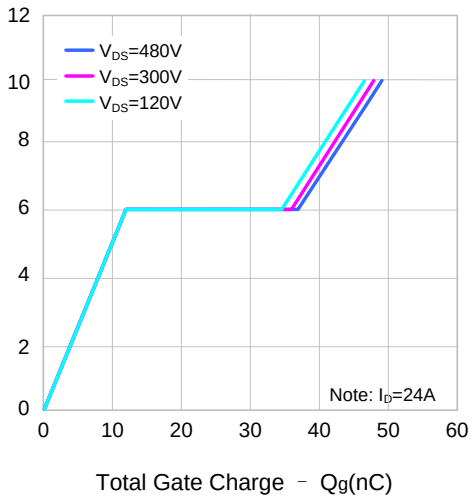


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

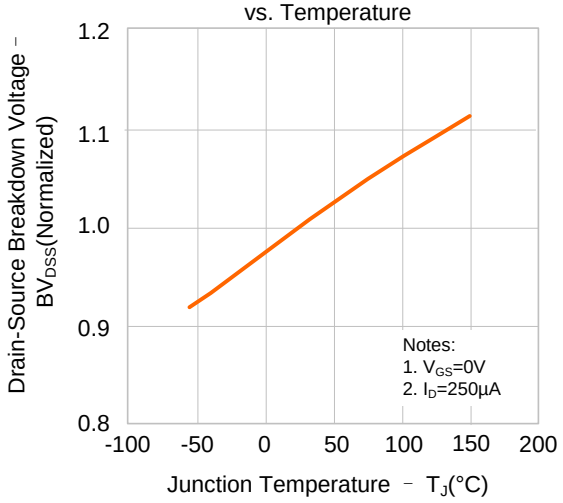


Figure 8. On-resistance Variation vs. Temperature

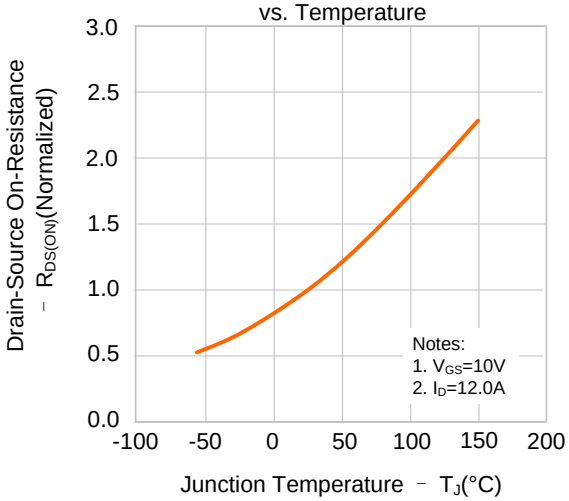


Figure 9-1. Max. Safe Operating Area (SVS24N60F/FJD2)

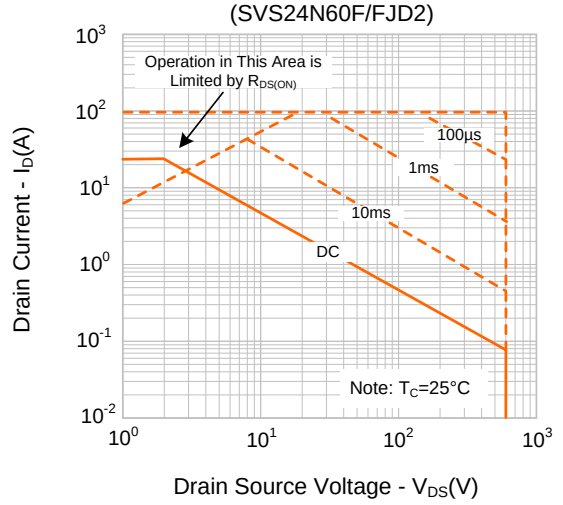


Figure 9-2. Max. Safe Operating Area (SVS24N60PND2)

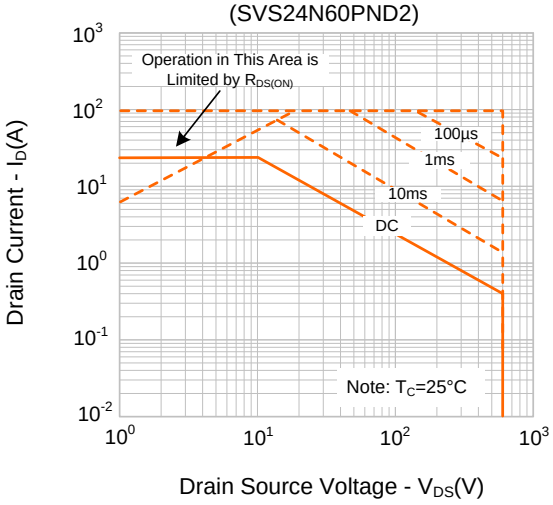
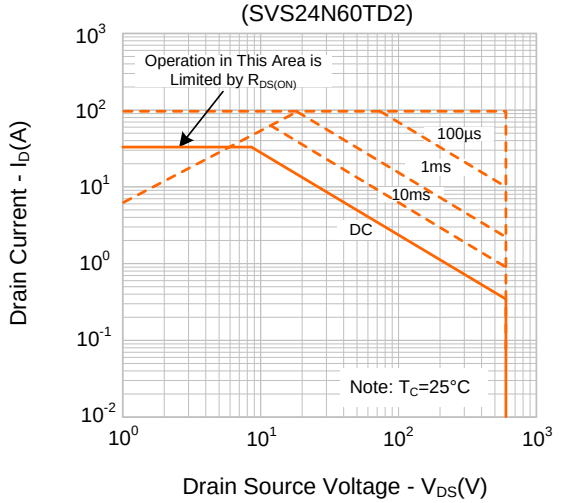
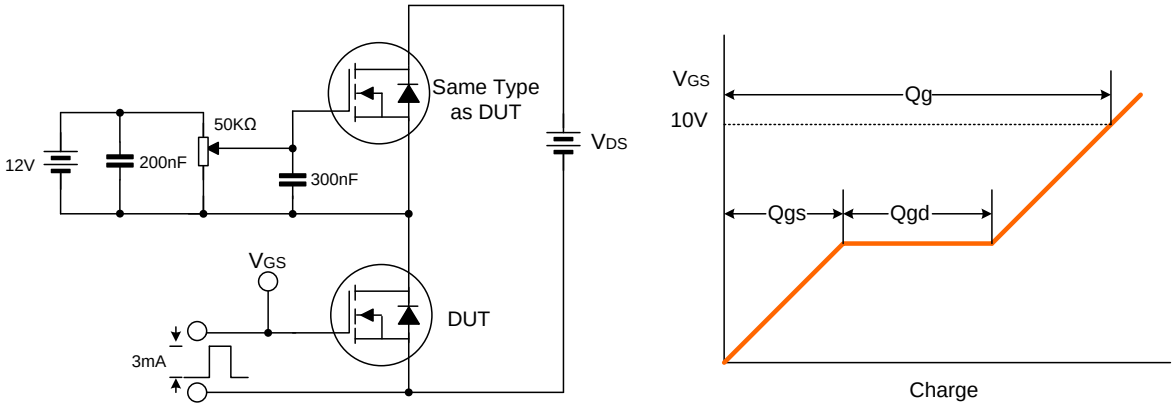


Figure 9-3. Max. Safe Operating Area (SVS24N60TD2)

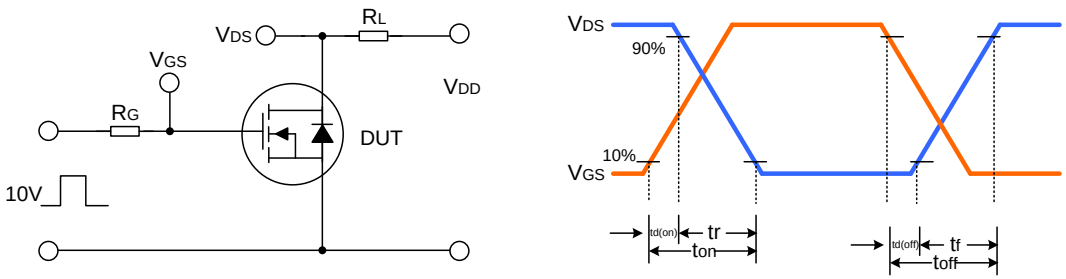


TYPICAL TEST CIRCUIT

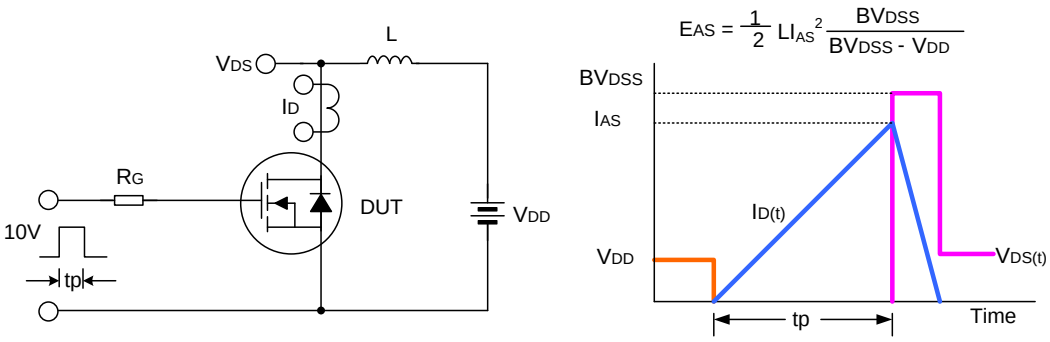
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



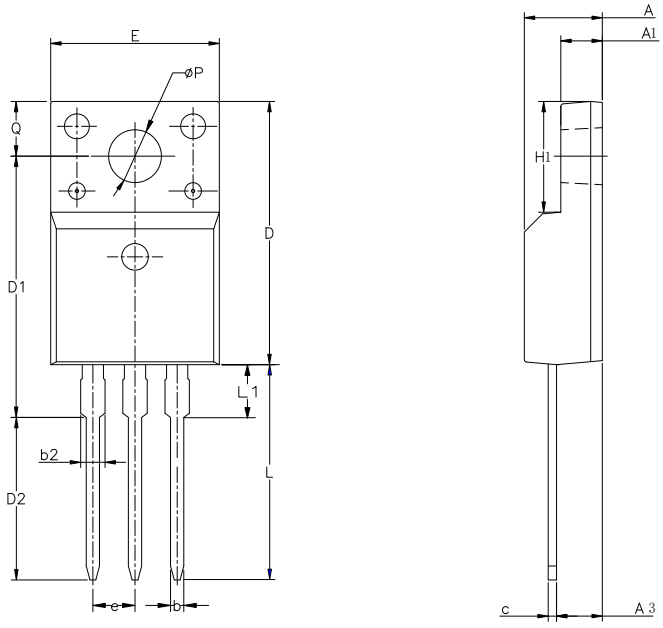
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220FJ-3L

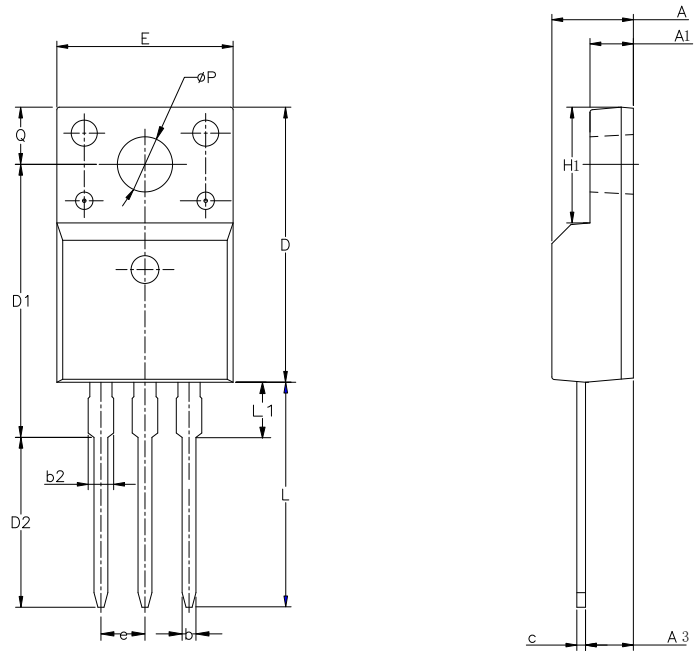
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-220F-3L

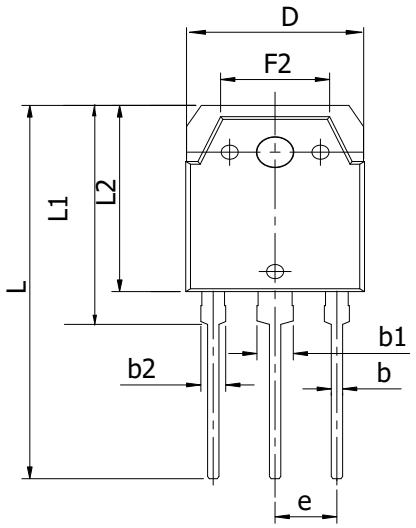
UNIT: mm

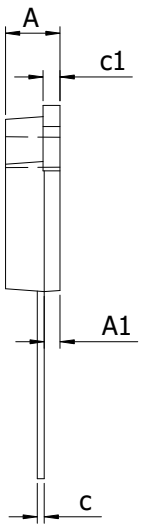


SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

PACKAGE OUTLINE (continued)

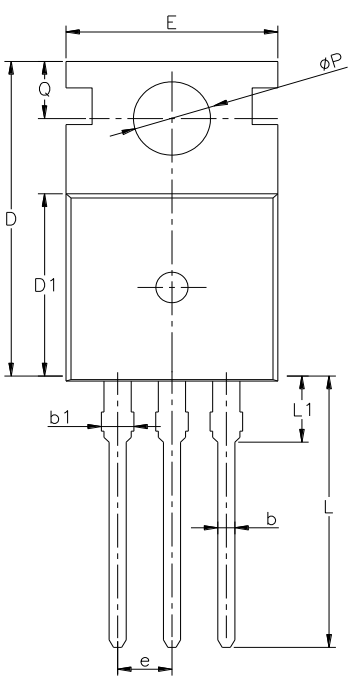
TO-3P **UNIT: mm**

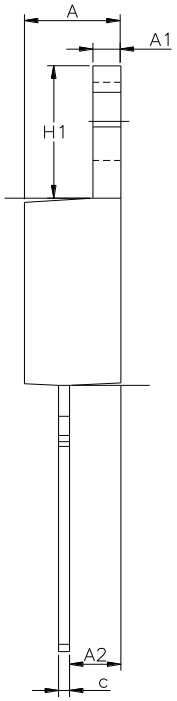




SYMBOL	MIN	NOM	MAX
A	4.4	\	5.2
C1	1.2	\	1.8
A1	1.2	\	2
b	0.7	1	1.3
b1	2.7	3	3.3
b2	1.7	2	2.3
D	15	15.5	16
C	0.4	0.6	0.8
F2	8.5	\	10
e	5.45typ		
L1	22.6	\	23.6
L	39	\	41.5
L2	19.5	\	21

TO-220-3L **UNIT: mm**





SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ΦP	3.40	3.70	3.90
Q	2.60	—	3.20

Disclaimer :

- **Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
- **All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.**
- **Silan will supply the best possible product for customers!**

Part No.:	SVS24N60F(FJ)(PN)(T)D2	Document Type:	Datasheet
Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http: //www.silan.com.cn

Rev.: 1.3

Revision History:

1. Modify the value of P_D and R_{JC}
2. Update SOA

Rev.: 1.2

Revision History:

1. Add SVS24N60TD2（T0-220-3L）

Rev.: 1.1

Revision History:

1. Modify characteristics and Fig 5 and 6

Rev.: 1.0

Revision History:

1. First release