



24NM70

Power MOSFET

24A, 700V N-CHANNEL SUPER-JUNCTION MOSFET

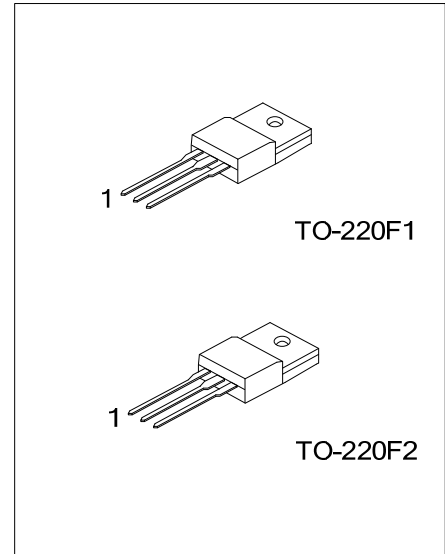
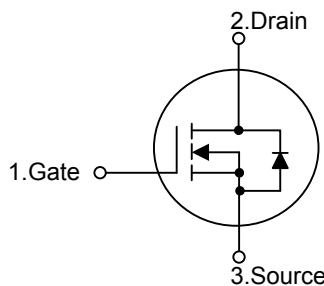
DESCRIPTION

The **UTC 24NM70** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

FEATURES

- * $R_{DS(ON)} \leq 0.19\Omega$ @ $V_{GS}=10V, I_D=12A$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



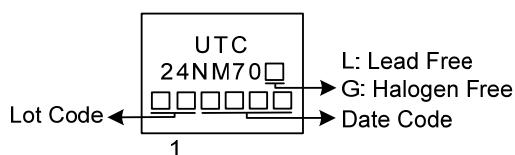
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
24NM70L-TF1-T	24NM70G-TF1-T	TO-220F1	G	D	S	Tube
24NM70L-TF2-T	24NM70G-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>24NM70G-TF1-T</p>	<p>(1) T: Tube</p> <p>(2) TF1: TO-220F1, TF2: TO-220F2</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	700	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	24	A
	Pulsed (Note 2)	I_{DM}	96	A
Avalanche Current (Note 2)		I_{AR}	5.2	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	879	mJ
Peak Diode Recovery dv/dt		dv/dt	6.3	V/ns
Power Dissipation		P_D	32	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 65\text{mH}$, $I_{AS} = 5.2\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 24\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.98	$^\circ\text{C}/\text{W}$

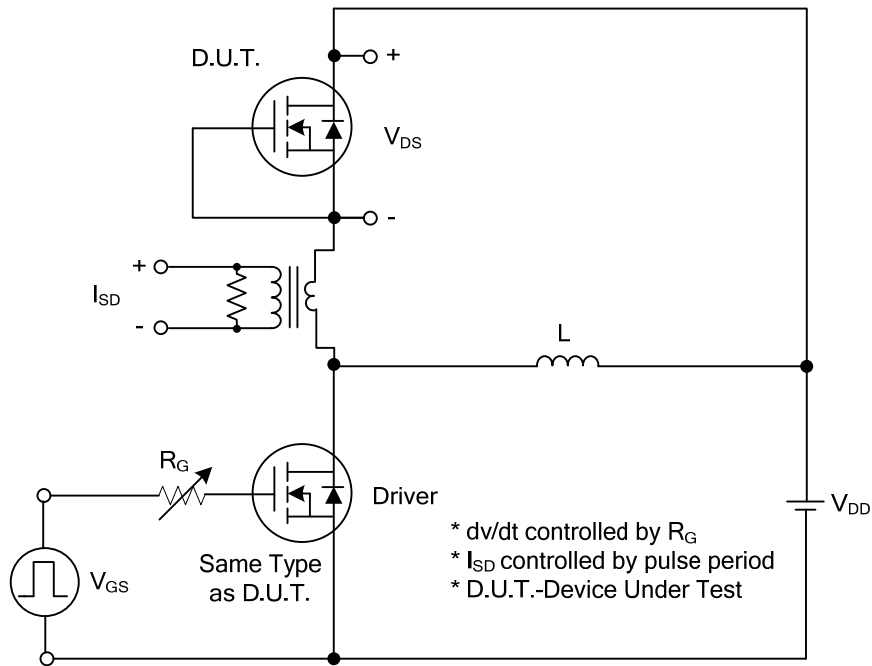
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	700			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 700\text{V}$, $V_{GS} = 0\text{V}$			10	μA
Gate- Source Leakage Current	I_{GSS}	Forward			+100	nA
		Reverse			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{V}$, $I_D = 12\text{A}$		0.18	0.19	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$		2000		pF
Output Capacitance	C_{OSS}			1280		pF
Reverse Transfer Capacitance	C_{RSS}			110		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS} = 560\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 24\text{A}$ $I_G = 1\text{mA}$ (Note1, 2)		70		nC
Gate to Source Charge	Q_{GS}			9.6		nC
Gate to Drain Charge	Q_{GD}			27.2		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS} = 100\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 24\text{A}$, $R_G = 25\Omega$ (Note1, 2)		26		ns
Rise Time	t_R			32		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			240		ns
Fall-Time	t_F			110		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				24	A
Maximum Body-Diode Pulsed Current	I_{SM}				96	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S = 24\text{A}$, $V_{GS} = 0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S = 24\text{A}$, $V_{GS} = 0\text{V}$, $dI_F/dt = 100\text{A}/\mu\text{s}$		520		ns
Body Diode Reverse Recovery Charge	Q_{rr}			10.5		μC

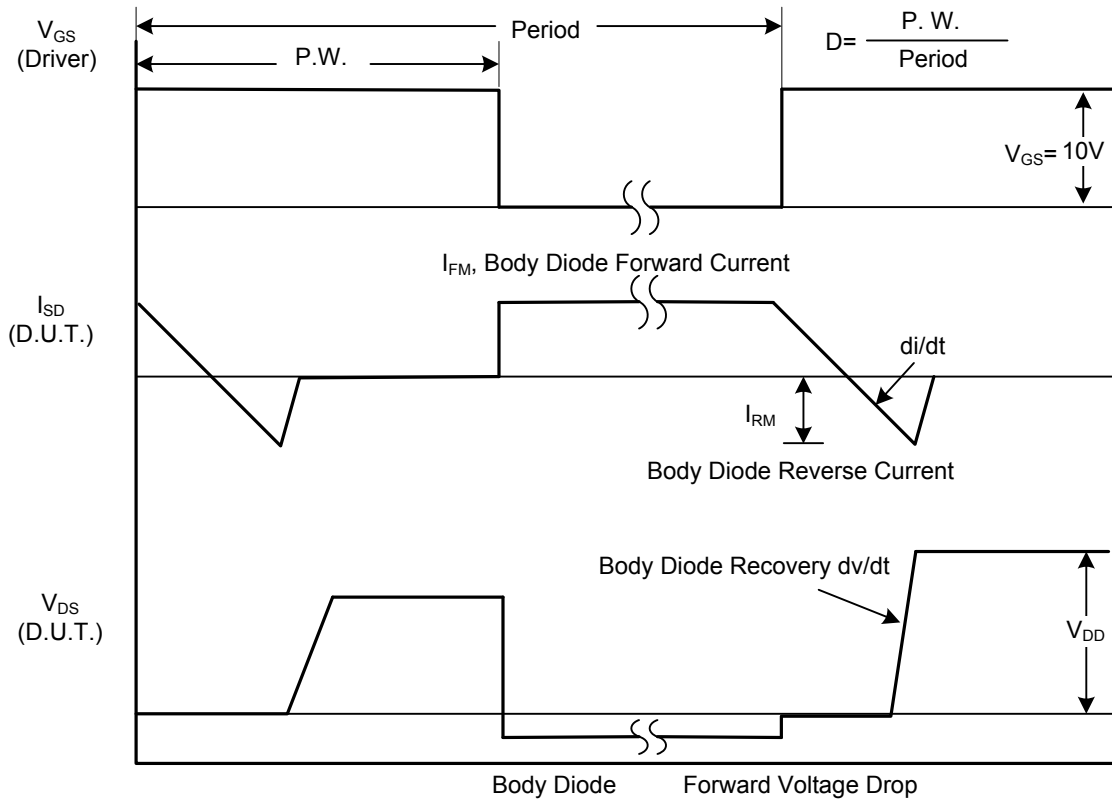
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



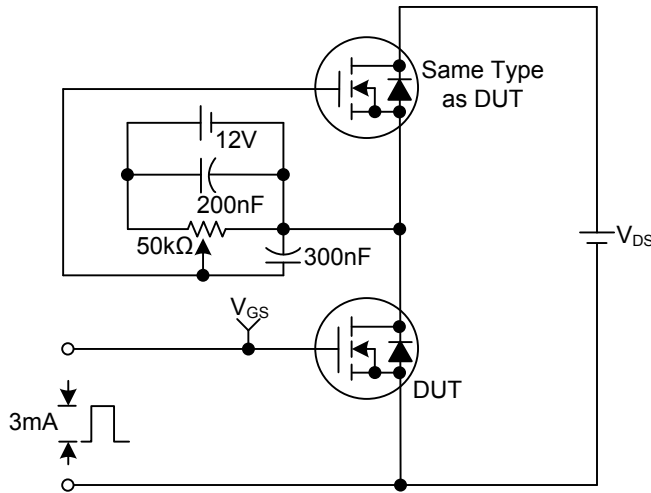
Peak Diode Recovery dv/dt Test Circuit



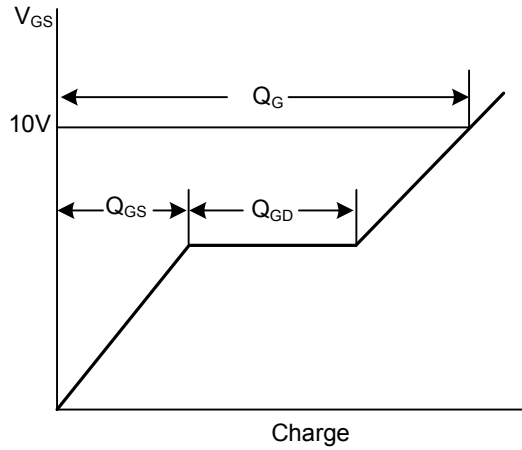
Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS

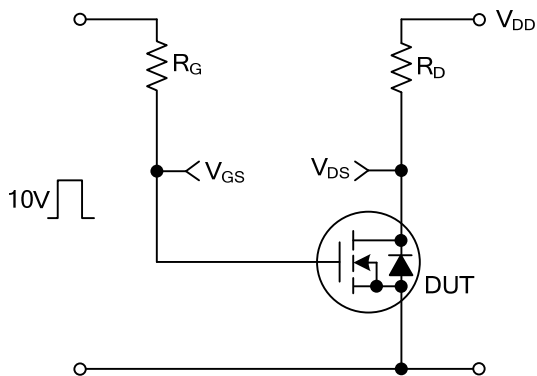
Gate Charge Test Circuit



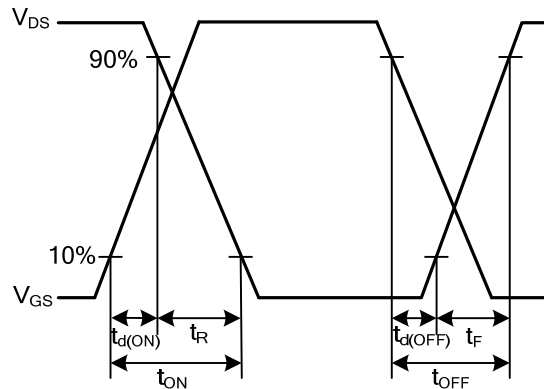
Gate Charge Waveforms



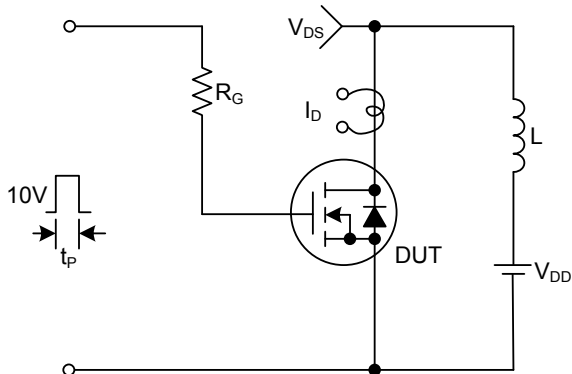
Resistive Switching Test Circuit



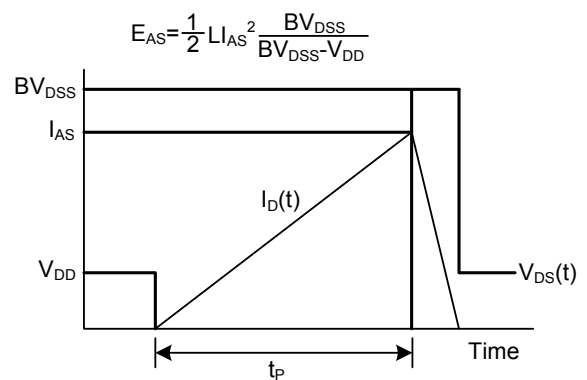
Resistive Switching Waveforms



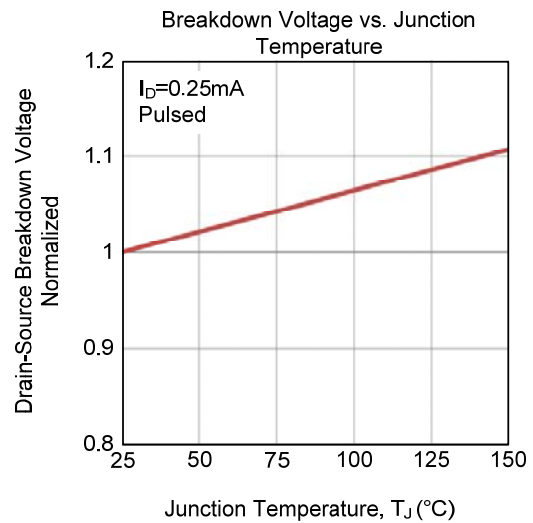
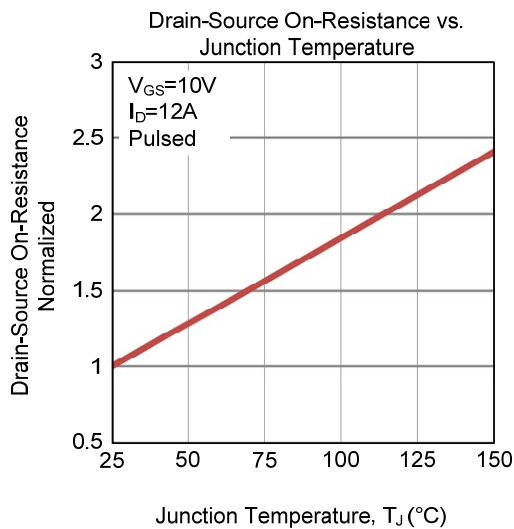
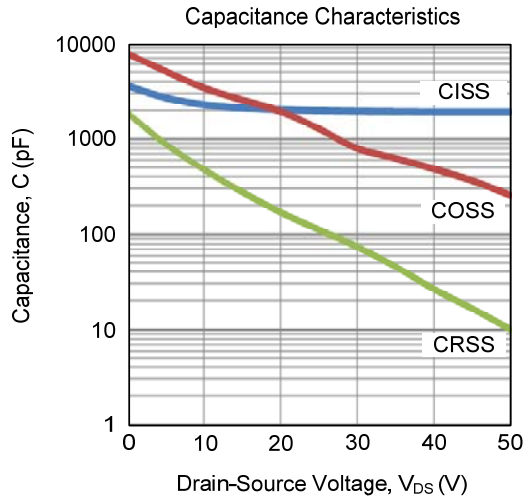
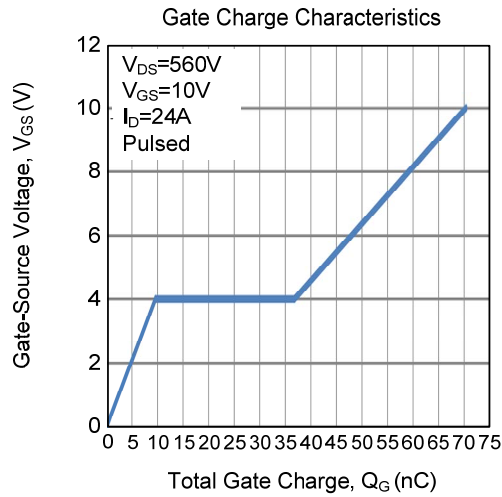
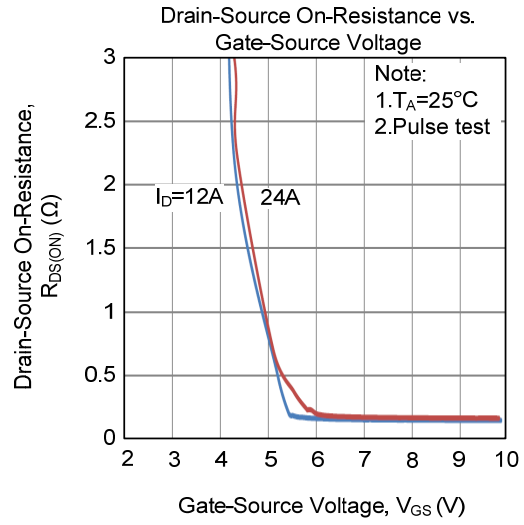
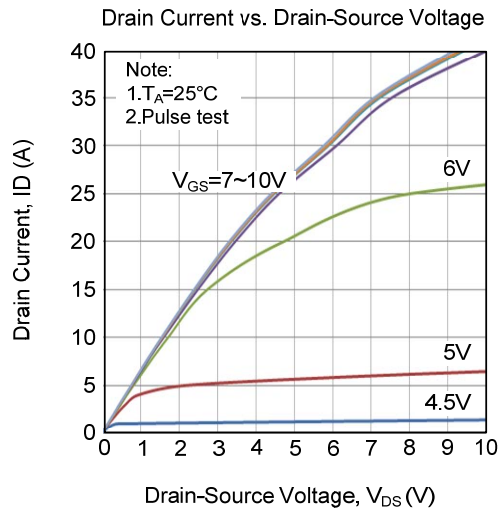
Unclamped Inductive Switching Test Circuit



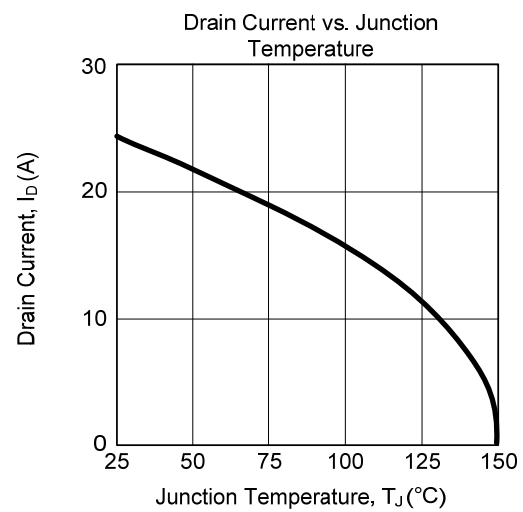
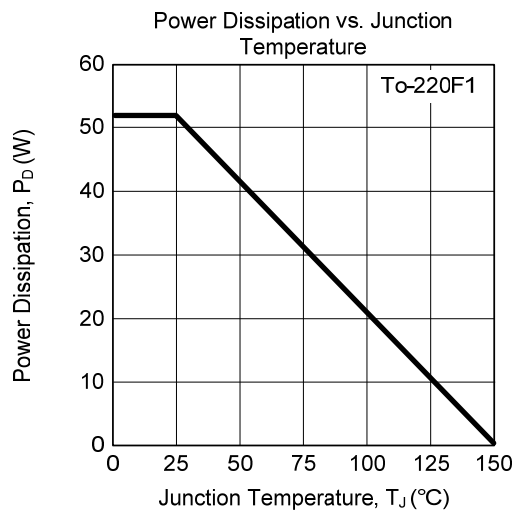
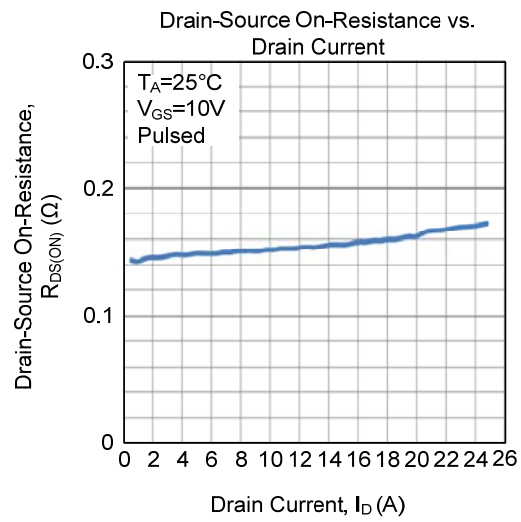
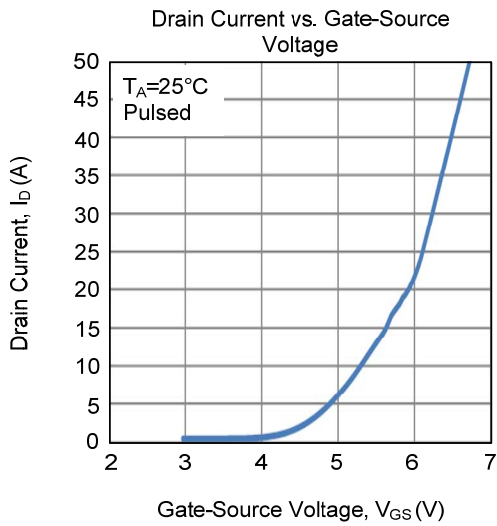
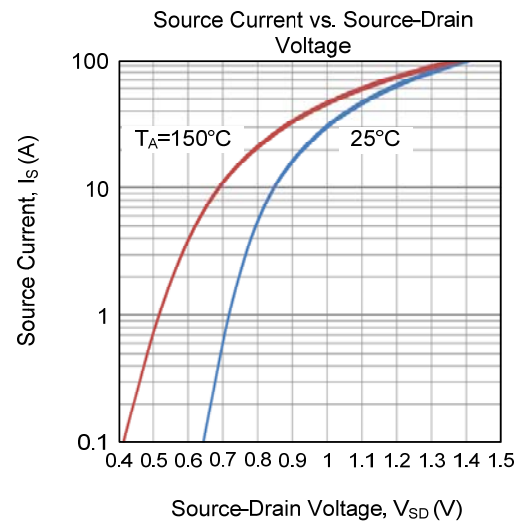
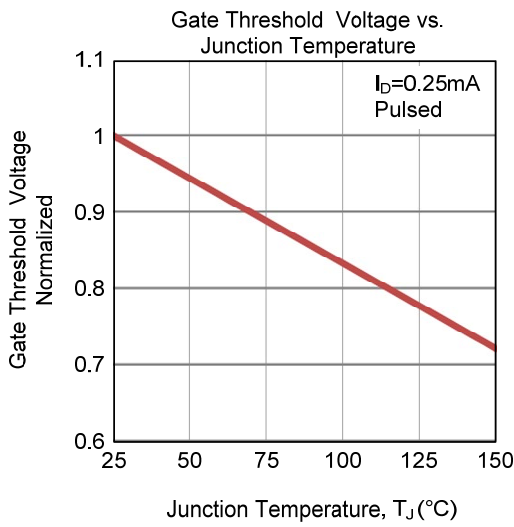
Unclamped Inductive Switching Waveforms



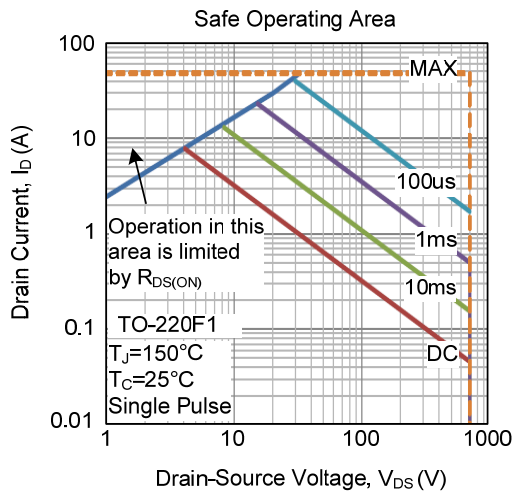
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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