S25FL032A

32 Megabit CMOS 3.0 Volt Flash Memory with 50MHz SPI (Serial Peripheral Interface) Bus

Data Sheet *(Preliminary)*

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S25FL032A

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Data Sheet *(Preliminary)*

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6 V read and program operations
- **Memory Architecture**
  - 64 sectors with 512 Kb each
- **Program**
  - Page Program (up to 256 bytes) in 1.4 ms (typical)
  - Program operations are on a page by page basis
- **Erase**
  - 0.5 s typical sector erase time
  - Bulk erase function
- **Cycling Endurance**
  - 100,000 cycles per sector typical
- **Data Retention**
  - 20 years typical
- **Device ID**
  - JEDEC standard two-byte electronic signature
  - RES command one-byte electronic signature for backward compatibility
- **Process Technology**
  - Manufactured on 0.20 µm MirrorBit™ process technology
- **Package Option**
  - Industry Standard Pinouts
  - 16-pin SO package (300 mils)

Performance Characteristics

- **Speed**
  - 50 MHz clock rate (maximum)
- **Power Saving Standby Mode**
  - Standby Mode 50 µA (max)
  - Deep Power Down Mode 2 µA (typical)

Memory Protection Features

- **Memory Protection**
  - W# pin works in conjunction with Status Register Bits to protect specified memory areas
  - Status Register Block Protection bits (BP2, BP1, BP0) in status register configure parts of memory as read-only

Software Features

- SPI Bus Compatible Serial Interface

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General Description

The S25FL032A is a 3.0 Volt (2.7 V to 3.6 V), single-power-supply Flash memory device. The device consists of 64 sectors, each with 512 Kb memory.

The device accepts data written to SI (Serial Input) and outputs data on SO (Serial Output). The devices are designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply.

The memory can be programmed 1 to 256 bytes at a time, using the Page Program command. The device supports Sector Erase and Bulk Erase commands.

Each device requires only a 3.0 volt power supply (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program operations. This device does not require a V_{PP} supply.

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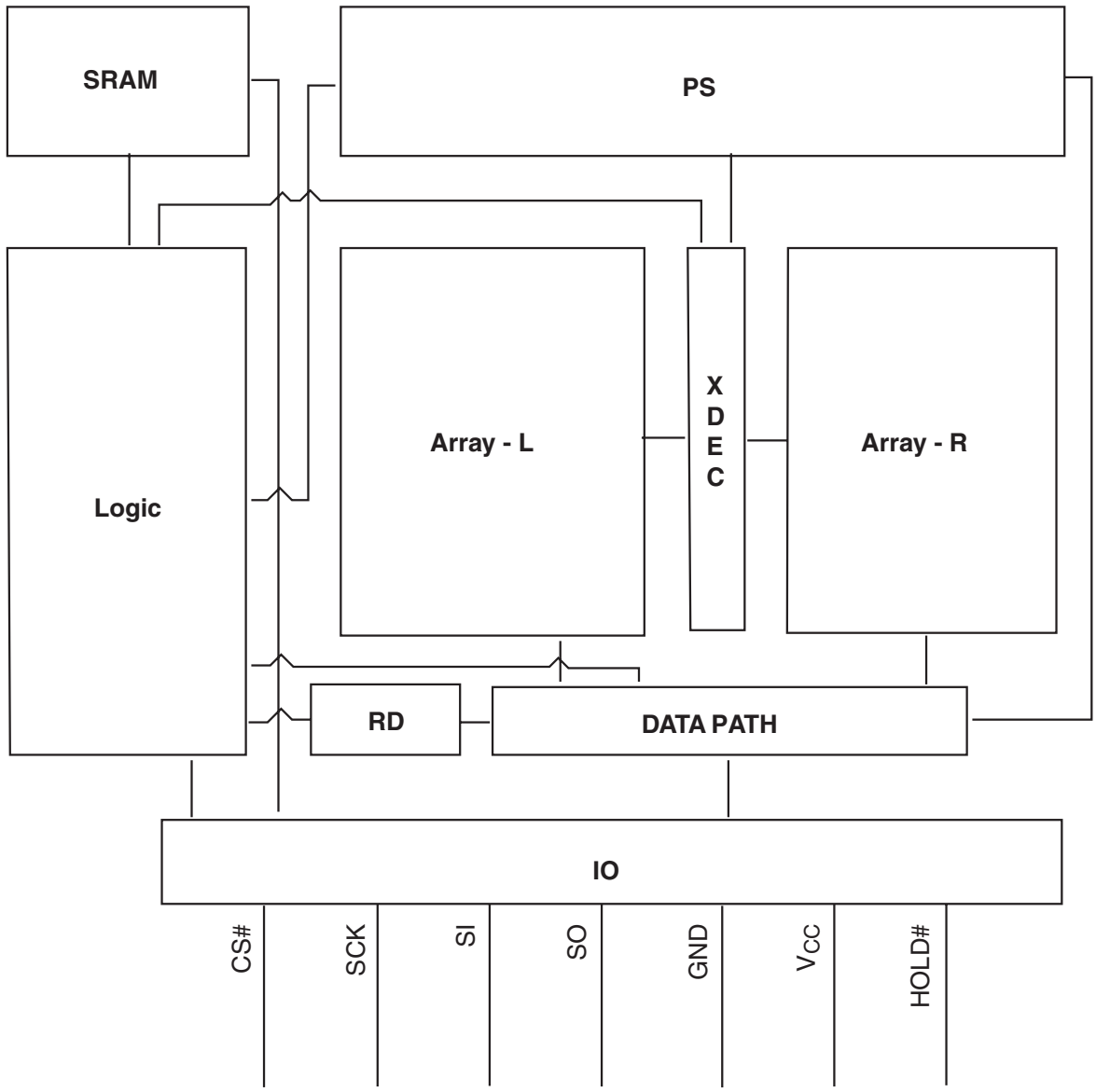
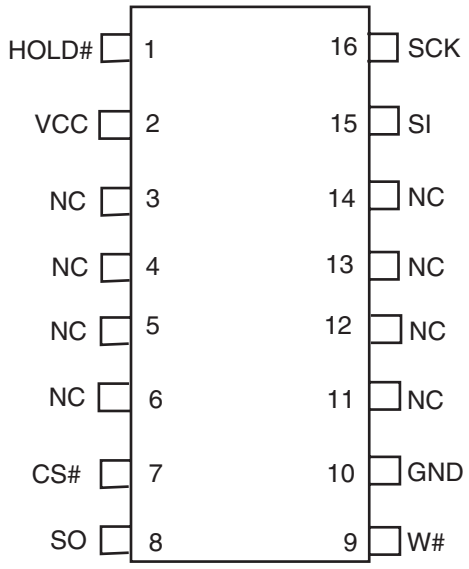


2. Connection Diagrams

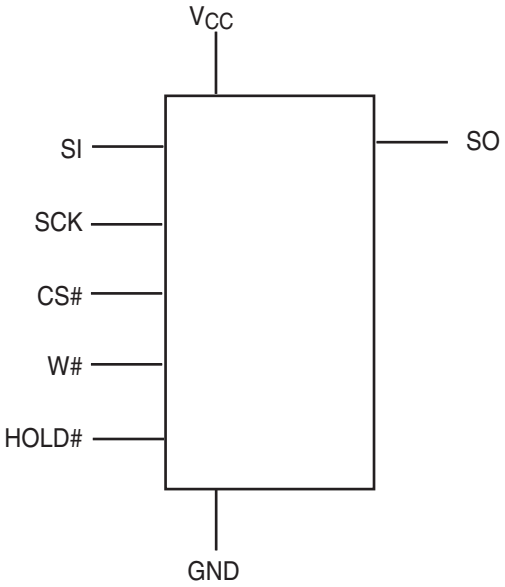
Figure 2.1 16-pin Plastic Small Outline Package (SO)



3. Input/Output Descriptions

Signal Name	I/O	Description
SO (Signal Data Output)	Output	Transfers data serially out of the device on the falling edge of SCK.
SI (Serial Data Input)	Input	Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCK.
SCK (Serial Clock)	Input	Provides serial interface timing. Latches commands, addresses, and data on SI on rising edge of SCK. Triggers output on SO after the falling edge of SCK.
CS# (Chip Select)	Input	Places device in active power mode when driven low. Deselects device and places SO at high impedance when high. After power-up, device requires a falling edge on CS# before any command is written. Device is in standby mode when a program, erase, or Write Status Register operation is not in progress.
HOLD# (Hold)	Input	Pauses any serial communication with the device without deselecting it. When driven low, SO is at high impedance, and all input at SI and SCK are ignored. Requires that CS# also be driven low.
W# (Write Protect)	Input	Protects the memory area specified by Status Register bits BP2:BP0. When driven low, prevents any program or erase command from altering the data in the protected memory area.
V_{CC}	Input	Supply Voltage
GND	Input	Ground

4. Logic Symbol



5. Ordering Information

The ordering part number is formed by a valid combination of the following:

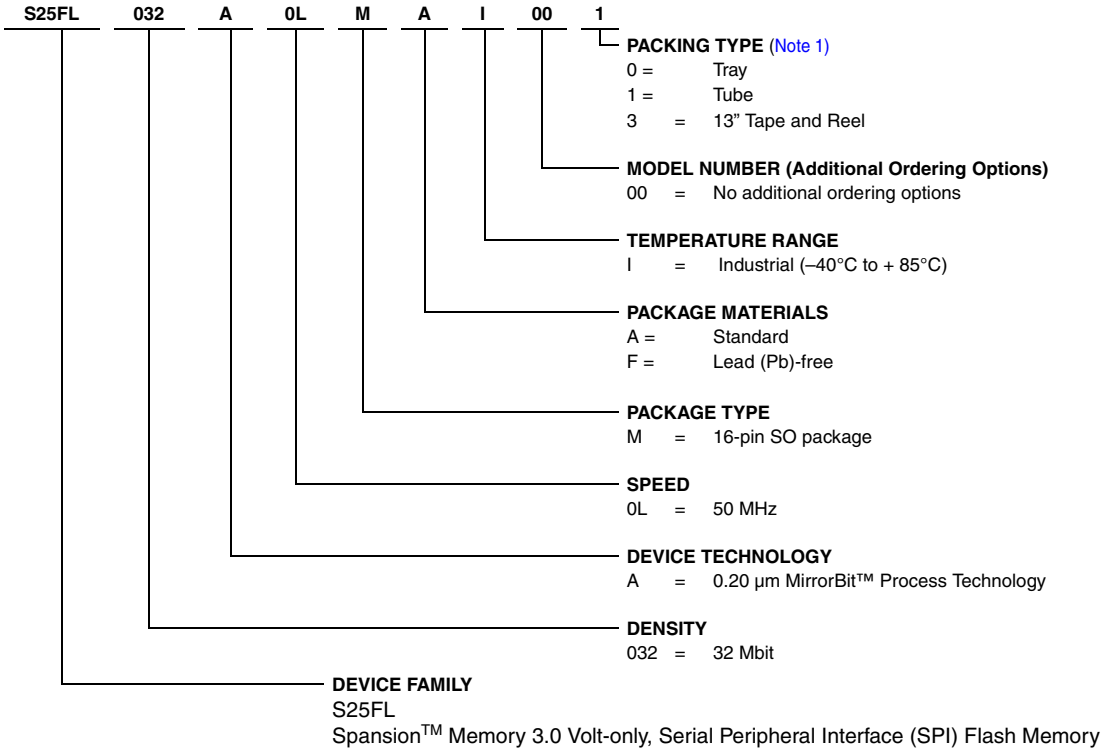


Table 5.1 S25FL032A Valid Combinations Table

S25FL032A Valid Combinations					Package Marking (Note 2)
Base Ordering Part Number	Speed Option	Package & Temperature	Model Number	Packing Type	
S25FL032A	0L	MAI, MFI	00	1, 3 (Note 1)	FL032A + (Temp) + (Note 3)

Notes

1. *Contact your local sales office for availability.*
2. *Package marking omits leading "S25" and speed, package, and model number form.*
3. A *for standard package (non-Pb free);* F *for Pb-free package.*

5.1 Valid Combinations

Table 5.1 lists the valid combinations configurations planned to be supported in volume for this device.

6. Spansion SPI Modes

A microcontroller can use either of its two SPI modes to control Spansion SPI Flash memory devices:

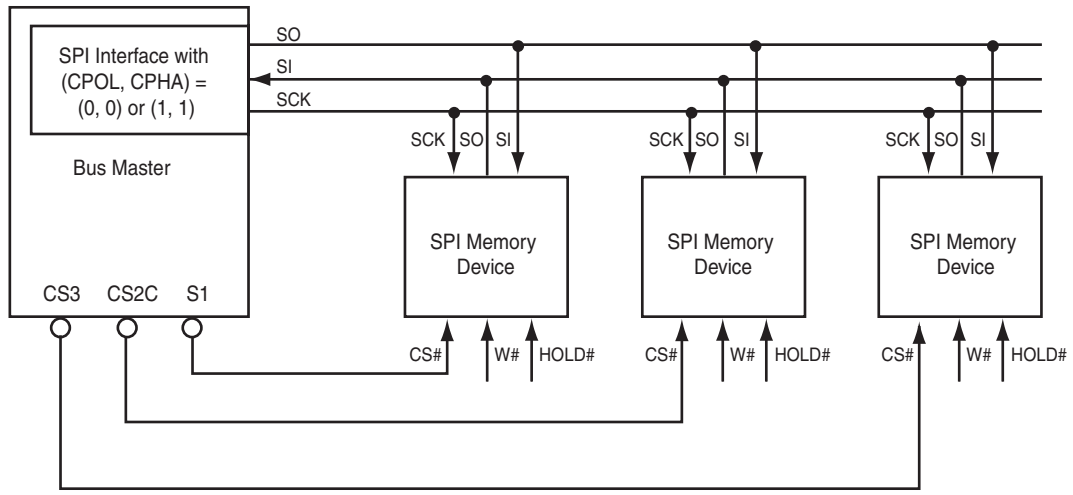
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode, SCK is as shown in Figure 6.2 for each of the two modes:

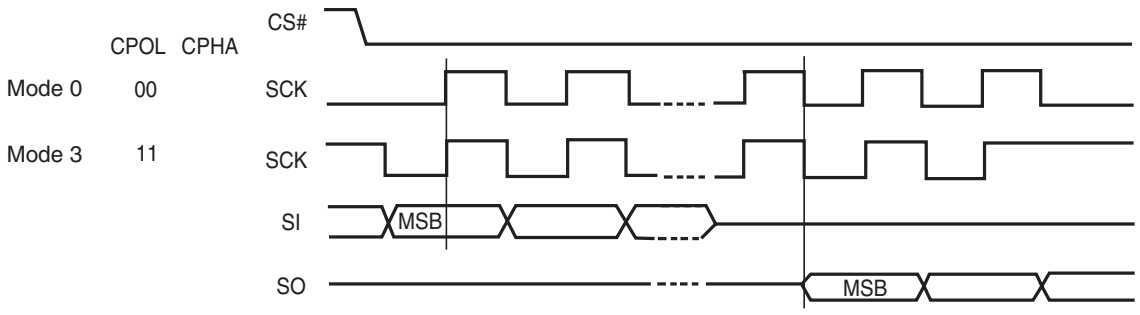
- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

Figure 6.1 Bus Master and Memory Devices on the SPI Bus



Note
The Write Protect (W#) and Hold (HOLD#) signals should be driven high (logic level 1) or low (logic level 0) as appropriate.

Figure 6.2 SPI Modes Supported



7. Device Operations

All Spansion SPI devices (S25FL-A) accept and output data in bytes (8 bits at a time).

7.1 Byte or Page Programming

Programming data requires two commands: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. The Page Program sequence accepts from 1 byte up to 256 consecutive bytes of data (which is the size of one page) to be programmed in one operation. Programming means that bits can either be left at 0, or programmed from 1 to 0. Changing bits from 0 to 1 requires an erase operation.

7.2 Sector Erase / Bulk Erase

The Sector Erase (SE) and Bulk Erase (BE) commands set all the bits in a sector or the entire memory array to 1. While bits can be individually programmed from a 1 to 0, erasing bits from 0 to 1 must be done on a sector-wide (SE) or array-wide (BE) level.

7.3 Monitoring Write Operations Using the Status Register

The host system can determine when a Write Status Register, program, or erase operation is complete by monitoring the Write in Progress (WIP) bit in the Status Register. The Read from Status Register command provides the state of the WIP bit.

7.4 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is high, the device is disabled, but may still be in the Active Power mode until all program, erase, and Write Status Register operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}. The Deep Power Down (DP) command provides additional data protection against inadvertent signals. After writing the DP command, the device ignores any further program or erase commands, and reduces its power consumption to I_{DP}.

7.5 Status Register

The Status Register contains the status and control bits that can be read or set by specific commands (Table 9.2, *S25FL032A Status Register* on page 18):

- **Write In Progress (WIP):** Indicates whether the device is performing a Write Status Register, program or erase operation.
- **Write Enable Latch (WEL):** Indicates the status of the internal Write Enable Latch.
- **Block Protect (BP2, BP1, BP0):** Non-volatile bits that define memory area to be software-protected against program and erase commands.
- **Status Register Write Disable (SRWD):** Places the device in the Hardware Protected mode when this bit is set to 1 and the W# input is driven low. In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits.

7.6 Data Protection Modes

Spansion SPI Flash memory devices provide the following data protection methods:

- **The Write Enable (WREN) command:** Must be written prior to any command that modifies data. The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit resets (disables writes) on *power-up* or after the device completes the following *commands*:
  - Page Program (PP)
  - Sector Erase (SE)
  - Bulk Erase (BE)

- Write Disable (WRDI)
- Write Status Register (WRSR)

- **Software Protected Mode (SPM):** The Block Protect (BP2, BP1, BP0) bits define the section of the memory array that can be read but not programmed or erased. Table 7.1 shows the sizes and address ranges of protected areas that are defined by Status Register bits BP2:BP0.
- **Hardware Protected Mode (HPM):** The Write Protect (W#) input and the Status Register Write Disable (SRWD) bit together provide write protection.
- **Clock Pulse Count:** The device verifies that all program, erase, and Write Status Register commands consist of a clock pulse count that is a multiple of eight before executing them.

Table 7.1 S25FL032A Protected Area Sizes

Status Register Block Protect Bits			Memory Array				Protected Portion of Total Memory Area
BP2	BP1	BP0	Protected Address Range	Protected Sectors	Unprotected Address Range	Unprotected Sectors	
0	0	0	None	(0)	000000h–3FFFFFh	SA63:SA0	0
0	0	1	3F0000h–3FFFFFh	(1) SA63	000000h–3EFFFFh	SA62:SA0	1/64
0	1	0	3E0000h–3FFFFFh	(2) SA63:SA62	000000h–3DFFFFh	SA61:SA0	1/32
0	1	1	3C0000h–3FFFFFh	(4) SA63:SA60	000000h–3BFFFFh	SA59:SA0	1/16
1	0	0	380000h–3FFFFFh	(8) SA63:SA56	000000h–37FFFFh	SA55:SA0	1/8
1	0	1	300000h–3FFFFFh	(16) SA63:SA48	000000h–2FFFFFh	SA47:SA0	1/4
1	1	0	200000h–3FFFFFh	(32) SA63:SA32	000000h–1FFFFFh	SA31:SA0	1/2
1	1	1	000000h–3FFFFFh	(64) SA63:SA0	None	None	All

7.7 Hold Mode (HOLD#)

The Hold input (HOLD#) stops any serial communication with the device, but does not terminate any Write Status Register, program or erase operation that is currently in progress.

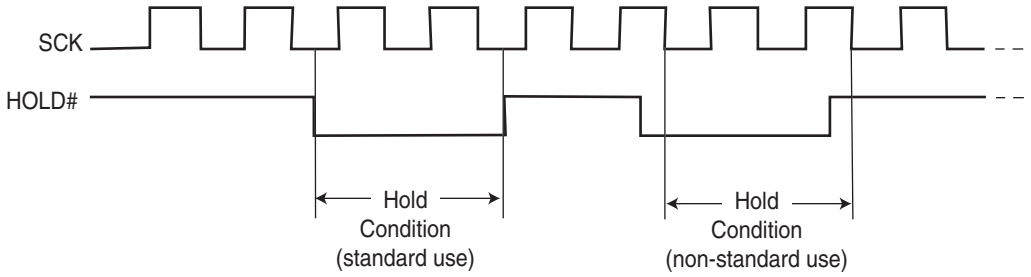
The Hold mode starts on the falling edge of HOLD# if SCK is also low (see Figure 7.1, on page 11, standard use). If the falling edge of HOLD# does not occur while SCK is low, the Hold mode begins after the next falling edge of SCK (non-standard use).

The Hold mode ends on the rising edge of HOLD# signal (standard use) if SCK is also low. If the rising edge of HOLD# does not occur while SCK is low, the Hold mode ends on the next falling edge of CLK (non-standard use) See Figure 7.1.

The SO output is high impedance, and the SI and SCK inputs are ignored (don't care) for the duration of the Hold mode.

CS# must remain low for the entire duration of the Hold mode to ensure that the device internal logic remains unchanged. If CS# goes high while the device is in the Hold mode, the internal logic is reset. To prevent the device from reverting to the Hold mode when device communication is resumed, HOLD# must be held high, followed by driving CS# low.

Figure 7.1 Hold Mode Operation



8. Sector Address Table

Table 8.1 shows the size of the memory array, sectors, and pages. The device uses *pages* to cache the program data before the data is programmed into the memory array. Each page or byte can be individually programmed (bits are changed from 1 to 0). The data is erased (bits are changed from 0 to 1) on a sector- or device-wide basis using the SE or BE commands. Table 8.2 shows the starting and ending address for each sector. The complete set of sectors comprises the memory array of the Flash device.

Table 8.1 S25FL032A Device Organization

Each Device has	Each Sector has	Each Page has	
4,194,304	65,536	256	bytes
16,384	256	—	pages
64	—	—	sectors

Table 8.2 S25FL032A Sector Address Table (Sheet 1 of 2)

Sector	Address Range	
SA63	3F0000h	3FFFFFh
SA62	3E0000h	3EFFFFh
SA61	3D0000h	3DFFFFh
SA60	3C0000h	3CFFFFh
SA59	3B0000h	3BFFFFh
SA58	3A0000h	3AFFFFh
SA57	390000h	39FFFFh
SA56	380000h	38FFFFh
SA55	370000h	37FFFFh
SA54	360000h	36FFFFh
SA53	350000h	35FFFFh
SA52	340000h	34FFFFh
SA51	330000h	33FFFFh
SA50	320000h	32FFFFh
SA49	310000h	31FFFFh
SA48	300000h	30FFFFh
SA47	2F0000h	2FFFFFh
SA46	2E0000h	2EFFFFh
SA45	2D0000h	2DFFFFh
SA44	2C0000h	2CFFFFh
SA43	2B0000h	2BFFFFh
SA42	2A0000h	2AFFFFh
SA41	290000h	29FFFFh
SA40	280000h	28FFFFh
SA39	270000h	27FFFFh
SA38	260000h	26FFFFh
SA37	250000h	25FFFFh
SA36	240000h	24FFFFh
SA35	230000h	23FFFFh
SA34	220000h	22FFFFh
SA33	210000h	21FFFFh
SA32	200000h	20FFFFh
SA31	1F0000h	1FFFFFh
SA30	1E0000h	1EFFFFh
SA29	1D0000h	1DFFFFh
SA28	1C0000h	1CFFFFh

Table 8.2 S25FL032A Sector Address Table (Sheet 2 of 2)

Sector	Address Range	
SA27	1B0000h	1BFFFFh
SA26	1A0000h	1AFFFFh
SA25	190000h	19FFFFh
SA24	180000h	18FFFFh
SA23	170000h	17FFFFh
SA22	160000h	16FFFFh
SA21	150000h	15FFFFh
SA20	140000h	14FFFFh
SA19	130000h	13FFFFh
SA18	120000h	12FFFFh
SA17	110000h	11FFFFh
SA16	100000h	10FFFFh
SA15	0F0000h	0FFFFFh
SA14	0E0000h	0EFFFFh
SA13	0D0000h	0DFFFFh
SA12	0C0000h	0CFFFFh
SA11	0B0000h	0BFFFFh
SA10	0A0000h	0AFFFFh
SA9	090000h	09FFFFh
SA8	080000h	08FFFFh
SA7	070000h	07FFFFh
SA6	060000h	06FFFFh
SA5	050000h	05FFFFh
SA4	040000h	04FFFFh
SA3	030000h	03FFFFh
SA2	020000h	02FFFFh
SA1	010000h	01FFFFh
SA0	000000h	00FFFFh

9. Command Definitions

The host system must shift all commands, addresses, and data in and out of the device, beginning with the most significant bit. On the first rising edge of SCK after CS# is driven low, the device accepts the one-byte command on SI (all commands are one byte long), most significant bit first. Each successive bit is latched on the rising edge of SCK. Table 9.4 on page 26 lists the complete set of commands.

Every command sequence begins with a one-byte command code. The command may be followed by address, data, both, or nothing, depending on the command. CS# must be driven high after the last bit of the command sequence has been written.

The Read Data Bytes (READ), Read Status Register (RDSR), Read Data Bytes at Higher Speed (FAST_READ) and Read Identification (RDID) command sequences are followed by a data output sequence on SO. CS# can be driven high after any bit of the sequence is output to terminate the operation.

The Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN), or Write Disable (WRDI) commands require that CS# be driven high at a byte boundary, otherwise the command is not executed. Since a byte is composed of eight bits, CS# must therefore be driven high when the number of clock pulses after CS# is driven low is an exact multiple of eight.

The device ignores any attempt to access the memory array during a Write Status Register, program, or erase operation, and continues the operation uninterrupted.

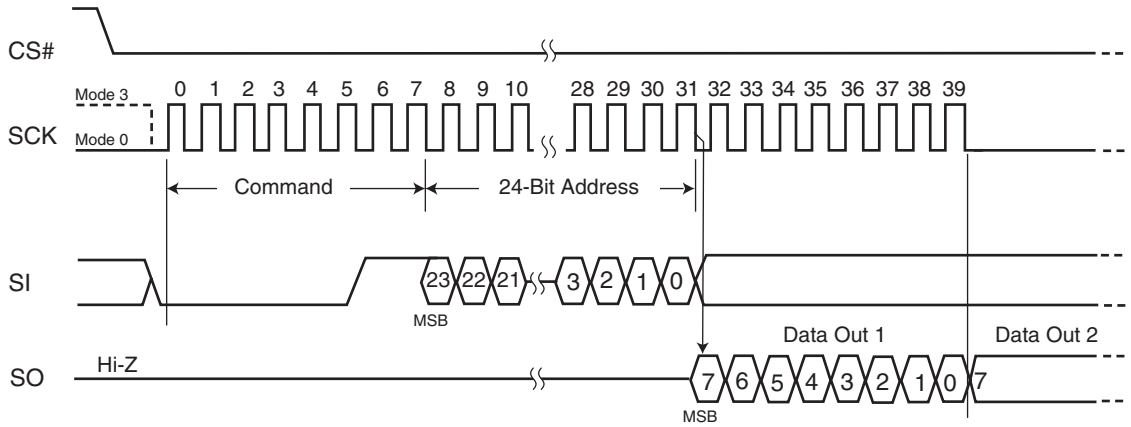
9.1 Read Data Bytes (READ)

The Read Data Bytes (READ) command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 33 MHz. The host system must first select the device by driving CS# low. The READ command is then written to SI, followed by a 3-byte address (A23-A0). Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK}, on the falling edge of SCK.

Figure 9.1 and Table 9.4 detail the READ command sequence. The first byte specified can be at any location. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The READ command is terminated by driving CS# high at any time during data output. The device rejects any READ command issued while it is executing a program, erase, or Write Status Register operation, and continues the operation uninterrupted.

Figure 9.1 Read Data Bytes (READ) Command Sequence



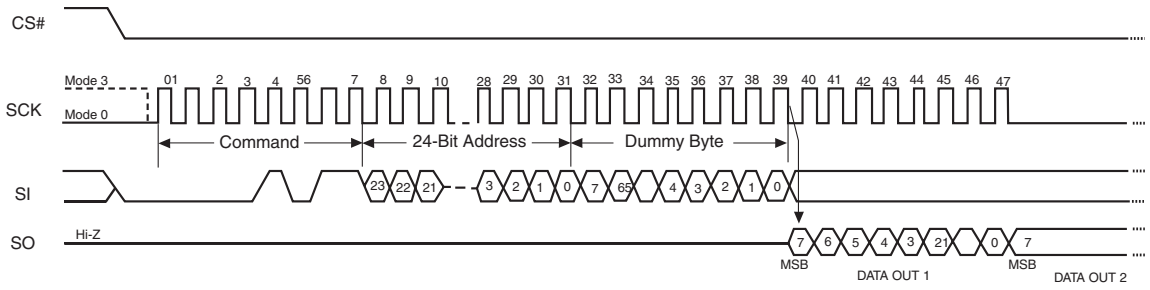
9.2 Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 50 MHz. The host system must first select the device by driving CS# low. The FAST_READ command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK}, on the falling edge of SCK.

The FAST_READ command sequence is shown in Figure 9.2 and Table 9.4. The first byte specified can be at any location. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single FAST_READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The FAST_READ command is terminated by driving CS# high at any time during data output. The device rejects any FAST_READ command issued while it is executing a program, erase, or Write Status Register operation, and continues the operation uninterrupted.

Figure 9.2 Read Data Bytes at Higher Speed (FAST_READ) Command Sequence



9.3 Read Identification (RDID)

The Read Identification (RDID) command outputs the one-byte manufacturer identification, followed by the two-byte device identification, to the host system.

JEDEC assigns the manufacturer identification byte; for Spansion devices it is 01h. The device manufacturer assigns the device identification: the first byte provides the memory type; the second byte indicates the memory capacity. See Table 9.1 or Table 9.4 for device ID data.

The host system must first select the device by driving CS# low. The RDID command is then written to SI, and each bit is latched on the rising edge of SCK. The 24-bit device identification data is output from the memory array on SO at a frequency f_{SCK}, on the falling edge of SCK.

The RDID command sequence is shown in Figure 9.3 and Table 9.4.

Driving CS# high after the device identification data has been read at least once terminates the READ_ID command. Driving CS# high at any time during data output also terminates the RDID operation.

The device rejects any RDID command issued while it is executing a program, erase, or Write Status Register operation, and continues the operation uninterrupted.

Figure 9.3 Read Identification (RDID) Command Sequence and Data-Out Sequence

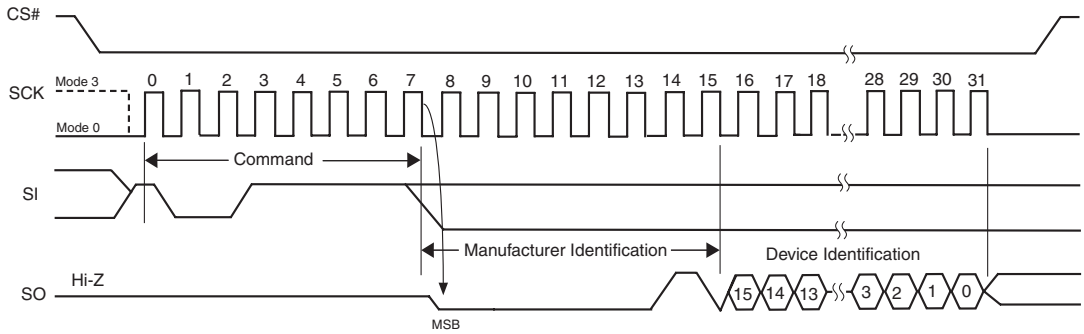


Table 9.1 Read Identification (RDID) Data-Out Sequence

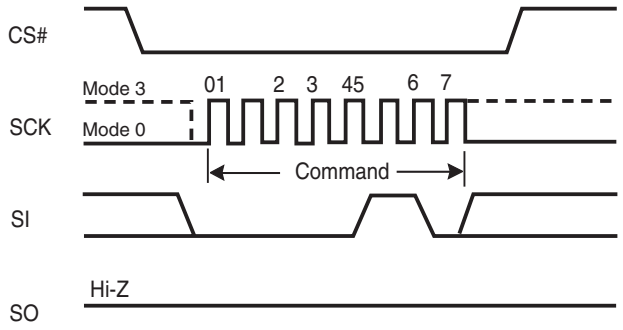
Manufacturer Identification	Device Identification	
	Memory Type	Memory Capacity
01h	02h	15h

9.4 Write Enable (WREN)

The Write Enable (WREN) command (see Figure 9.4) sets the Write Enable Latch (WEL) bit to a 1, which enables the device to accept a Write Status Register, program, or erase command. The WEL bit must be set prior to every Page Program (PP), Erase (SE or BE) and Write Status Register (WRSR) command.

The host system must first drive CS# low, write the WREN command, and then drive CS# high.

Figure 9.4 Write Enable (WREN) Command Sequence



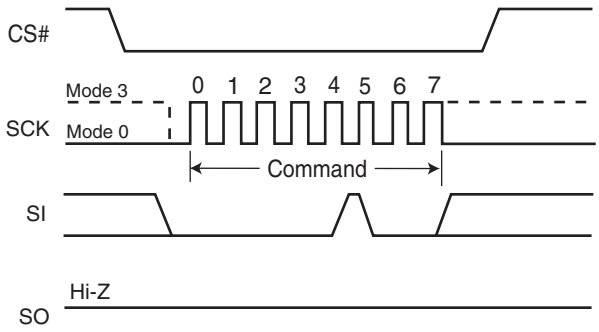
9.5 Write Disable (WRDI)

The Write Disable (WRDI) command (see Figure 9.5) resets the Write Enable Latch (WEL) bit to a 0, which disables the device from accepting a Write Status Register, program, or erase command. The host system must first drive CS# low, write the WRDI command, and then drive CS# high.

Any of following conditions resets the WEL bit:

- Power-up
- Write Disable (WRDI) command completion
- Write Status Register (WRSR) command completion
- Page Program (PP) command completion
- Sector Erase (SE) command completion
- Bulk Erase (BE) command completion

Figure 9.5 Write Disable (WRDI) Command Sequence



9.6 Read Status Register (RDSR)

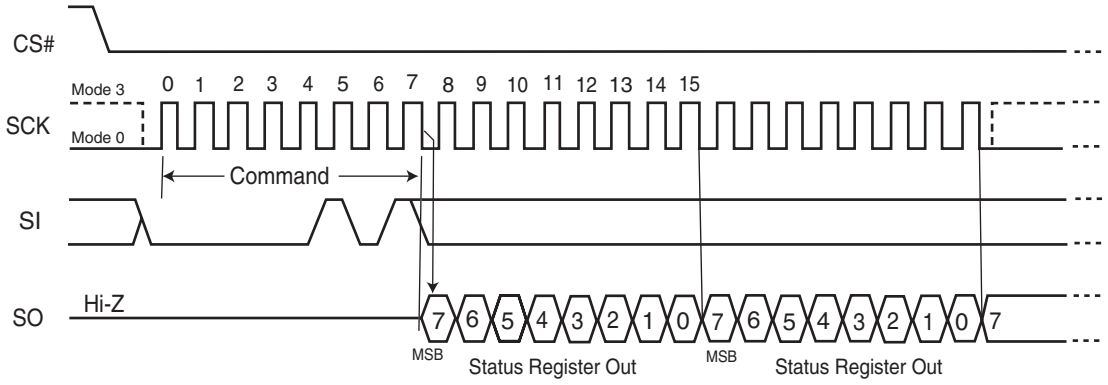
The Read Status Register (RDSR) command outputs the state of the Status Register bits. Table 9.2 shows the status register bits and their functions.

The RDSR command may be written at any time, even while a program, erase, or Write Status Register operation is in progress. The host system should check the Write In Progress (WIP) bit before sending a new command to the device if an operation is already in progress. Figure 9.6 shows the RDSR command sequence, which also shows that it is possible to read the Status Register continuously until CS# is driven high.

Table 9.2 S25FL032A Status Register

Bit	Status Register Bit	Bit Function	Description
7	SRWD	Status Register Write Disable	1 = Protects when W# is low 0 = No protection, even when W# is low
6	—	—	Not used
5	—	—	Not used
4B	P2	Block Protect	000–111 = Protects upper half of address range in 5 sizes. See Table 7.1.
3B	P1		
2B	P0		
1	WEL	Write Enable Latch	1 = Device accepts Write Status Register, program, or erase commands 0 = Ignores Write Status Register, program, or erase commands
0	WIP	Write in Progress	1 = Device Busy. A Write Status Register, program, or erase operation is in progress 0 = Ready. Device is in standby mode and can accept commands.

Figure 9.6 Read Status Register (RDSR) Command Sequence



The following describes the status and control bits of the Status Register.

Write In Progress (WIP) bit: Indicates whether the device is busy performing a Write Status Register, program, or erase operation. This bit is read-only, and is controlled internally by the device. If WIP is 1, one of these operations is in progress; if WIP is 0, no such operation is in progress.

Write Enable Latch (WEL) bit: Determines whether the device will accept and execute a Write Status Register, program, or erase command. When set to 1, the device accepts these commands; when set to 0, the device rejects the commands. This bit is set to 1 by writing the WREN command, and set to 0 by the WRDI command, and is also automatically reset to 0 after the completion of a Write Status Register, program, or erase operation. WEL cannot be directly set by the WRSR command.

Block Protect (BP2, BP1, BP0) bits: Define the portion of the memory area that will be protected against any changes to the stored data. The Write Status Register (WRSR) command controls these bits, which are non-volatile. When one or more of these bits is set to 1, the corresponding memory area (see Table 7.1 on page 11) is protected against Page Program (PP) and Sector Erase (SE) commands. If the Hardware Protected mode is enabled, BP2:BP0 cannot be changed. The Bulk Erase (BE) command is executed only if all Block Protect (BP2, BP1, BP0) bits are 0.

Status Register Write Disable (SRWD) bit: Provides data protection when used together with the Write Protect (W#) signal. When SRWD is set to 1 and W# is driven low, the device enters the Hardware Protected mode. The non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits and the device ignores any Write Status Register (WRSR) command.

9.7 Write Status Register (WRSR)

The Write Status Register (WRSR) command changes the bits in the Status Register. A Write Enable (WREN) command, which itself sets the Write Enable Latch (WEL) in the Status Register, is required prior to writing the WRSR command. Table 9.2, *S25FL032A Status Register* on page 18 shows the status register bits and their functions.

The host system must drive CS# low, write the WRSR command, and the appropriate data byte on SI (Figure 9.7).

The WRSR command cannot change the state of the Write Enable Latch (bit 1). The WREN command must be used for that purpose. Bit 0 is a status bit controlled internally by the Flash device. Bits 6 and 5 are always read as 0 and have no user significance.

The WRSR command also controls the value of the Status Register Write Disable (SRWD) bit. The SRWD bit and W# together place the device in the Hardware Protected Mode (HPM). The device ignores all WRSR commands once it enters the Hardware Protected Mode (HPM). Table 9.3 shows that W# must be driven low and the SRWD bit must be 1 for this to occur.

Figure 9.7 Write Status Register (WRSR) Command Sequence

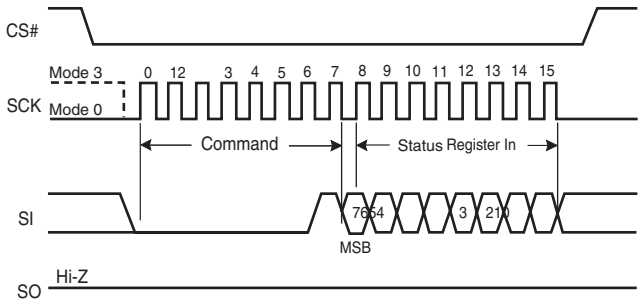


Table 9.3 Protection Modes

W# Signal	SRWD Bit	Mode	Write Protection of the Status Register	Protected Area (See Note)	Unprotected Area (See Note)
11		Software Protected (SPM)	Status Register is writable (if the WREN command has set the WEL bit). The values in the SRWD, BP2, BP1 and BP0 bits can be changed.	Protected against program and erase commands	Ready to accept Page Program and Sector Erase commands
1	0				
0	0				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected. The values in the SRWD, BP2, BP1 and BP0 bits cannot be changed.	Protected against program and erase commands	Ready to accept Page Program and Sector Erase commands

Note
As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in Table 7.1 on page 11.

Table 9.3 shows that neither W# or SRWD bit by themselves can enable HPM. The device can enter HPM either by setting the SRWD bit after driving W# low, or by driving W# low after setting the SRWD bit. However, the device disables HPM only when W# is driven high.

Note that HPM only protects against changes to the status register. Since BP2:BP0 cannot be changed in HPM, the size of the protected area of the memory array cannot be changed. Note that HPM provides no protection to the memory array area outside that specified by BP2:BP0 (Software Protected Mode, or SPM).

If W# is permanently tied high, HPM can never be activated, and only the SPM (BP2:BP0 bits of the Status Register) can be used.

9.8 Page Program (PP)

The Page Program (PP) command changes specified bytes in the memory array (from 1 to 0 only). A WREN command is required prior to writing the PP command.

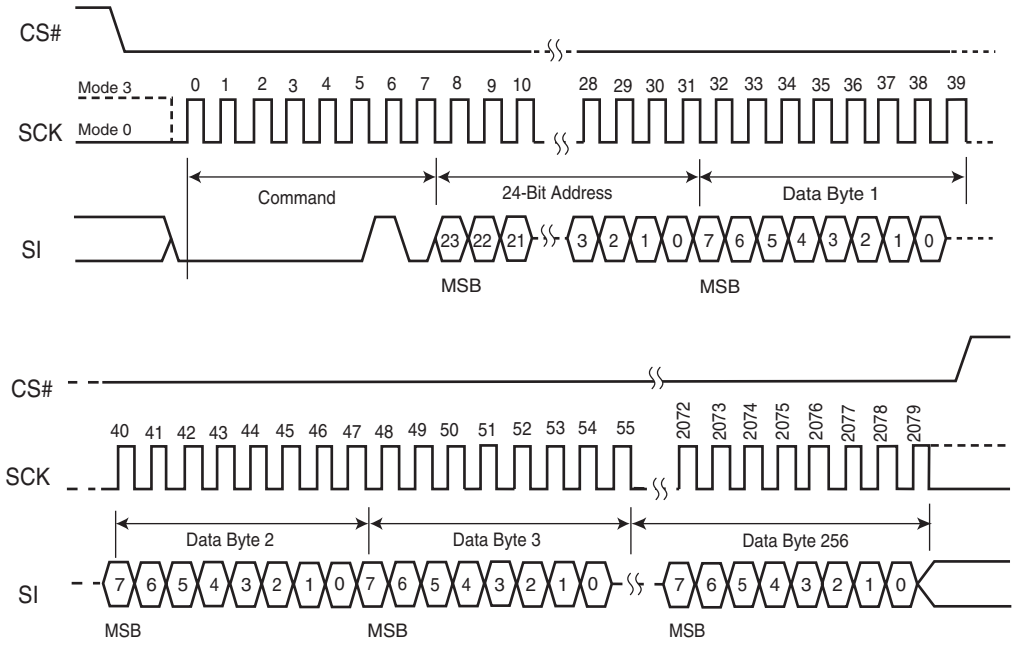
The host system must drive CS# low, and then write the PP command, three address bytes, and at least one data byte on SI. CS# must be driven low for the entire duration of the PP sequence. The command sequence is shown in Figure 9.8 and Table 9.4.

The device programs only the last 256 data bytes sent to the device. If the number of data bytes exceeds this limit, the bytes sent before the last 256 bytes are discarded, and the device begins programming the last 256 bytes sent at the starting address of the specified page. This may result in data being programmed into different addresses within the same page than expected. If fewer than 256 data bytes are sent to device, they are correctly programmed at the requested addresses.

The host system must drive CS# high after the device has latched the 8th bit of the data byte, otherwise the device does not execute the PP command. The PP operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{PP}. The Status Register may be read to check the value of the Write In Progress (WIP) bit while the PP operation is in progress. The WIP bit is 1 during the PP operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

The device does not execute a Page Program (PP) command that specifies a page that is protected by the Block Protect bits (BP2:BP0) (see Table 7.1 on page 11).

Figure 9.8 Page Program (PP) Command Sequence



9.9 Sector Erase (SE)

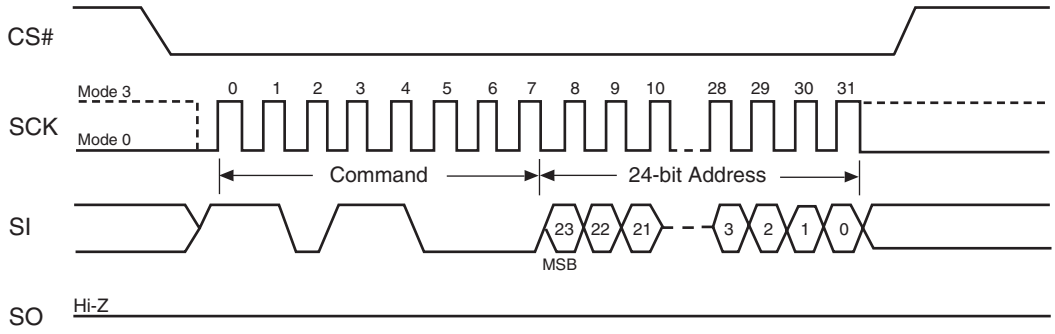
The Sector Erase (SE) command sets all bits at all addresses within a specified sector to a logic 1. A WREN command is required prior to writing the PP command.

The host system must drive CS# low, and then write the SE command plus three address bytes on SI. Any address within the sector (see Table 7.1 on page 11) is a valid address for the SE command. CS# must be driven low for the entire duration of the SE sequence. The command sequence is shown in Figure 9.9 and Table 9.4.

The host system must drive CS# high after the device has latched the 8th bit of the SE command, otherwise the device does not execute the command. The SE operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{SE}. The Status Register may be read to check the value of the Write In Progress (WIP) bit while the SE operation is in progress. The WIP bit is 1 during the SE operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

The device does not execute an SE command that specifies a sector that is protected by the Block Protect bits (BP2:BP0) (see Table 7.1 on page 11).

Figure 9.9 Sector Erase (SE) Command Sequence



9.10 Bulk Erase (BE)

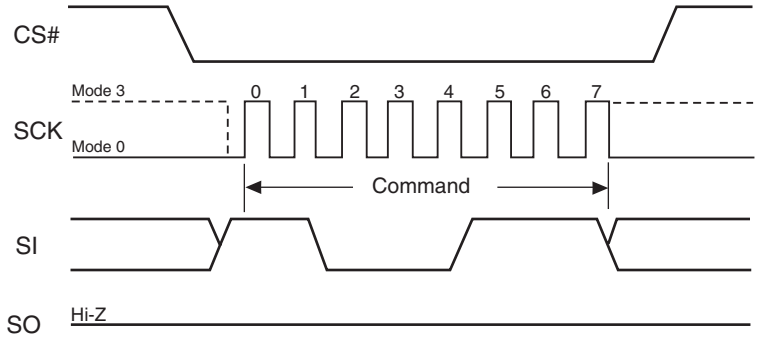
The Bulk Erase (BE) command sets all the bits within the entire memory array to logic 1s. A WREN command is required prior to writing the PP command.

The host system must drive CS# low, and then write the BE command on SI. CS# must be driven low for the entire duration of the BE sequence. The command sequence is shown in Figure 9.10 and Table 9.4.

The host system must drive CS# high after the device has latched the 8th bit of the CE command, otherwise the device does not execute the command. The BE operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{BE}. The Status Register may be read to check the value of the Write In Progress (WIP) bit while the BE operation is in progress. The WIP bit is 1 during the BE operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

The device only executes a BE command if all Block Protect bits (BP2:BP0) are 0 (see Table 7.1 on page 11). Otherwise, the device ignores the command.

Figure 9.10 Bulk Erase (BE) Command Sequence



9.11 Deep Power Down (DP)

The Deep Power Down (DP) command provides the lowest power consumption mode of the device. It is intended for periods when the device is not in active use, and ignores all commands except for the Release from Deep Power Down (RES) command. *The DP mode therefore provides the maximum data protection against unintended write operations.* The standard standby mode, which the device goes into automatically when CS# is high (and all operations in progress are complete), should generally be used for the lowest power consumption when the quickest return to device activity is required.

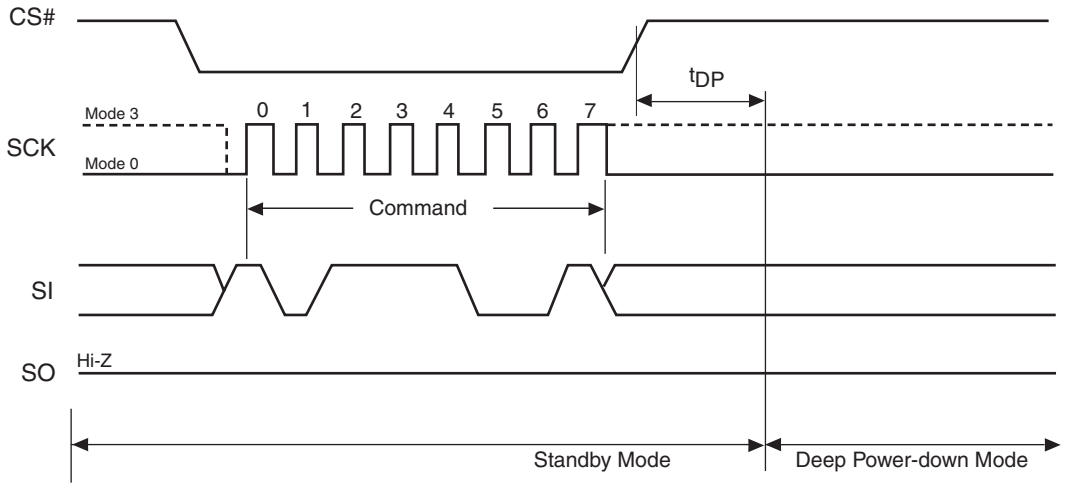
The host system must drive CS# low, and then write the DP command on SI. CS# must be driven low for the entire duration of the DP sequence. The command sequence is shown in Figure 9.11 and Table 9.4.

The host system must drive CS# high after the device has latched the 8th bit of the DP command, otherwise the device does not execute the command. After a delay of t_{DP}, the device enters the DP mode and current reduces from I_{SB} to I_{DP} (see Table 14.1 on page 28).

Once the device has entered the DP mode, all commands are ignored except the RES command (which releases the device from the DP mode). The RES command also provides the Electronic Signature of the device to be output on SO, if desired (see sections 9.12 and 9.12.1).

DP mode automatically terminates when power is removed, and the device always powers up in the standard standby mode. The device rejects any DP command issued while it is executing a program, erase, or Write Status Register operation, and continues the operation uninterrupted.

Figure 9.11 Deep Power Down (DP) Command Sequence



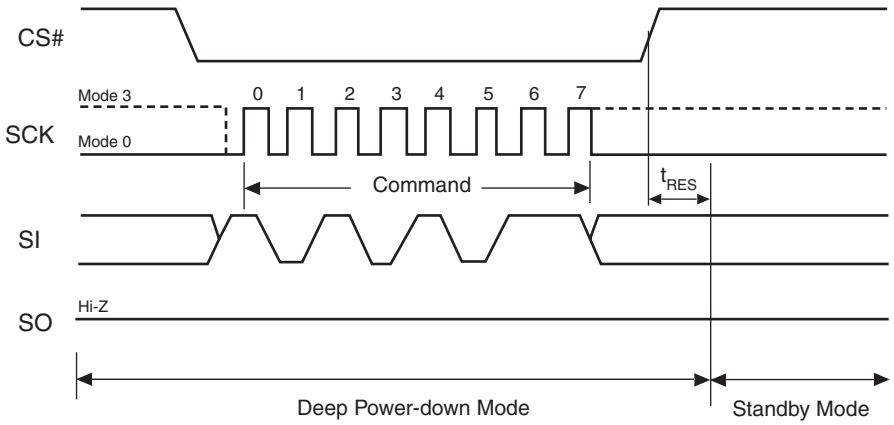
9.12 Release from Deep Power Down (RES)

The device requires the Release from Deep Power Down (RES) command to exit the Deep Power Down mode. When the device is in the Deep Power Down mode, all commands except RES are ignored.

The host system must drive CS# low and write the RES command to SI. CS# must be driven low for the entire duration of the sequence. The command sequence is shown in Figure 9.12 and Table 9.4.

The host system must drive CS# high $t_{RES(max)}$ after the 8-bit RES command byte. The device transitions from DP mode to the standby mode after a delay of t_{RES} (see Table 16.1 on page 30). In the standby mode, the device can execute any read or write command.

Figure 9.12 Release from Deep Power Down (RES) Command Sequence



9.12.1 Release from Deep Power Down and Read Electronic Signature (RES)

The device features an 8-bit Electronic Signature, which can be read using the RES command. See Figure 9.13 and Table 9.4 for the command sequence and signature value. The Electronic Signature is not to be confused with the identification data obtained using the RDID command. The device offers the Electronic Signature so that it can be used with previous devices that offered it; however, the Electronic Signature should not be used for new designs, which should read the RDID data instead.

After the host system drives CS# low, it must write the RES command followed by 3 dummy bytes to SI (each bit is latched on SI during the rising edge of SCK). The Electronic Signature is then output on SO; each bit is shifted out on the falling edge of SCK. The RES operation is terminated by driving CS# high after the Electronic Signature is read at least once. Additional clock cycles on SCK with CS# low cause the device to output the Electronic Signature repeatedly.

When CS# is driven high, the device transitions from DP mode to the standby mode after a delay of t_{RES}, as previously described. The RES command always provides access to the Electronic Signature of the device and can be applied even if DP mode has not been entered.

Any RES command issued while an erase, program, or WRSR operation is in progress not executed, and the operation continues uninterrupted.

Figure 9.13 Release from Deep Power Down and Read Electronic Signature (RES) Command Sequence

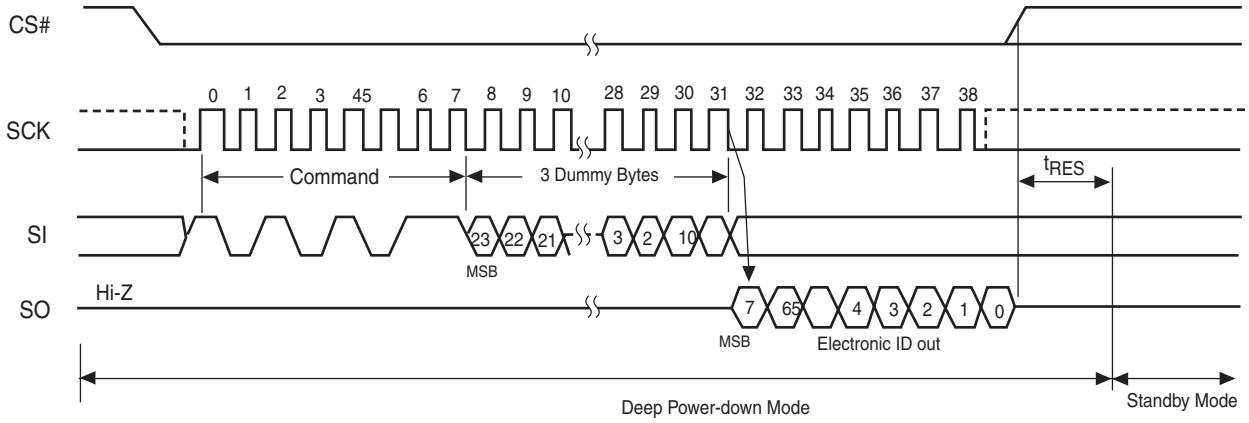


Table 9.4 Command Definitions

Operation	Command	Description	One-Byte Command Code	Address Bytes	Dummy Byte	Data Bytes
Read	READ	Read Data Bytes	03H (0000 0011)	3	0	1 to ∞
	FAST_READ	Read Data Bytes at Higher Speed	0BH (0000 1011)	3	1	1 to ∞
	RDID	Read Identification (Note 1)	9FH (1001 1111)	0	0	1 to 3
Write Control	WREN	Write Enable	06H (0000 0110)	0	0	0
	WRDI	Write Disable	04H (0000 0100)	0	0	0
Erase	SE	Sector Erase	D8H (1101 1000)	3	0	0
	BE	Bulk (Chip) Erase	C7H (1100 0111)	0	0	0
Program	PP	Page Program	02H (0000 0010)	3	0	1 to 256
Status Register	RDSR	Read from Status Register	05H (0000 0101)	0	0	1 to ∞
	WRSR	Write to Status Register	01H (0000 0001)	0	0	1
Power Saving	DP	Deep Power Down	B9H (1011 1001)	0	0	0
	RES	Release from Deep Power Down	ABH (1010 1011)	0	0	0
		Release from Deep Power Down and Read Electronic Signature (Note 2)	ABH (1010 1011)	0	3	1 to ∞

Notes

1. *The S25FL032A has a manufacturer ID of 01h, and a device ID consisting of the memory type (02h) and the memory capacity (15h).*
2. *The S25FL032A has an Electronic Signature ID of 15h.*

10. Power-up and Power-down

During power-up and power-down, certain conditions must be observed. CS# must follow the voltage applied on V_{CC}, and must not be driven low to select the device until V_{CC} reaches the allowable values as follows (see Figure 10.1 and Table 10.1):

- At power-up, V_{CC} (min) plus a period of t_{PU}
- At power-down, V_{SS}

A pull-up resistor on Chip Select (CS#) typically meets proper power-up and power-down requirements.

No Write Status Register, program, or erase command should be sent to the device until V_{CC} rises to the V_{CC} min, plus a delay of t_{PU}. At power-up, the device is in standby mode (not Deep Power Down mode) and the WEL bit is reset (0).

Each device in the host system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins (this capacitor is generally of the order of 0.1 µF), as a precaution to stabilizing the V_{CC} feed.

When V_{CC} drops from the operating voltage to below the minimum V_{CC} threshold at power-down, all operations are disabled and the device does not respond to any commands. Note that data corruption may result if a power-down occurs while a Write Register, program, or erase operation is in progress.

Figure 10.1 Power-Up Timing Diagram

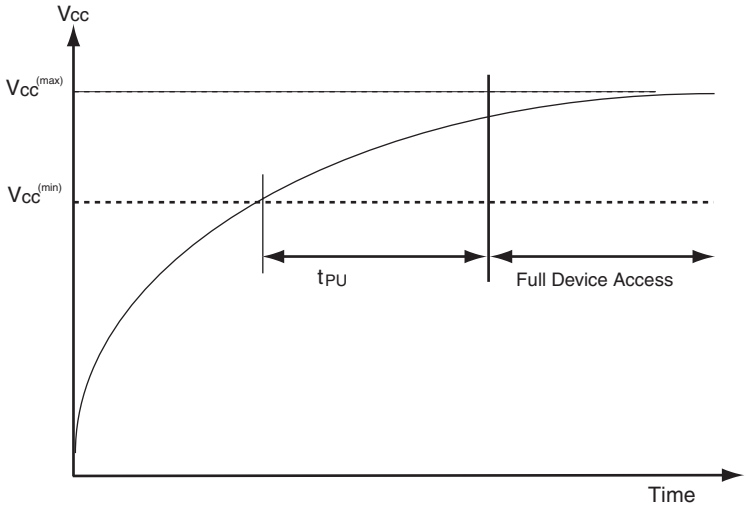


Table 10.1 Power-Up Timing Characteristics

Symbol	Parameter	Min	Max	Unit
$V_{CC(min)}$	V_{CC} (minimum)	2.7		V
t_{PU}	V_{CC} (min) to device operation	10		ms

11. Initial Delivery State

The device is delivered with all bits set to 1 (each byte contains FFh) upon initial factory shipment. The Status Register contains 00h (all Status Register bits are 0).

12. Absolute Maximum Ratings

Do not stress the device beyond the ratings listed in this section, or serious, permanent damage to the device may result. These are stress ratings only and device operation at these or any other conditions beyond those indicated in this section and in the Operating Ranges section of this document is not implied. Device operation for extended periods at the limits listed in this section may affect device reliability.

Table 12.1 Absolute Maximum Ratings

Description	Rating
Ambient Storage Temperature	–65°C to +150°C
Voltage with Respect to Ground: All Inputs and I/Os	–0.3 V to 4.5 V

13. Operating Ranges

Table 13.1 Operating Ranges

Description		Rating
Ambient Operating Temperature (T_A)	Commerical	0°C to +70°C
	Industrial	–40°C to +85°C
Positive Power Supply	Voltage Range	2.7 V to 3.6 V

Note
Operating ranges define those limits between which functionality of the device is guaranteed.

14. DC Characteristics

This section summarizes the DC Characteristics of the device. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in Table 15.1 on page 29, when relying on the quoted parameters.

Table 14.1 DC Characteristics (CMOS Compatible)

Parameter	Description	Test Conditions (See Note)		Min	Typ.	Max	Unit
V_{CC}	Supply Voltage			2.7	3	3.6	V
I_{CC1}	Active Read Current	SCK = 0.1 V_{CC}/0.9V_{CC}	33 MHz			12	mA
		SCK = 0.1 V_{CC}/0.9V_{CC}	V_{CC} = 3.0V 50 MHz			19	mA
I_{CC2}	Active Page Program Current	CS# = V_{CC}			19.5	28	mA
I_{CC3}	Active WRSR Current	CS# = V_{CC}				24	mA
I_{CC4}	Active Sector Erase Current	CS# = V_{CC}				24	mA
I_{CC5}	Active Bulk Erase Current	CS# = V_{CC}				24	mA
I_{SB}	Standby Current	V_{CC} = 3.0 V CS# = V_{CC}			20	50	µA
I_{DP}	Deep Power Down Current	V_{CC} = 3.0 V CS# = V_{CC}			1.5	5	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}				1µ	A
I_{LO}	Output Leakage Current	V_{IN} = GND to V_{CC}				1µ	A
V_{IL}	Input Low Voltage			–0.3		0.3 V_{CC}	V
V_{IH}	Input High Voltage			0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = $V_{CC\ min}$ 0.				4	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA		V_{CC} – 0.2			V

Note
Typical values are at T_A = 25° C and 3.0 V.

15. Test Conditions

Figure 15.1 AC Measurements I/O Waveform

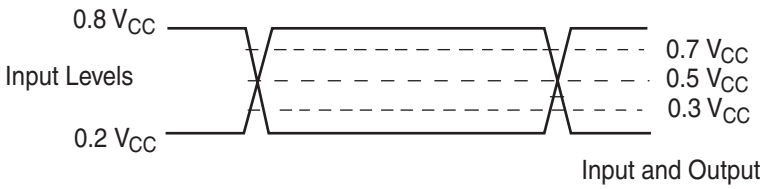


Table 15.1 Test Specifications

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltage	0.2 V_{CC} to 0.8 V_{CC}		V
	Input Timing Reference Voltage	0.3 V_{CC} to 0.7 V_{CC}		V
	Output Timing Reference Voltage	0.5 V_{CC}		V

16. AC Characteristics

Table 16.1 AC Characteristics

Symbol (Notes)	Parameter	Min	Typ (Notes)	Max (Notes)	Unit
F_{SCK}	SCK Clock Frequency READ command	D.C.		33	MHz
F_{SCK}	SCK Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.		50	MHz
t_{CRT}	Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CFT}	Clock Fall Time (Slew Rate)	0.1			V/ns
t_{WH}	SCK High Time	9n			s
t_{WL}	SCK Low Time	9n			s
t_{CS}	CS# High Time	100			ns
t_{CSS} (3)	CS# Setup Time	5n			s
t_{CSH} (3)C	S# HOLD Time	5n			s
t_{HD} (3)	HOLD# Setup Time (relative to SCK)	5			ns
t_{CD} (3)	HOLD# Hold Time (relative to SCK)	5			ns
t_{HC}	HOLD# Setup Time (relative to SCK)	5			ns
t_{CH}	HOLD# Hold Time (relative to SCK)	5			ns
t_{V}	Output Valid	01		0	ns
t_{HO}	Output Hold Time	0n			s
$t_{HD:DAT}$	Data in Hold Time	5n			s
$t_{SU:DAT}$	Data in Setup Time	5			ns
t_{R}	Input Rise Time			5n	s
t_{F}	Input Fall Time			5n	s
t_{LZ} (3)	HOLD# to Output Low Z			10	ns
t_{HZ} (3)	HOLD# to Output High Z			10	ns
t_{DIS} (3)	Output Disable Time			10	ns
t_{WPS} (3)	Write Protect Setup Time	15			ns
t_{WPH} (3)	Write Protect Hold Time	15			ns
t_{W}	Write Status Register Time		67	150	ms
t_{DP}	CS# High to Deep Power Down Mode			3	µs
t_{RES}	Release DP Mode			30	µs
t_{PP}	Page Programming Time		1.5 (1)3	(2)m	s
t_{SE}	Sector Erase Time		0.5 (1)3	(2)s	ec
t_{BE}	Bulk Erase Time		25 (1)1	92 (2)s	ec

Notes

1. *Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0V; 10,000 cycles; checkerboard data pattern*
2. *Under worst-case conditions of 90°C; V_{CC} = 2.7V; 100,000 cycles*
3. *Not 100% tested*

Figure 16.1 SPI Mode 0 (0,0) Input Timing

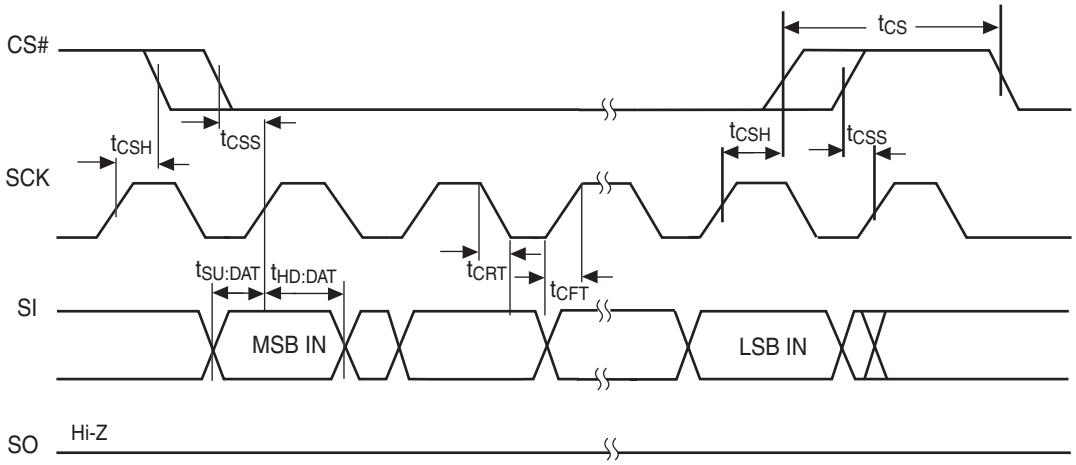


Figure 16.2 SPI Mode 0 (0,0) Output Timing

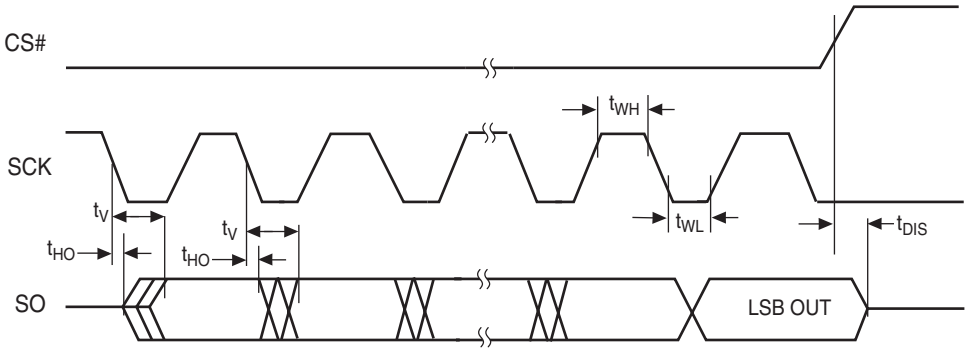


Figure 16.3 HOLD# Timing

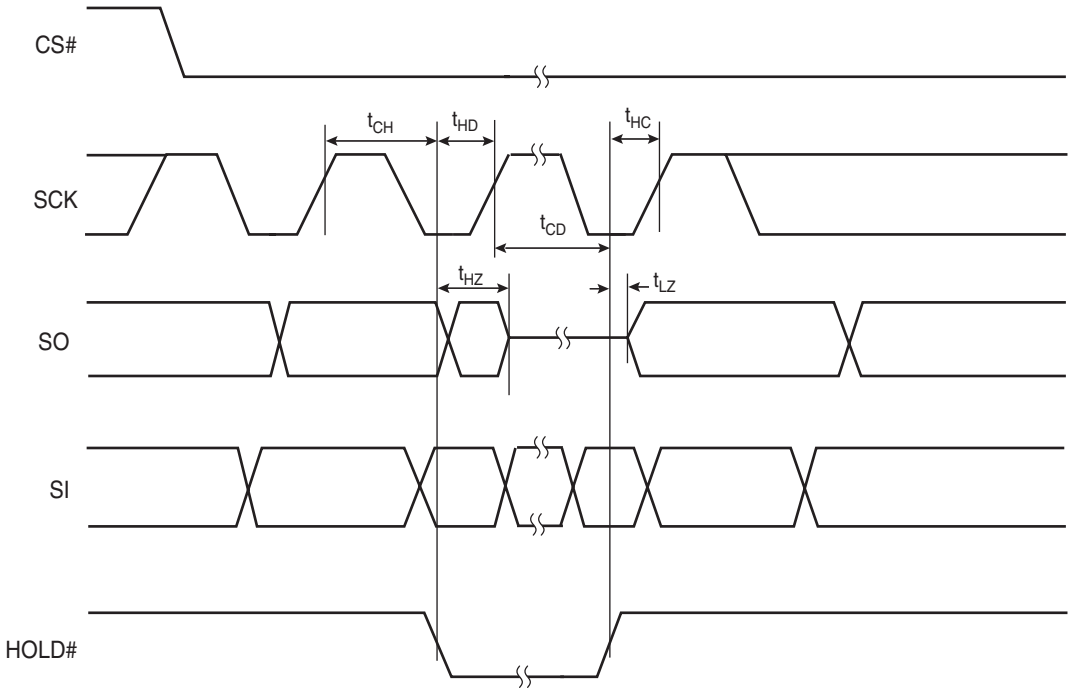
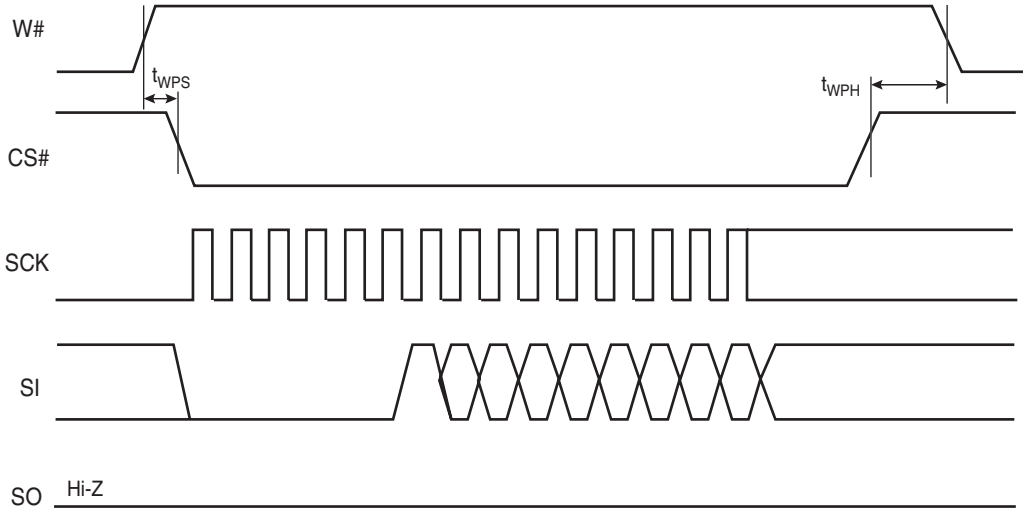
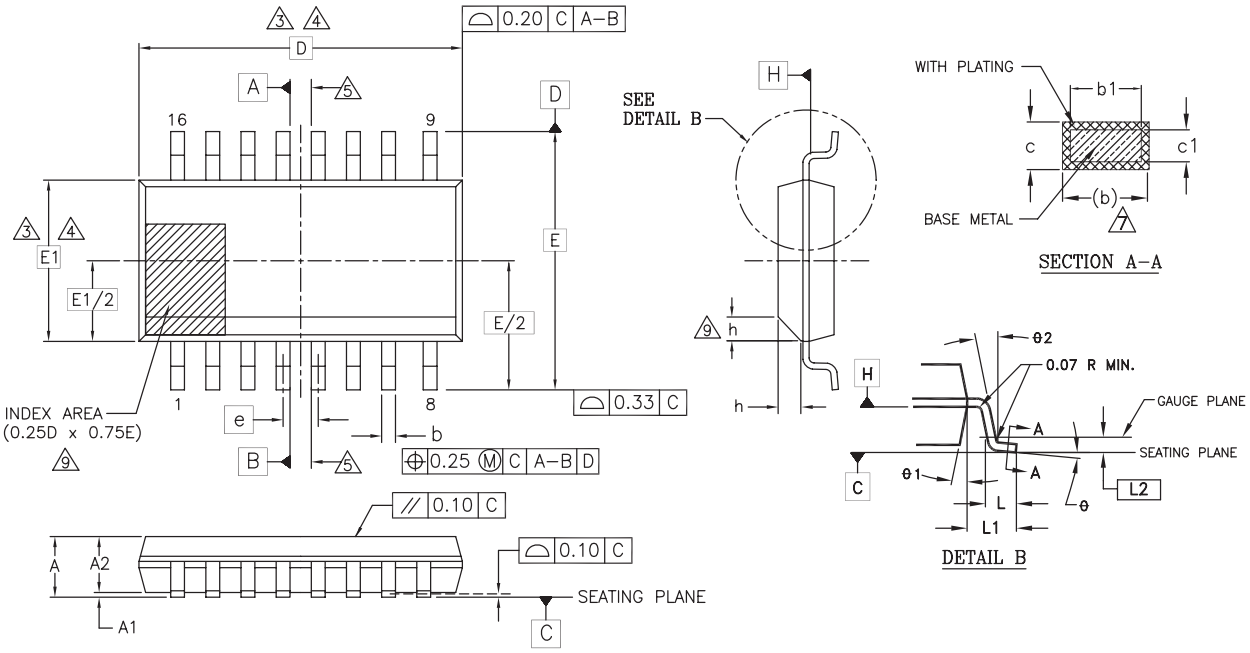


Figure 16.4 Write Protect Setup and Hold Timing during WRSR when SRWD=1



17. Physical Dimensions

17.1 SO3 016—16-pin Wide Plastic Small Outline Package (300-mil Body Width)



PACKAGE	SO3 016 (inches)		SO3 016 (mm)	
JEDEC	MS-013(D)AA		MS-013(D)AA	
SYMBOL	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.081	0.104	2.05	2.55
b	0.012	0.020	0.31	0.51
b1	0.011	0.019	0.27	0.48
c	0.008	0.013	0.20	0.33
c1	0.008	0.012	0.20	0.30
D	0.406 BSC		10.30 BSC	
E	0.406 BSC		10.30 BSC	
E1	0.295 BSC		7.50 BSC	
e	.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
L1	.055 REF		1.40 REF	
L2	.010 BSC		0.25 BSC	
N	16		16	
h	0.10	0.30	0.25	0.75
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0°		0°	

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

3601 \ 16-038.03 \ 8.31.6

18. Revision History

Section	Description
Revision A (August 10, 2005)	
Global	Initial release.
Revision B0 (April 16, 2006)	
Global	Changed document status from Advance Information to Preliminary. Changed title from family of devices to specific device.
Revision B1 (June 29, 2006)	
DC Characteristics	Changed typical and maximum specifications for I_{CC2}.
Revision C0 (September 1, 2006)	
Global	Rewrote entire document for better flow and clarity. No specifications were changed.

Colophon

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