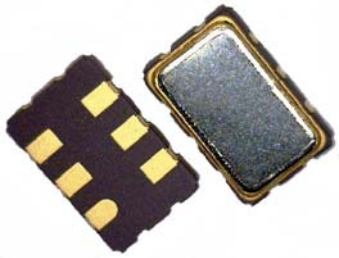
Differential LVPECL Crystal Clock Oscillators
HPK5361 Series 200 fsec Jitter +2.5V +3.3V "K" Family

MERCURY
Since 1973

- Femto second integrated phase jitter (200 fs typical, 12 KHz to 20 MHz)
- Superior phase noise (-138 dBc/Hz at 10 KHz and -144 dBc/Hz at 100 KHz offset).
- High performance with surprisingly low price.
- 2.5V or 3.3V supply voltage.

RoHS Compliant Product by Mercury



General Specifications

Product Series	HPK5361; "K" family characteristics. Tri-State on pad 1							
Frequency Range	40 MHz ~ 200 MHz.							
Output Logic	Differential PECL square wave							
Frequency Stability vs Operating Temperature Range	Stability Code	Commercial " C ":: -10°C to +70°C	Industrial " I ": -40°C to +85°C					
	±25 ppm	A	D					
	±50 ppm	B	E					
	±100 ppm	C	F					
	Custom ±xx ppm	Cxx	Ixx					
	If custom, use "temperature range code + desired stability in ppm" for the stability code. Example: "C20" (±20 ppm over -10 to +70°C).							
Supply Voltage V_{CC}	+2.5 V ± 5 % (Voltage code is "25"); or +3.3 V ± 5 % (Voltage code is "3")							
Output Voltage HIGH "1", V_{OH}	V_{DD}-1.025 V min.; V_{DD}-0.95 V typical; V_{DD}-0.88 V max. Condition: 50 ohms to V_{DD}-2V							
Output Voltage LOW "0", V_{OL}	V_{DD}-1.810 V min.; V_{DD}-1.70 V typical; V_{DD}-1.62 V max. Condition: 50 ohms to V_{DD}-2V							
Output Swing	595 mV min; 750 mV typical; 930 mV max.							
Current Consumption	35 mA typical; 50 mA max.							
Load	50 ohms into V_{CC}-2V or Thevenin equivalent (terminating resistors required on all outputs).							
Rise Time (Tr)	0.3 n sec. typ; 0.5 n sec. max. 20%→80% of waveform							
Fall Time (Tf)	0.3 n sec. typ; 0.5 n sec. max. 80%→20% of waveform							
Duty Cycle	50% ± 5% max. measured at 50% waveform							
Tri-state Function on pad No. 1	If no connection or V_{DD}*70% min is applied: Output. Internal pull-up Oscillation disable time is 0.2 u sec max.							
	If V_{DD}*30% max is applied: High impedance. Current consumption is 10 uA typical Oscillation enable time is 2 m sec. max.							
Phase Jitter (RMS)	200 fs typical (12 KHz to 20 MHz integrated)							
SSB Phase Noise (dBc/Hz). Typical	Offset	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
	125 MHz	-50	-82	-116	-138	-144	-149	-155
Start-up Time	3 ms typical; 10 m sec. max.							
Aging	±3 ppm / year max.							
Packaging	180 mm reel; 16 mm tape, 7.8 mm pitch. 1000 pcs per reel.							

(1)Inclusive of 25°C tolerance, operating temperature range, ±10% input voltage variation, load change, aging at +25°C, shock and vibration

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Absolute Maximum Rating Permanent damage may be created if operate beyond limits specified Ta=25°C, Vss=0V

Parameters	Rating	
	Min.	Max.
Supply Voltage	Vss-0.5V	5.0V
Input Voltage	Vss-0.5V	V_{DD}+0.5V
Output Voltage	Vss-0.5V	V_{DD}+0.5V

Environmental Performance Specifications

Green Requirement	RoHS 6/6 (2002/95/EC) and WEEE (2002/96/EC) compliant
MSL Level	Level 1 per IPC/JEDEC J-STD-020D.1
Storage temp. range	-55°C to +125°C
Humidity	85% RH, 85°C, 48 hours
Hermetic seal	Leak rate $2x10^{-8}$ ATM-cm^3/sec max.
Solderability	MIL-STD-202F method 208E
Reflow	260°C for 10 sec max.. 2 times max.
Vibration	MIL-STD-202F method 204, 35G, 50 to 2000 Hz
Shock	MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave
ESD Protection	2KV max. Human body model.
Contact pad surface finish	Gold (0.3~1.0 um) on nickel (1.27~8.89 um)
Weight per unit	160 mg typical

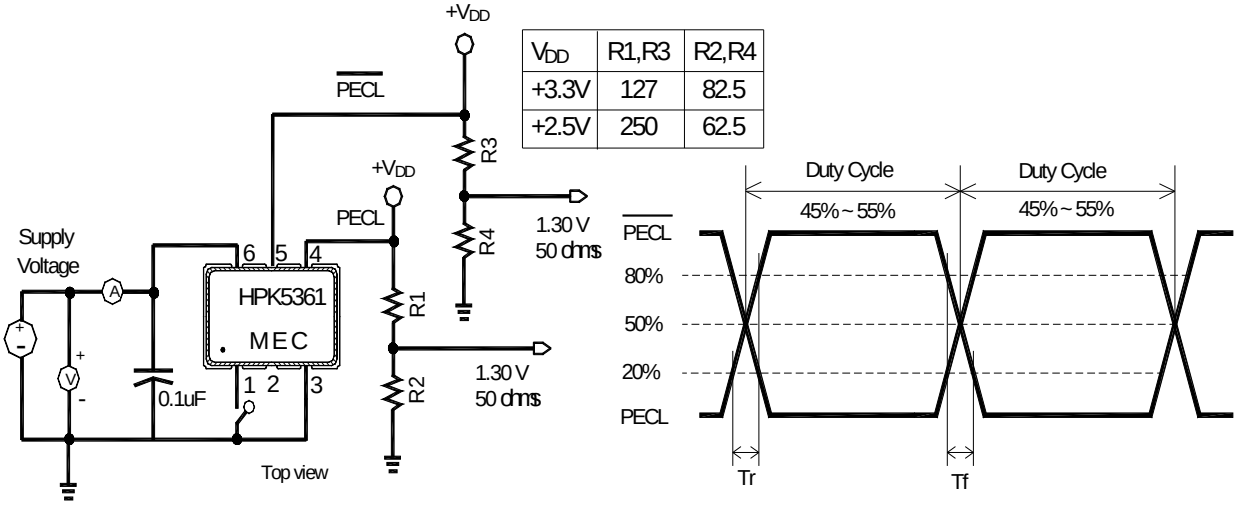
Part Number Format and Examples:

Example: 3HPK5361-A-155.520; 25HPK5361-A-155.520
Explanation: +3.3V HPK5361 series LVPECL output clock oscillator, frequency stability is ±25 ppm over -10°C to +70°C, 155.520 MHz

			✍		✍	✍: customer to specify
3	HPK5361	—	A	—	155.520	
①	②		③		④	

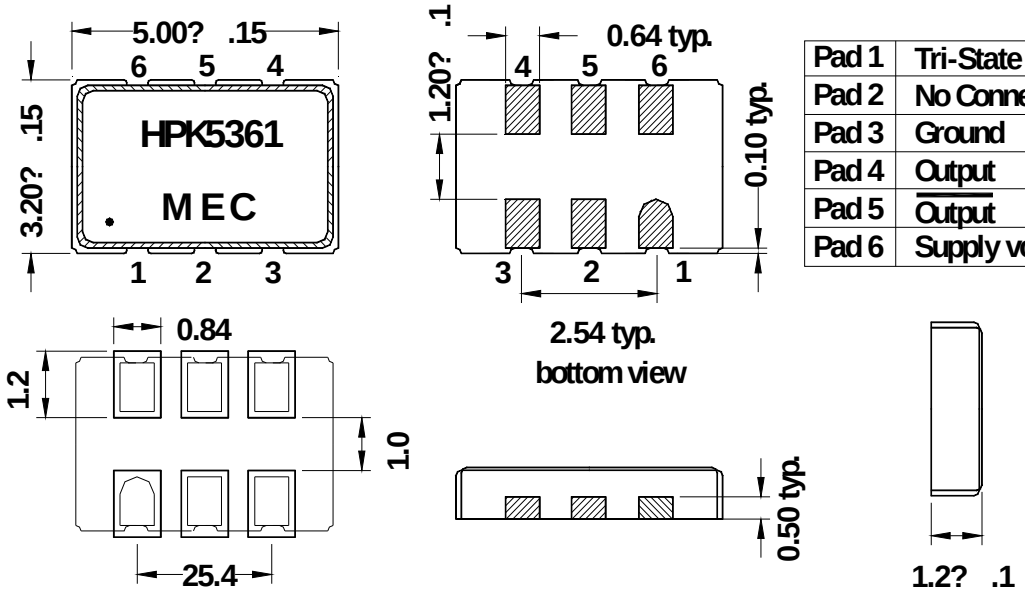
①: V_{DD} voltage codes: "3" for +3.3 V; "25" for +2.5 V ②: HPK5361 product series. 'H" for clock; "P" for PECL; "K": for "K" family characteristics."536" for 3.2x5 mm SMD with 6 pads. '1" for Tri-State on pad 1.
③: Frequency stability code: "A" ~ "F" or custom. See table above. ④: Frequency in MHz

25HPK5361 and 3HPK5361 Test Circuit and Waveform:



V_{DD}	R1,R3	R2,R4
+3.3V	127	82.5
+2.5V	250	62.5

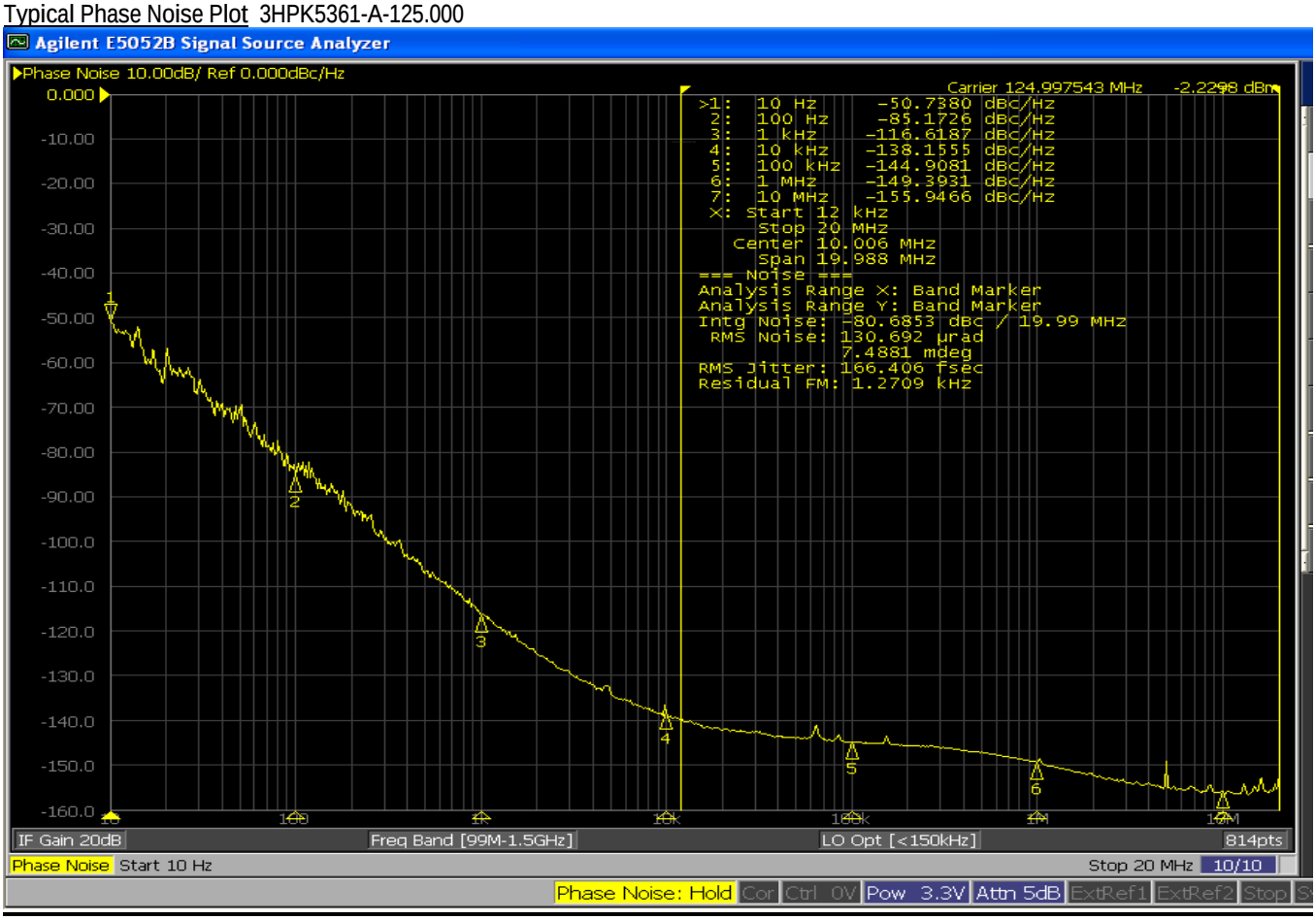
HPK5361 Package Dimensions and Recommended Solder Pad Layout: unit mm



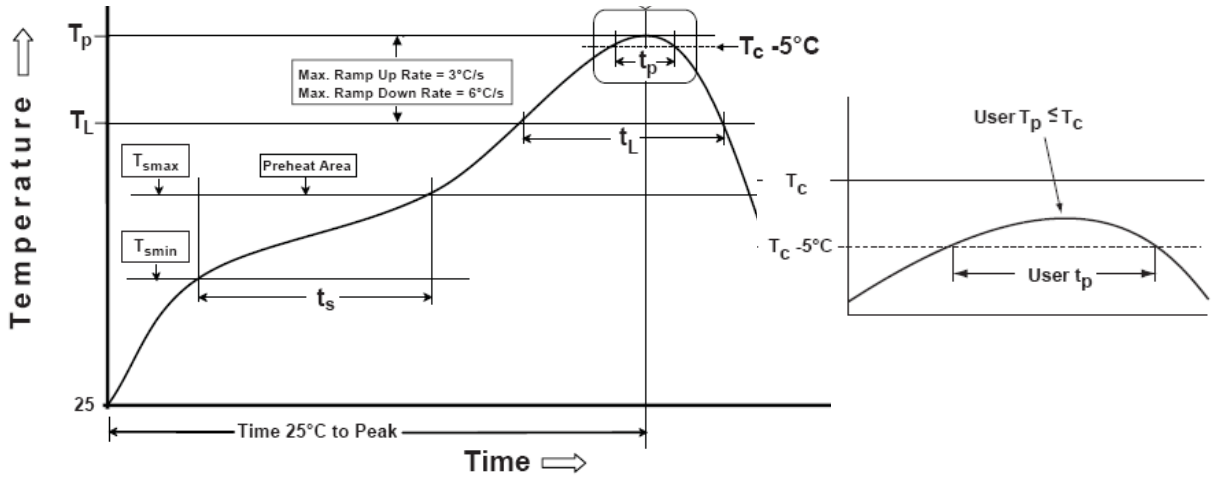
Pad 1	Tri-State
Pad 2	No Connection
Pad 3	Ground
Pad 4	Output
Pad 5	$\overline{\text{Output}}$
Pad 6	Supply voltage

Rounded pad is pad No. 1. Count counter-clockwise when looking at top view.
Count clockwise when looking at bottom view.

Typical Phase Noise Plot 3HPK5361-A-125.000



HPK5361 Recommended Solder Reflow Profile (from IPC/JEDEC J-STD-020D.1)



Profile Feature	Sn-Pb Eutectic Assembly	Pb-free Assembly
Preheat/Soak		
- Temperature min. (Ts min.)	100ºC	150ºC
- Temperature max. (Ts max.)	150ºC	200ºC
- Time (ts) (Ts min. to Ts max.)	60 to 120 seconds	60 to 180 seconds
Ramp-up rate (T_L to Tp)	3ºC / sec. max.	3ºC / sec. max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183ºC 60 to 150 seconds	217ºC 60 to 150 seconds
Peak package body temperature (Tp)	235ºC	260ºC
Time (Tp) within 5ºC of the classification temperature Tc	10 to 30 seconds	20 to 40 seconds
Ramp-down rate (Tp to T_L)	6ºC / second max.	6ºC / second max.
Time 25ºC to peak temperature	6 minutes max.	8 minutes max.

All temperatures refer to topside of the package, measured on the package body surface.