



N-CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

DESCRIPTION

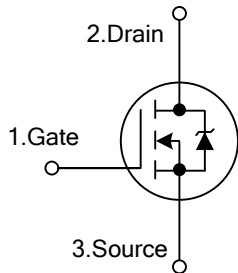
The UTC **25N06** is an N-channel enhancement mode Power MOSFET, which provides low gate charge, avalanche rugged technology, and so on.

The UTC **25N06** is universally applied in DC-DC & DC-AC converters, motor control, high current, high speed switching, solenoid and relay drivers, regulators, audio amplifiers, automotive environment.

FEATURES

- * Low Gate Charge
- * $R_{DS(on)} = 0.048 \Omega$ (TYP.)
- * Avalanche Rugged Technology
- * 100% Avalanche Tested
- * Repetitive Avalanche at 100°C
- * High Current Capability
- * Operating Temperature: 175°C
- * Application Oriented Characterization

SYMBOL

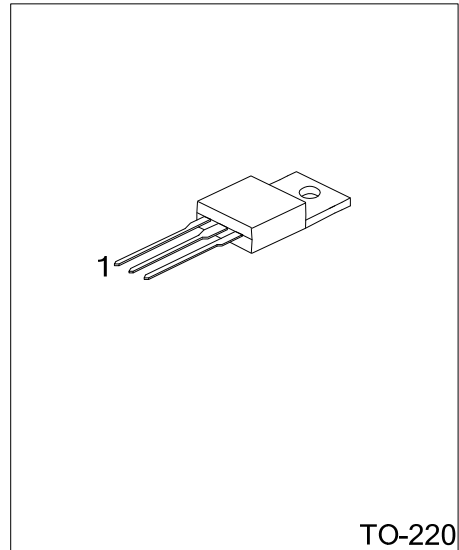


ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
25N06L-TA3-T	25N06G-TA3-T	TO-220	G	D	S	Tube

Note: G: Gate, D: Drain, S: Source

<p>25N06G-TA3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Halogen Free</p>	<p>(1) T: Tube</p> <p>(2) TA3: TO-220</p> <p>(3) G: Halogen Free</p>
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■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage ($V_{GS}=0$)	V_{DS}	60	V
Drain-Gate Voltage ($R_{GS}=20k\Omega$)	V_{DGR}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current (Continuous)	I_D	$T_C=25^\circ\text{C}$	25
		$T_C=100^\circ\text{C}$	17
Drain Current (Pulsed) (Note 2)	I_{DM}	100	A
Single Pulse Avalanche Energy (starting $T_J=25^\circ\text{C}$, $I_D=25\text{A}$, $V_{DD}=25\text{V}$)	E_{AS}	100	mJ
Total Dissipation at $T_C=25^\circ\text{C}$	P_D	90	W
Maximum Operating Junction Temperature	T_J	175	$^\circ\text{C}$
Storage Temperature	T_{STG}	-65 ~ +175	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by safe operating area

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C/W}$
Junction to Case	θ_{JC}	1.57	$^\circ\text{C/W}$

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	60			V
Drain-Source Leakage Current (V _{GS} =0)	I _{DSS}	V _{DS} =Max Rating			1	μA
		V _{DS} = Max Rating×0.8, T _C =125°C			10	
Gate- Source Leakage Current (V _{DS} =0)	I _{GSS}	V _{GS} =±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2	2.9	4	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =12.5A		0.048	0.065	Ω
On State Drain Current	I _{D(on)}	V _{DS} >I _{D(on)} ×R _{DS(on)max} , V _{GS} =10V	25			A
Forward Transconductance (Note 1)	g _{FS}	V _{DS} >I _{D(on)} ×R _{DS(on)max} , I _D =12.5A	7	11		S
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1MHz		700	900	pF
Output Capacitance	C _{OSS}			320	450	pF
Reverse Transfer Capacitance	C _{RSS}			90	150	pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DD} =40V, V _{GS} =10V, I _D =25A		26	40	nC
Gate to Source Charge	Q _{GS}			8		nC
Gate to Drain Charge	Q _{GD}			9		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =30V, I _D =3A, R _G =50Ω,		30	45	ns
Rise Time	t _R	V _{GS} =10V		90	130	
Turn-OFF Delay Time	t _{D(OFF)}	V _{DD} =40V, I _D =25A, R _G =50Ω, V _{GS} =10V		80	120	ns
Fall-Time	t _F			80	120	ns
Cross-Over Time	t _C			170	250	ns
Turn-on Current Slope	(di/dt) _{on}	V _{DD} =40V, I _D =25A, R _G =50Ω, V _{GS} =10V		230		A/μs
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _{SD} =25A, V _{GS} =0V			1.5	V
Reverse Recovery Time	t _{RR}	I _{SD} =25A, di/dt=100A/μs, V _{DD} =30V, T _J =150°C		80		ns
Reverse Recovery Charge	Q _{RR}			0.22		μC
Reverse Recovery Current	I _{RPM}			5.5		A
Source-Drain Current	I _{SD}				25	A
Source-Drain Current (Pulsed) (Note 2)	I _{SDM}				100	A

Note: 1. Pulsed: Pulse duration = 300μs, duty cycle 1.5%.

2. Pulse width limited by safe operating area

■ SWITCHING TIME TEST CIRCUIT

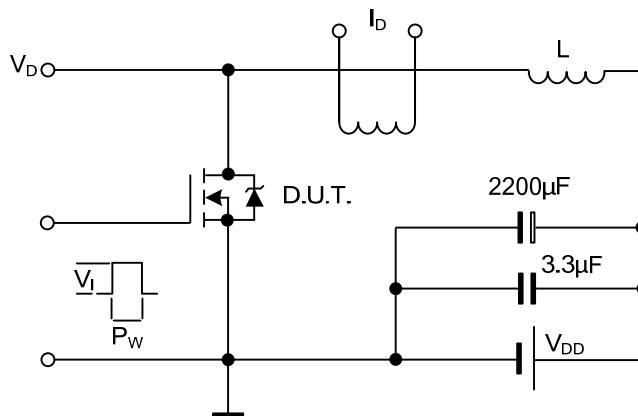


Fig. 1 Unclamped Inductive Load Test Circuits

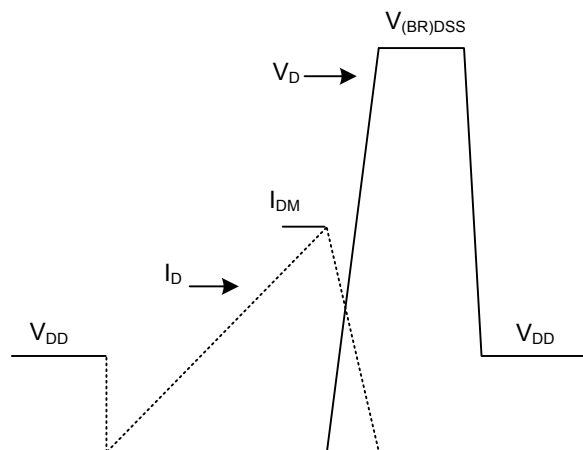


Fig. 2 Unclamped Inductive Waveforms

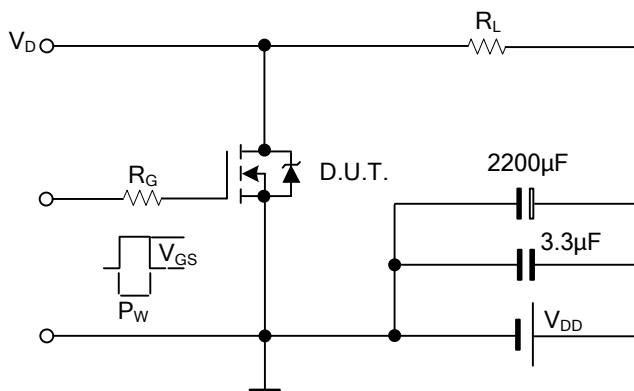


Fig. 3. Switching Times Test Circuits For Resistive Load

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■ SWITCHING TIME TEST CIRCUIT (Cont.)

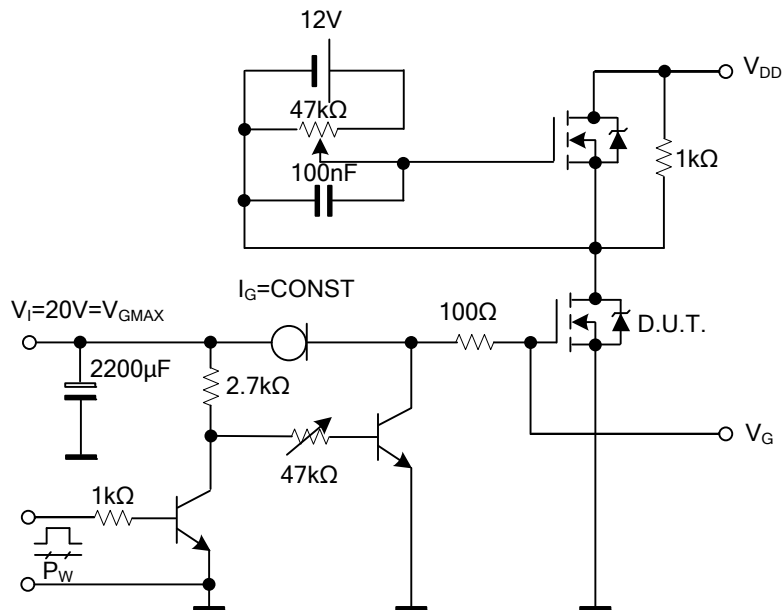


Fig. 4 Gate Charge Test Circuit

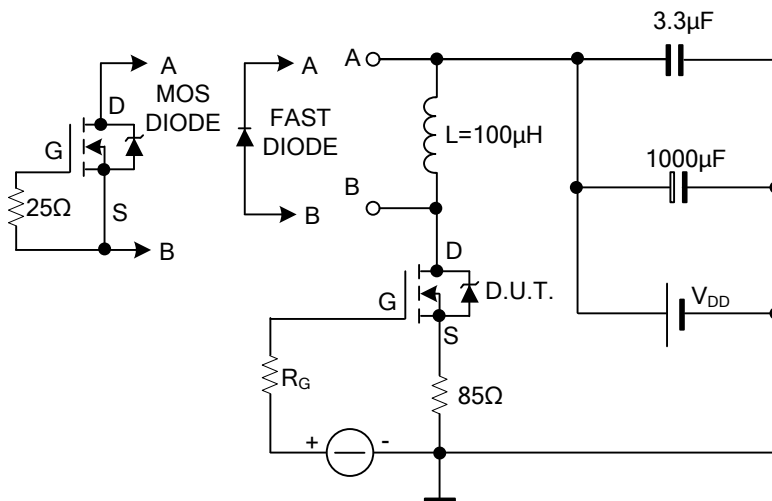


Fig. 5 Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time

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