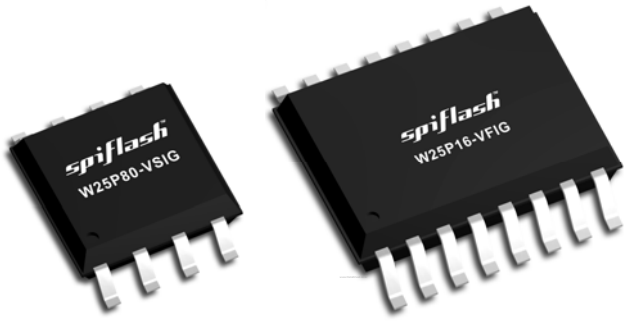
# 8M-BIT AND 16M-BIT SERIAL FLASH MEMORY




**Formally NexFlash NX25P80 and NX25P16**

The Winbond W25P80/16 are fully compatible with the previous NexFlash NX25P80/16 Serial Flash memories.

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## 1. GENERAL DESCRIPTION

The W25P80 (8M-bit) and W25P16 (16M-bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. They are ideal for code download applications as well as storing voice, text and data. The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1µA for power-down. Devices are offered in space-saving SOIC packages. As part of a family of Serial Flash products, Winbond also offers compatible devices in 1M/2M/4M-bit densities.

The W25P80/16 array is organized into 4,096/8,192 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instruction. Pages are grouped into 16/32 erasable sectors of 256 pages (64K-byte) each as shown in figure 2. Both Sector Erase and Chip (full chip) Erase instructions are supported. Additionally, a 256-byte Parameter Page is provided for user data that is typically stored in EEPROMs such as ID or revision numbers and configuration parameters. The parameter page is separate from the main array allowing for much faster erase times.

The Serial Peripheral Interface (SPI) consists of four pins (Serial Clock, Chip Select, Serial Data In and Serial Data Out) that support high speed serial data transfers up to 50MHz. A Hold pin, Write Protect pin and programmable write protect features provide further control flexibility. Additionally, the device can be queried for manufacturer and device type.

The Winbond W25P80/16 are fully compatible with the previous NexFlash NX25P80/16 Serial Flash memories.

## 2. FEATURES

- **8M / 16M / 32M-bit Serial Flash Memories**
- **Family of Serial Flash Memories**
  - W25P80: 8M-bit/1M-byte (1,048,576)
  - W25P16: 16M-bit/2M-byte (2,097,152)
  - 256-bytes per programmable page
  - Compatible 1M/2M/4M-bit devices
- **4-pin SPI Serial Interface**
  - Clock, Chip Select, Data In, Data Out
  - Easily interfaces to popular microcontrollers
  - Compatible with SPI Modes 0 and 3
  - Optional Hold function for SPI flexibility
- **Low Power Consumption, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, 1µA Power-down (typ)
  - -40° to +85°C operating range
- **Fast and Flexible Serial Data Access**
  - Clock operation to 50MHz
  - Auto-increment Read capability
  - Manufacturer and device type ID
- **Programming Features**
  - Page program up to 256 bytes in 3.5ms
  - Sector Erase (64K-byte) 0.6 seconds
  - 100,000 erase/write cycles
  - Twenty-year data retention
- **Software and Hardware Write Protection**
  - Write-Protect all or portion of memory
  - Enable/Disable protection with /WP pin
- **Parameter Page**
  - 256 Byte page for ID# revision# or configuration data
  - Separate from array, erase time <200ms
- **Space Saving Packaging**
  - 8-pin SOIC (W25P80 and W25P16)
  - 16-pin SOIC (W25P16)
- **Ideal for systems with limited pins, space, and power**
  - Controller-based serial code-download
  - µC systems storing data, text or voice
  - Battery-operated and portable products

## 3. PIN CONFIGURATION 208-MIL

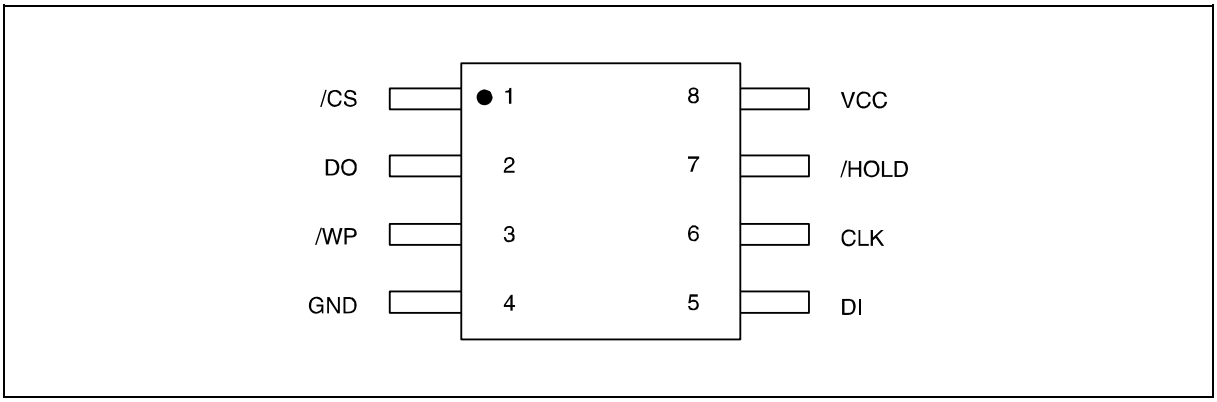



Figure 1a. W25P80/16 Pin Assignments, 8-pin SOIC 208-mi

## 4. PIN DESCRIPTION 208-MIL

| PIN NO. | PIN NAME | I/O | FUNCTION |
|---|---|---|---|
| 1 | /CS | I | Chip Select Input |
| 2 | DO | O | Data Output |
| 3 | /WP | I | Write Protect Input |
| 4 | GND | | Ground |
| 5 | DI | I | Data Input |
| 6 | CLK | I | Serial Clock Input |
| 7 | /HOLD | I | Hold Input |
| 8 | VCC | | Power Supply |

## 5. PIN CONFIGURATION 300-MIL

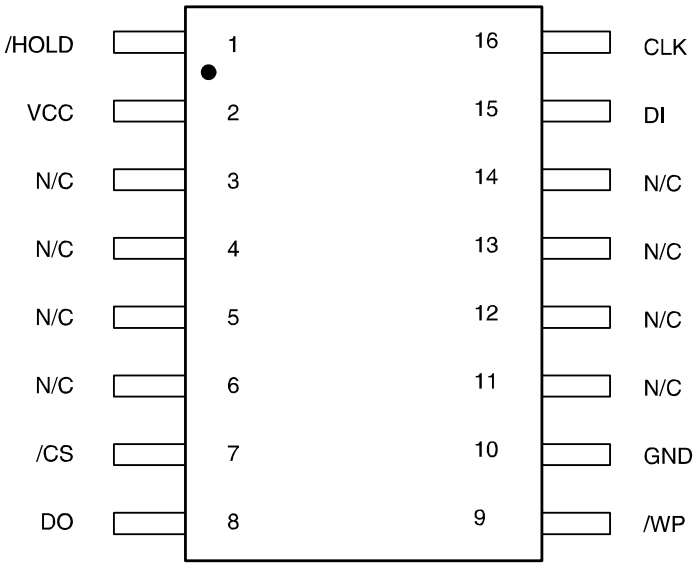



Figure 1b. W25P16 Pin Assignments, 16-pin SOIC 300-mil

## 6. PIN DESCRIPTION 300-MIL

| PAD NO. | PAD NAME | I/O | FUNCTION |
|---|---|---|---|
| 1 | /HOLD | I | Hold Input |
| 2 | VCC | | Power Supply |
| 3 | N/C | | No Connect |
| 4 | N/C | | No Connect |
| 5 | N/C | | No Connect |
| 6 | N/C | | No Connect |
| 7 | /CS | I | Chip Select Input |
| 8 | DO | O | Data Output |
| 9 | /WP | I | Write Protect Input |
| 10 | GND | | Ground |
| 11 | N/C | | No Connect |
| 12 | N/C | | No Connect |
| 13 | N/C | | No Connect |
| 14 | N/C | | No Connect |
| 15 | DI | I | Data Input |
| 16 | CLK | I | Serial Clock Input |

## 6.1 Package Types

The W25P80/16 are primarily offered in SOIC packages. The W25P80 and W25P16 use an 8-pin plastic 208-mil width SOIC (Winbond package code SS) (NexFlash package code S) and the W25P16 also uses a 16-pin plastic 300-mil width SOIC (Winbond package code SF) (NexFlash package code F) as shown in figures 1A and 1B respectively. Package diagrams and dimensions are illustrated at the end of this data sheet. Optional 8-contact MLP packages may be available. Please contact Winbond for further MLP package information.

## 6.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection” and figure 16). If needed a pull-up resister on /CS can be used to accomplish this.

## 6.3 Serial Data Output (DO)

The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

## 6.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (BP2, BP1, and BP0) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The /WP pin is active low.

## 6.5 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. (“See Hold function”)

## 6.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI "Operations")

## 6.7 Serial Data Input (DI)

The SPI Serial Data Input (DI) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin.

## 7. BLOCK DIAGRAM

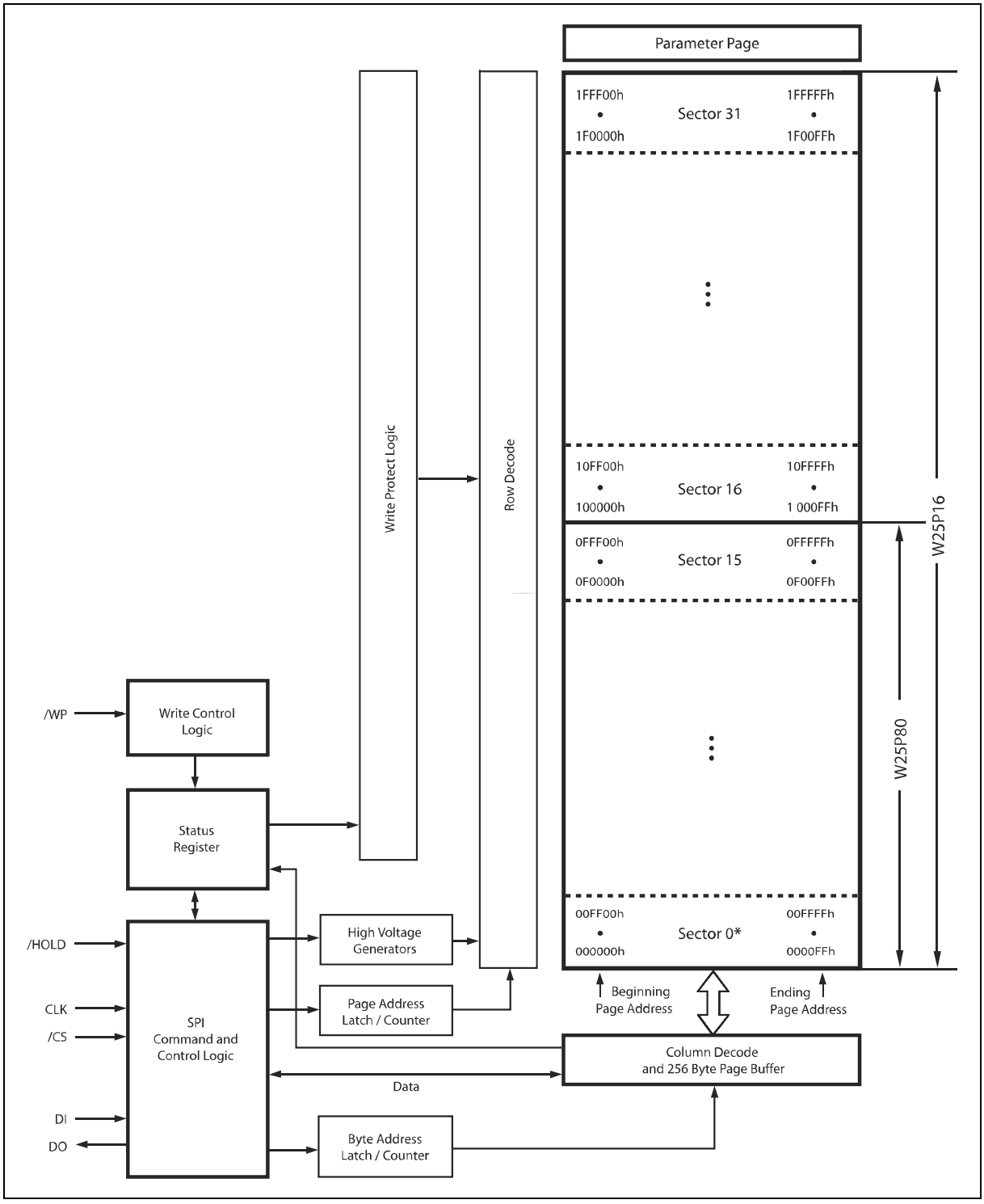



Figure 2. W25P80 and W25P16 Block Diagram

# 8. FUNCTIONAL DESCRIPTION

## 8.1 SPI OPERATIONS

### 8.1.1 SPI Modes

The W25P80/16 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

### 8.1.2 HOLD Function

The /HOLD signal allows the W25P80/16 operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK.

During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

## 8.2 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the W25P80/16 provides several means to protect data from inadvertent writes.

### 8.2.1 Write Protect Features

- Device resets when VCC is below threshold.
- Time delay write disable after Power-up.
- Write enable/disable instructions.
- Automatic write disable after program and erase.
- Software write protection using Status Register.
- Hardware write protection using Status Register and /WP pin.
- Write Protection using Power-down instruction.

Upon power-up or at power-down the W25P80/16 will maintain a reset condition while VCC is below the threshold value of $V_{WI}$, (See Power-up Timing and Voltage Levels and Figure 17). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds $V_{WI}$, all program and erase related instructions are further disabled for a time delay of $t_{PUW}$. This includes the Write Enable, Page Program, Sector Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and $t_{VSL}$ time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (BP2, BP1, and BP0) bits. These Status Register bits allow a portion or all of the memory to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information.

Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

## 9. CONTROL AND STATUS REGISTERS

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, and the state of write protection. The Write Status Register instruction can be used to configure the devices write protection features. See Figure 3.

### 9.1 STATUS REGISTER

#### 9.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see $t_W$, $t_{PP}$, $t_{SE}$ and $t_{CE}$ in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

#### 9.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Chip Erase and Write Status Register.

### 9.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

### 9.1.4 Reserved Bits

Status register bit locations 5 and 6 are reserved for future use. Current devices will read 0 for these bit locations. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

### 9.1.5 Status Register Protect (SRP)

The Status Register Protect (SRP) bit is a non-volatile
read/write bit in the status register (S7) that can be used in conjunction with the Write Protect (/WP) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

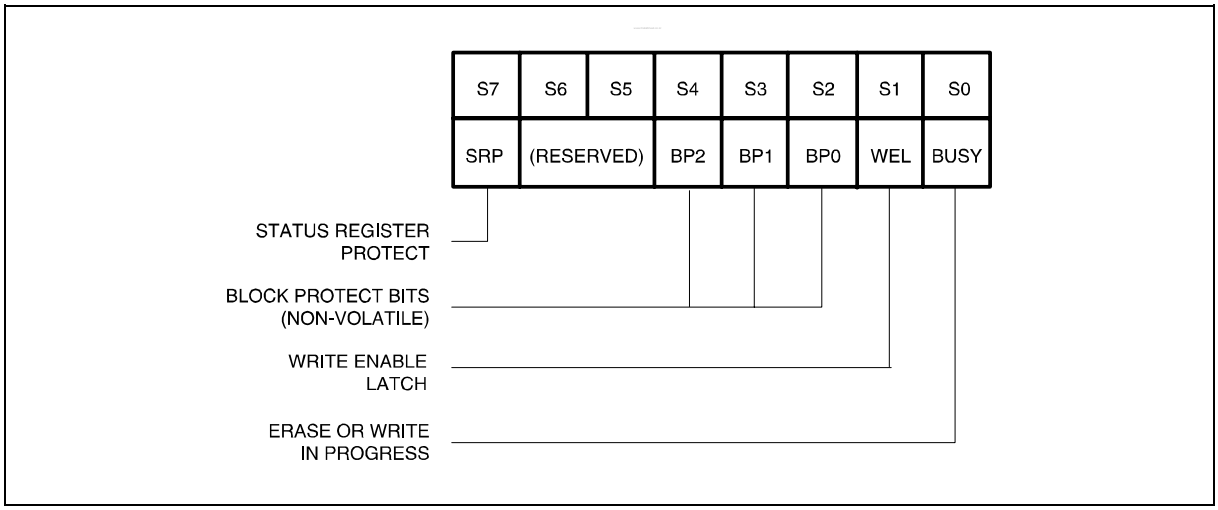



Figure 3. Status Register Bit Locations

### 9.1.6 Status Register Memory Protection

| STATUS REGISTER(1) | | | W25P16 (16M-BIT) MEMORY PROTECTION | | | |
|---|---|---|---|---|---|---|
| **BP2** | **BP1** | **BP0** | **SECTOR(S)** | **ADDRESSES** | **DENSITY (KB)** | **PORTION** |
| 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 1 | 31 | 1F0000h - 1FFFFFh | 512K-bit | Upper 1/32 |
| 0 | 1 | 0 | 30 and 31 | 1E0000h - 1FFFFFh | 1M-bit | Upper 1/16 |
| 0 | 1 | 1 | 28 thru 31 | 1C0000h - 1FFFFFh | 2M-bit | Upper 1/8 |
| 1 | 0 | 0 | 24 thru 31 | 180000h - 1FFFFFh | 4M-bit | Upper 1/4 |
| 1 | 0 | 1 | 16 thru 31 | 100000h - 1FFFFFh | 8M-bit | Upper 1/2 |
| 1 | 1 | x | ALL | 000000h - 1FFFFFh | All memory plus Parameter Page | |

| STATUS REGISTER(1) | | | W25P80 (8M-BIT) MEMORY PROTECTION | | | |
|---|---|---|---|---|---|---|
| **BP2** | **BP1** | **BP0** | **SECTOR(S)** | **ADDRESSES** | **DENSITY (KB)** | **PORTION** |
| 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 1 | 15 | 0F0000h - 0FFFFFh | 512K-bit | Upper 1/16 |
| 0 | 1 | 0 | 14 and 15 | 0E0000h - 0FFFFFh | 1M-bit | Upper 1/8 |
| 0 | 1 | 1 | 12 thru 15 | 0C0000h - 0FFFFFh | 2M-bit | Upper 1/4 |
| 1 | 0 | 0 | 8 thru 15 | 080000h - 0FFFFFh | 4M-bit | Upper 1/2 |
| 1 | 0 | 1 | ALL | 000000h - 0FFFFFh | All memory plus Parameter Page | |
| 1 | 1 | x | ALL | 000000h - 0FFFFFh | | |

**Note:**
1. x = don't care

## 9.2 INSTRUCTIONS

The instruction set of the W25P80/16 consists of thirteen basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 21. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

### 9.2.1 Manufacturer and Device Identification

| **MANUFACTURER ID** | **(M7-M0)** | |
|---|---|---|
| Winbond Serial Flash | EFh | |
| | | |
| **Device ID** | **(ID7-ID0)** | **(ID15-ID0)** |
| **Instruction** | **ABH, 90h** | **9Fh** |
| W25P80 | 13h | 2014h |
| W25P16 | 14h | 2015h |

### 9.2.2 Instruction Set (1)

| INSTRUCTION NAME | BYTE 1 CODE | BYTE 2 (5) | BYTE 3 | BYTE 4 | BYTE 5 | BYTE 6 | N-BYTES |
|---|---|---|---|---|---|---|---|
| Write Enable | 06h | | | | | | |
| Write Disable | 04h | | | | | | |
| Read Status Register | 05h | (S7–S0)(1) | | | | | (2) |
| Write Status Register | 01h | S7–S0 | | | | | |
| Read Data | 03h | A23–A16 | A15–A8 | A7–A0 | (D7–D0) | (Next byte) | continuous |
| Fast Read | 0Bh | A23–A16 | A15–A8 | A7–A0 | dummy | (D7–D0) | (Next Byte) continuous |
| Page Program | 02h | A23–A16 | A15–A8 | A7–A0(3) | (D7–D0) | (Next byte) | Up to 256 bytes (128 Words) (3) |
| Sector Erase | D8h | A23–A16 | A15–A8 | A7–A0 | | | |
| Chip Erase | C7h | | | | | | |
| Power-down | B9h | | | | | | |
| Read Parameter Page | 53h | Don't care | Don't care | A7–A0 | D7-D0 | Next Byte | Next Byte |
| Fast Read Parameter Page | 5Bh | Don't care | Don't care | A7–A0 | dummy | D7-D0 | Next Byte |
| Program Parameter Page | 52h | Don't care | Don't care | A7–A0(3) | D7-D0 | D15-D8 | Up to 256 bytes (128 Words) |
| Erase Parameter Page | D5h | | | | | | |
| Release Power-down / Device ID (4) | ABh | dummy | dummy | dummy | (ID7-ID0) | | (5) |
| Manufacturer/ Device ID (4) | 90h | dummy | dummy | 00h | (M7-M0) | (ID7-ID0) | |
| JEDEC ID | 9Fh | (M7-M0) Manufacturer | (ID15-ID8) Memory Type | (ID7-ID0) Capacity | | | |

**Notes:**
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until //CS terminates the instruction.
3. The Page Program instruction programs in increments of one word (two bytes) at a time. The Program address A23-A16 must be an "Even" Address (A0 must equal 0).
4. See Manufacturer and Device Identification table for Device ID information
5. The Device ID will repeat continuously until //CS terminates the instruction.

### 9.2.3 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

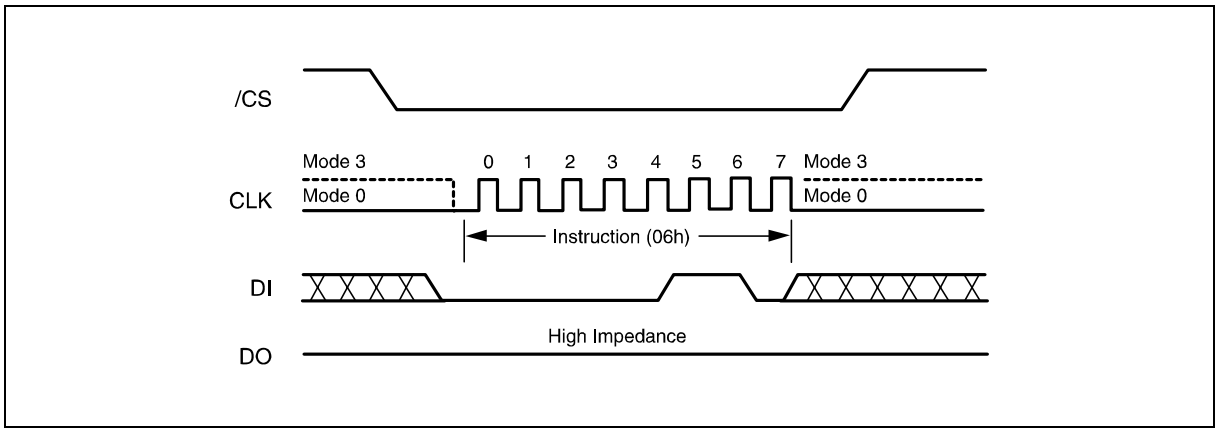



Figure 4. Write Enable Instruction Sequence Diagram

### 9.2.4 Write Disable (04h)

The Write Disable instruction (Figure 5) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, and Chip Erase instructions.

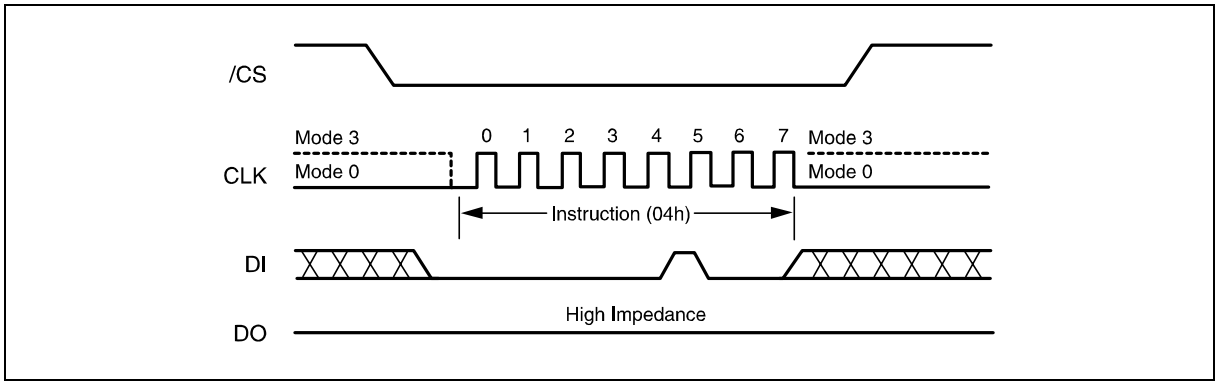



Figure 5. Write Disable Instruction Sequence Diagram

### 9.2.5 Read Status Register (05h)

The Read Status Register instruction allows the 8-bit Status Register to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3 and include the BUSY, WEL, BP2-BP0, and SRP bits (see description of the Status Register earlier in this data sheet).

The Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in figure 6. The instruction is completed by driving /CS high.

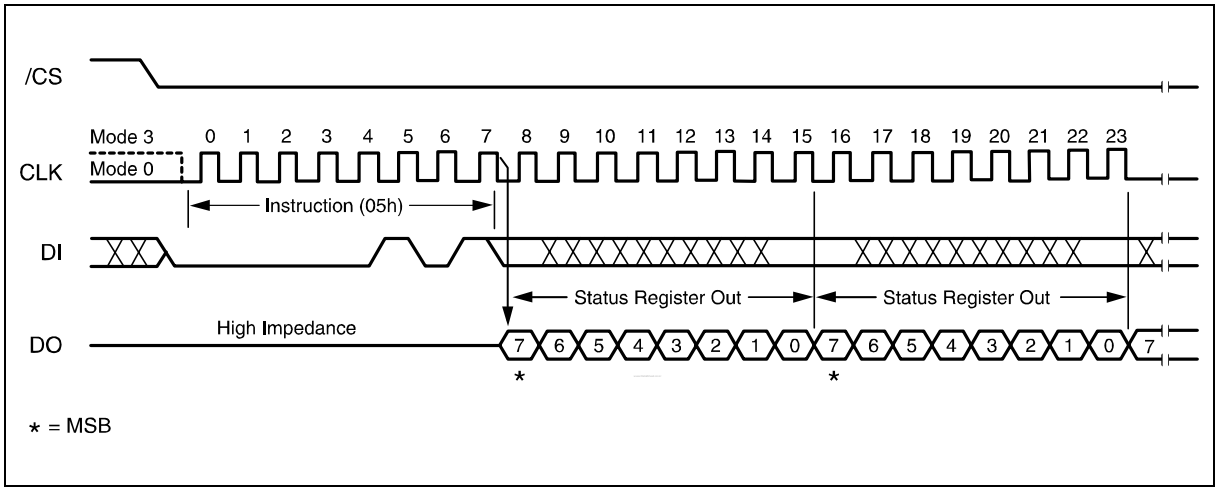



Figure 6. Read Status Register Instruction Sequence Diagram

### 9.2.6 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 7. The Status Register bits are shown in figure 3 and described earlier in this data sheet.

Only non-volatile Status Register bits SRP, BP2, BP1 and BP0 (bits 7, 4, 3 and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Write Status Register instruction will not be executed. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table). The Write Status Register instruction also allows the Status Register Protect bit (SRP) to be set. This bit is used in conjunction with the Write Protect (/WP) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

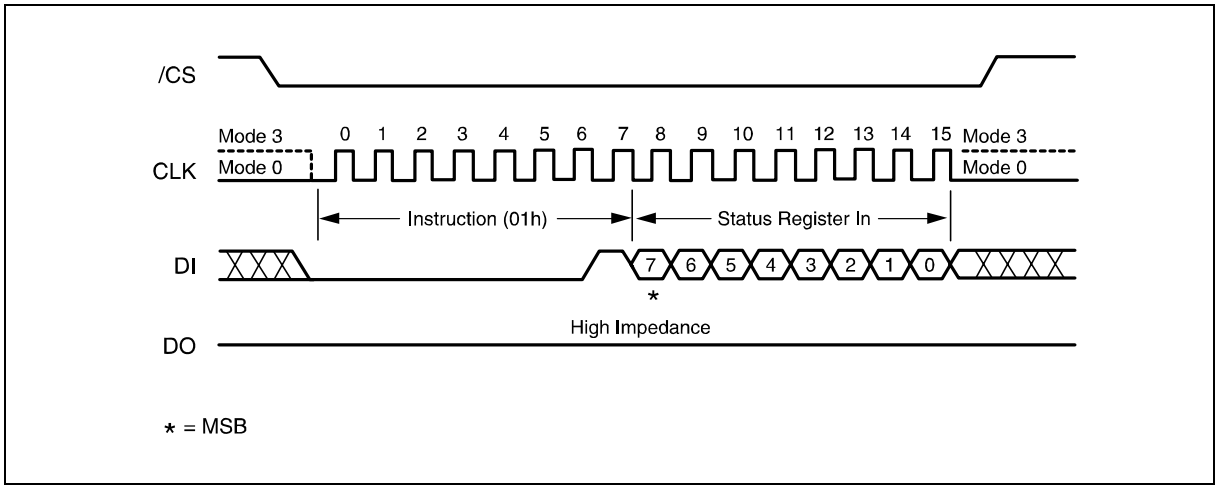



Figure 7. Write Status Register Instruction Sequence Diagram

### 9.2.7 Read Data (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The Read Data instruction sequence is shown in figure 8. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of $f_R$ ( see AC Electrical Characteristics).

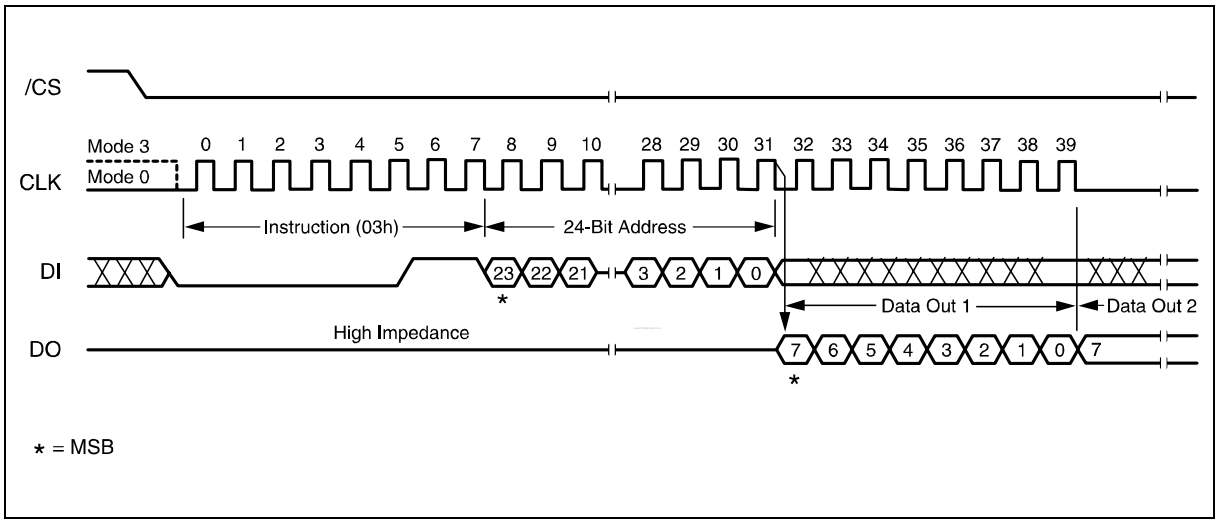



Figure 8. Read Data Instruction Sequence Diagram

### 9.2.8 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding a "dummy" byte after the 24-bit address as shown in figure 9. The dummy byte allows the devices internal circuits additional time for setting up the initial address. The dummy byte data value on the DI pin is a "don't care".

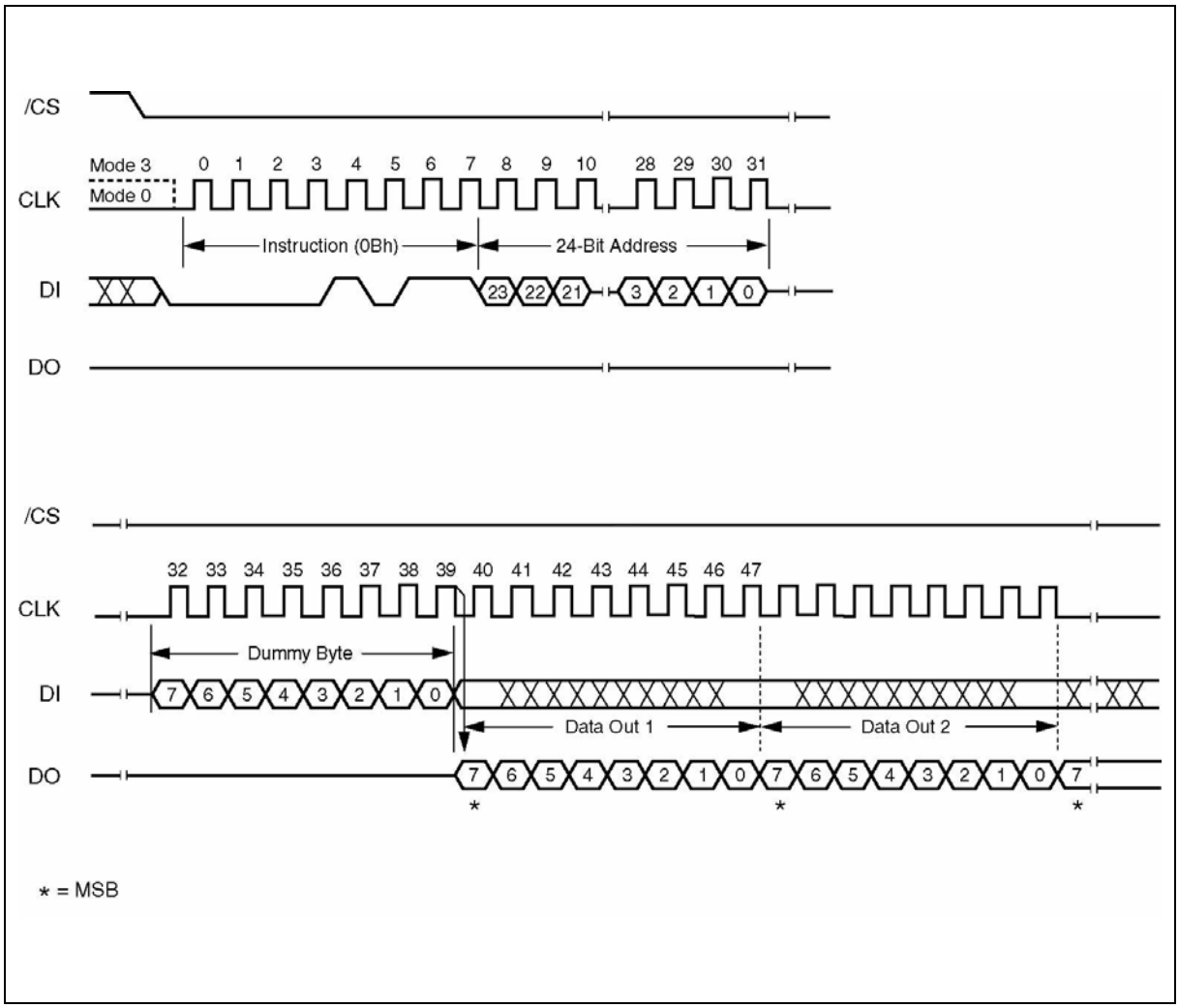



Figure 9. Fast Read Instruction Sequence Diagram

### 9.2.9 Page Program (02h)

The Page Program instruction allows up to 256 bytes of data to be programmed at previously erased to all 1s (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least two data bytes, into the DI pin. Because the W25P80/16 programs in increments of one word (two bytes) at a time the 24-bit address (A23-A0) must be an even address (A0 must equal 0). The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in figure 10.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. Less than 256 bytes can be programmed without having any effect on other bytes within the same page. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, BP0) bits (see Status Register Memory Protection table).

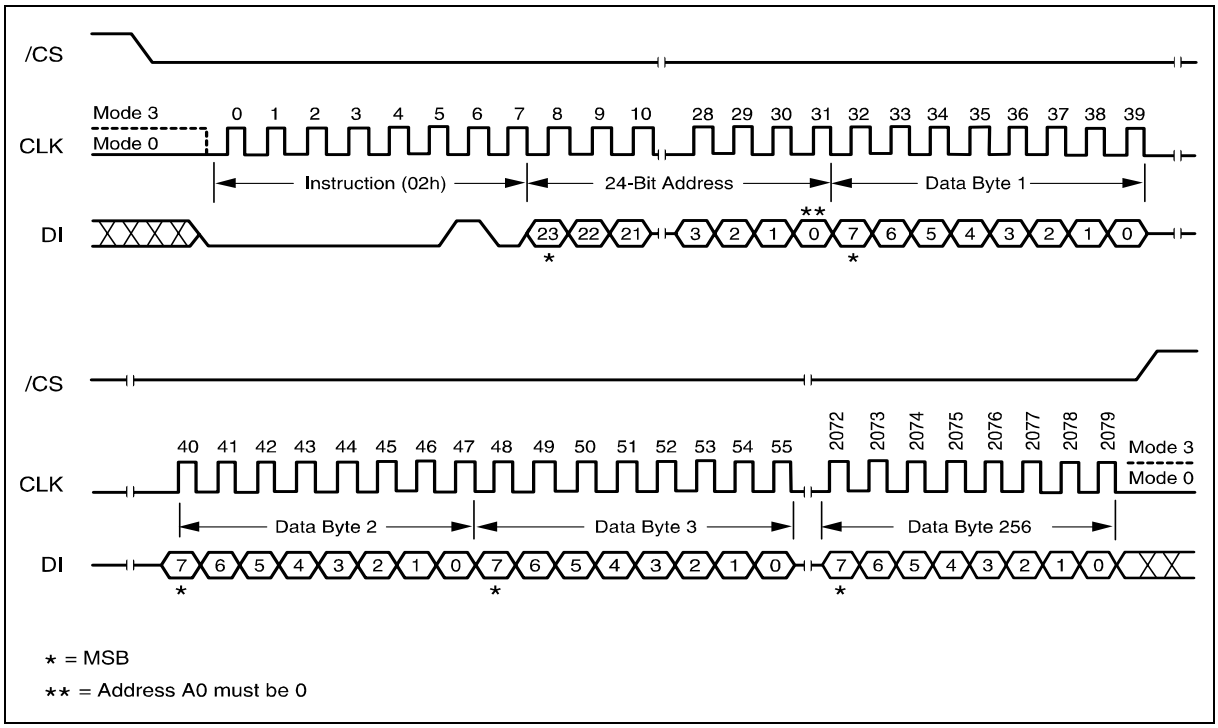



Figure 10. Page Program Instruction Sequence Diagram

### 9.2.10 Sector Erase (D8h)

The Sector Erase instruction sets all memory within a specified sector to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Erase Sector Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit sector address (A23-A0) (see Figure 2). The Sector Erase instruction sequence is shown in figure 11.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of $t_{SE}$ (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, BP0) bits (see Status Register Memory Protection table).

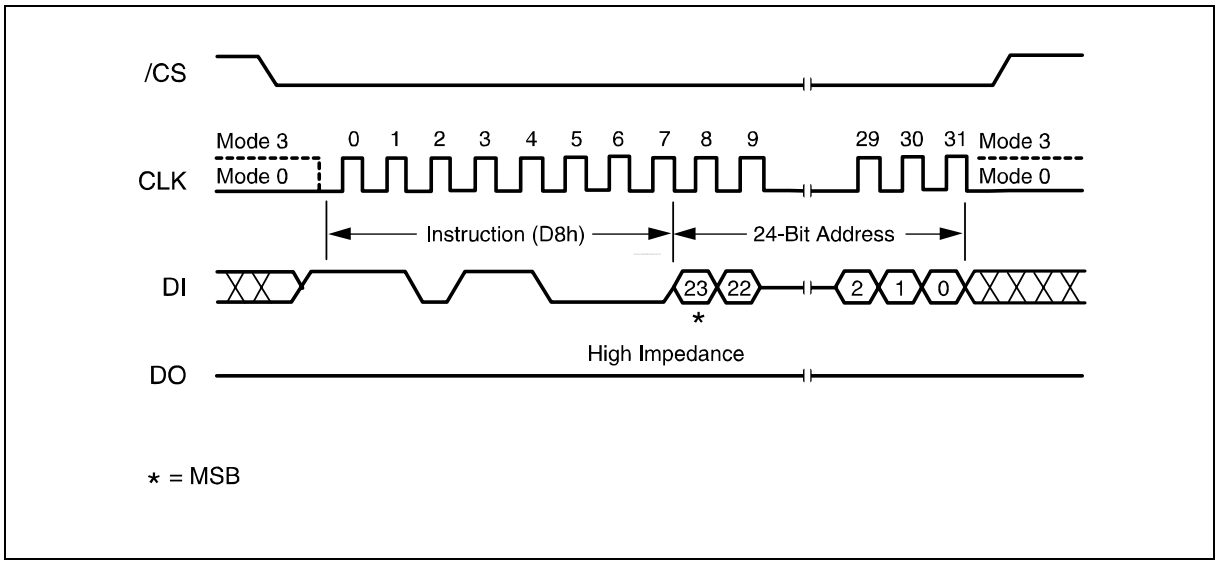



Figure 11. Sector Erase Instruction Sequence Diagram

### 9.2.11 Chip Erase (C7h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h”. The Chip Erase instruction sequence is shown in figure 12.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of $t_{CE}$ (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, BP0) bits (see Status Register Memory Protection table).

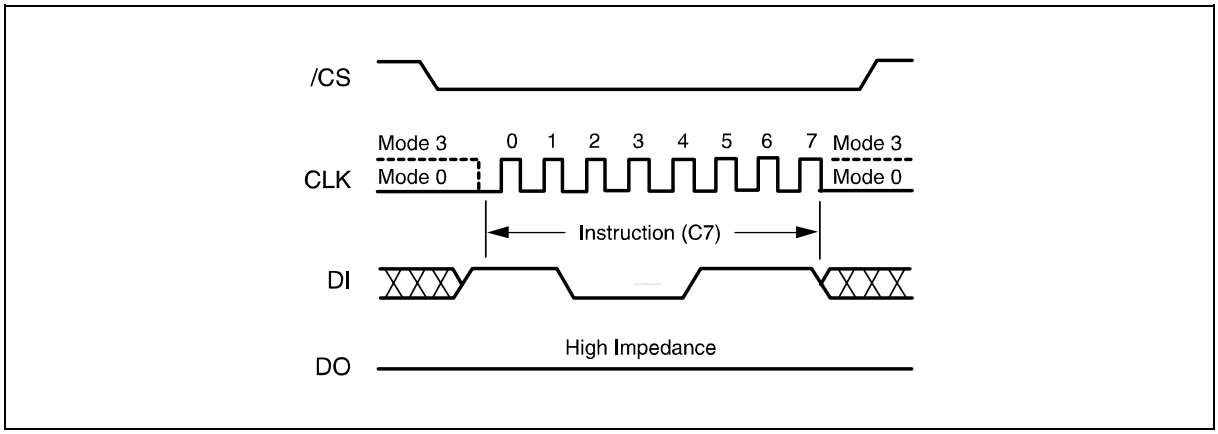



Figure 12. Chip Erase Instruction Sequence Diagram

### 9.2.12 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in figure 13.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of $t_{DP}$ (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

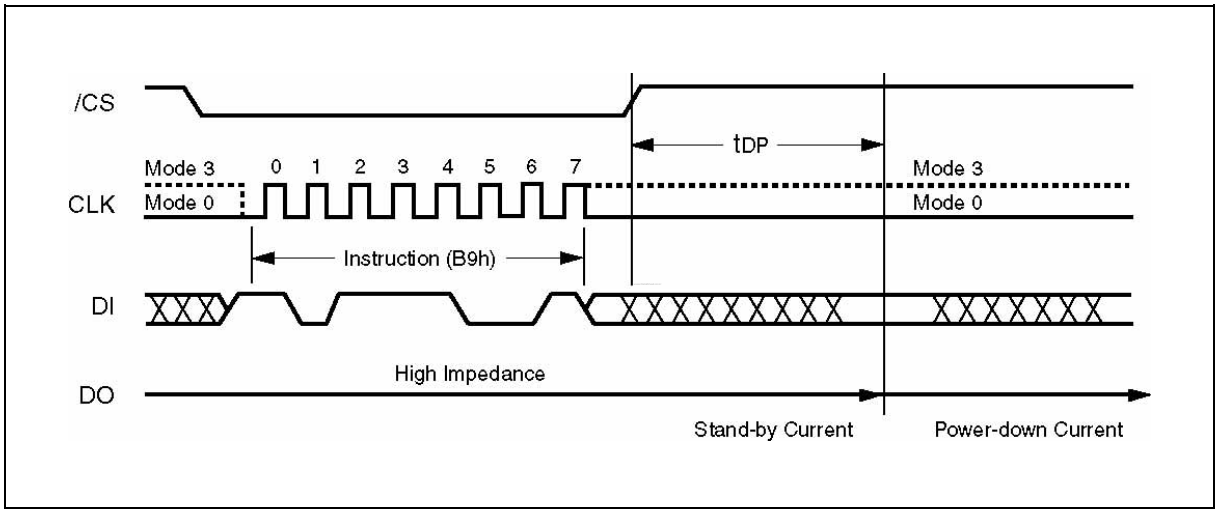



Figure 13. Deep Power-down Instruction Sequence Diagram

### 9.2.13 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, obtain the devices electronic identification (ID) number or do both.

When used only to release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code "ABh" and driving /CS high as shown in figure 14. After the time duration of $t_{RES1}$ (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The /CS pin must remain high during the $t_{RES1}$ time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 15. The Device ID values for the W25P80 and W25P16 are listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 13, except that after /CS is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted.

If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

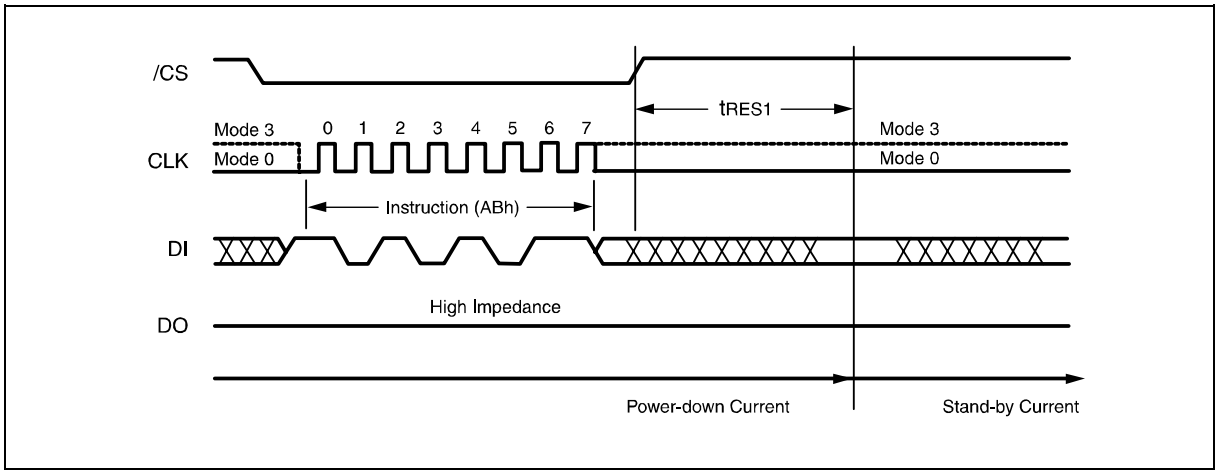



Figure 14. Release Power-down Instruction Sequence

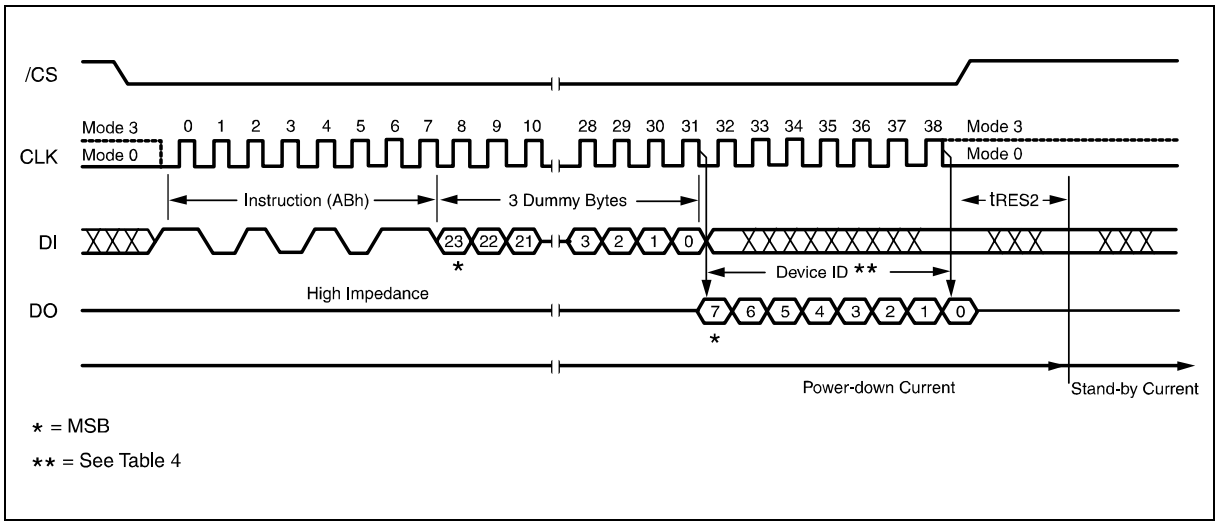



Figure 15. Release Power-down / Device ID Instruction Sequence Diagram

### 9.2.14 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 16. The Device ID values for the W25P80 and W25P16 are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

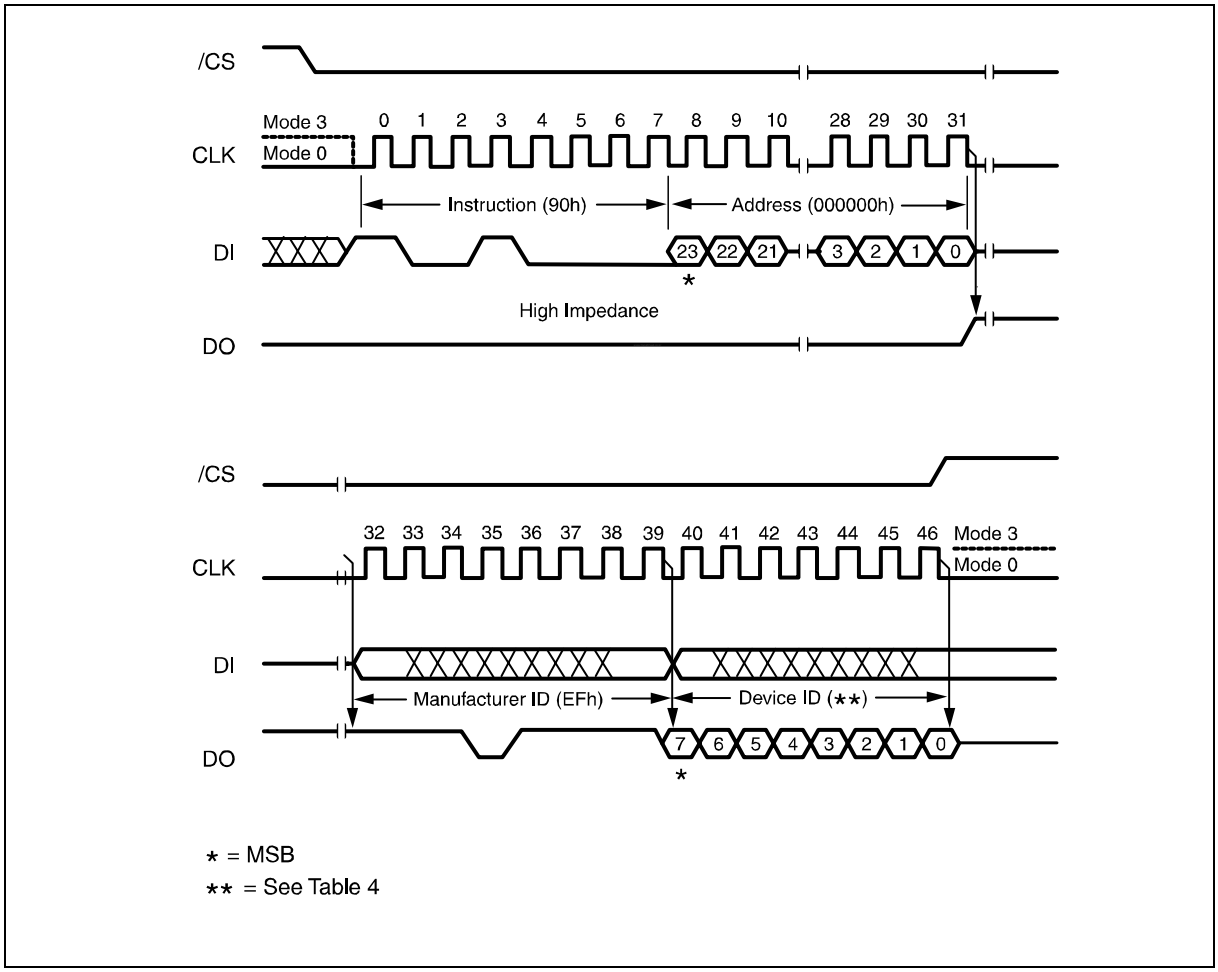



Figure 16. Read Manufacturer / Device ID Diagram

### 9.2.15 JEDEC ID (9Fh)

For compatibility reasons, the W25P80/16 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 17. For the W25P80, the Memory Type is 20h and the Capacity is 14h. For the W25P16, the Memory type is also 20h and the Capacity is 15h.

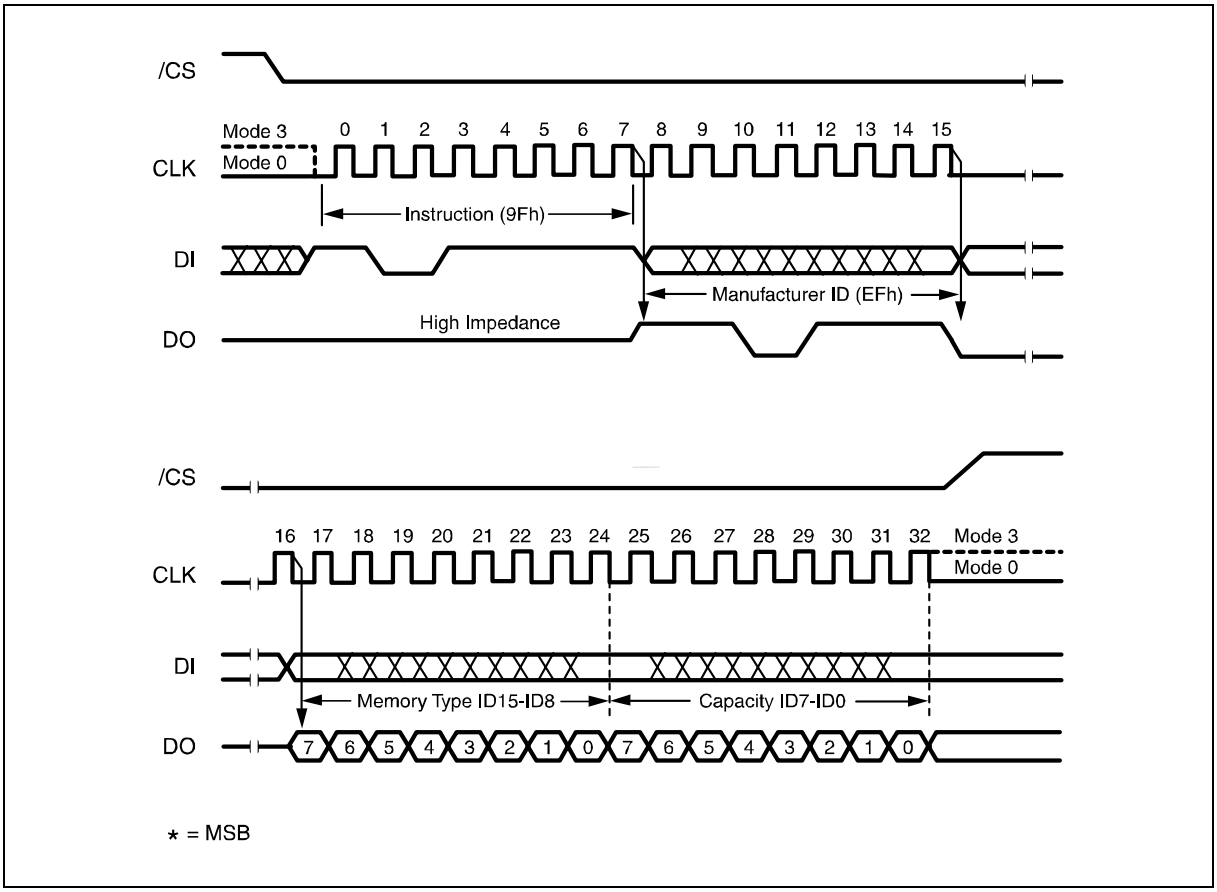



Figure 17. Read JEDEC ID

### 9.2.16 Read Parameter Page (53h)

The Parameter Page is a 256-byte page of Flash memory that can be used for storing serial numbers, revision information and configuration data that might typically be stored in an additional Serial EEPROM memory. Because the Parameter Page is relatively small and separate from the array, the erase time is significantly shorter than that of a sector erase (see tPE in AC Electrical Characteristics). This makes it convenient for more frequent updates.

The Read Parameter Page instruction allows one or more bytes of the Parameter page to be read. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “53h” followed by a 24-bit address (A23-A0) into the DI pin. Only the lower 8 address bits (A7-A0) are used, the 16 upper most address bits (A23-A8) are ignored (don’t care). The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. When the end of the Parameter page is reached the address will wrap to the beginning. The Read Parameter Page instruction is shown in figure 18. If the Read Parameter Page instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Parameter Page instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

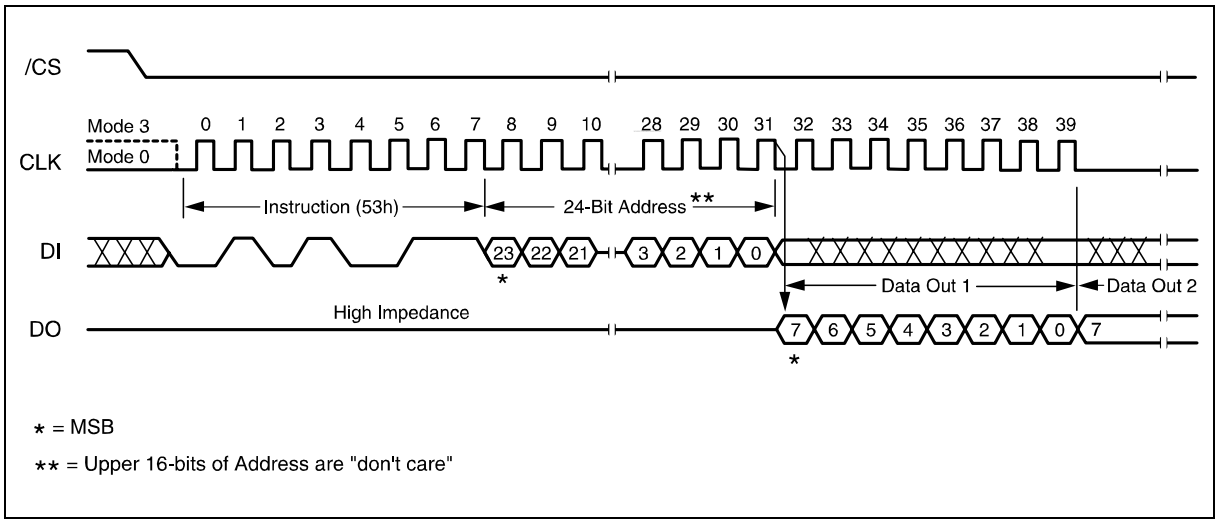



Figure 18. Read Parameter Page Instruction Sequence Diagram

### 9.2.17 Fast Read Parameter Page (5Bh)

The Fast Read Parameter Page instruction is basically the same as the Read Parameter Page instruction except that it allows for a faster clock rate to be used. The Fast Read Parameter Page instruction can opperate at clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics). This is accomplished by adding a “dummy” byte after the 24-bit address, as shown in figure 19. The dummy byte allows the devices internal circuits additional time for setting up the initial address. The dummy byte data value on the DI pin is a “don’t care”.

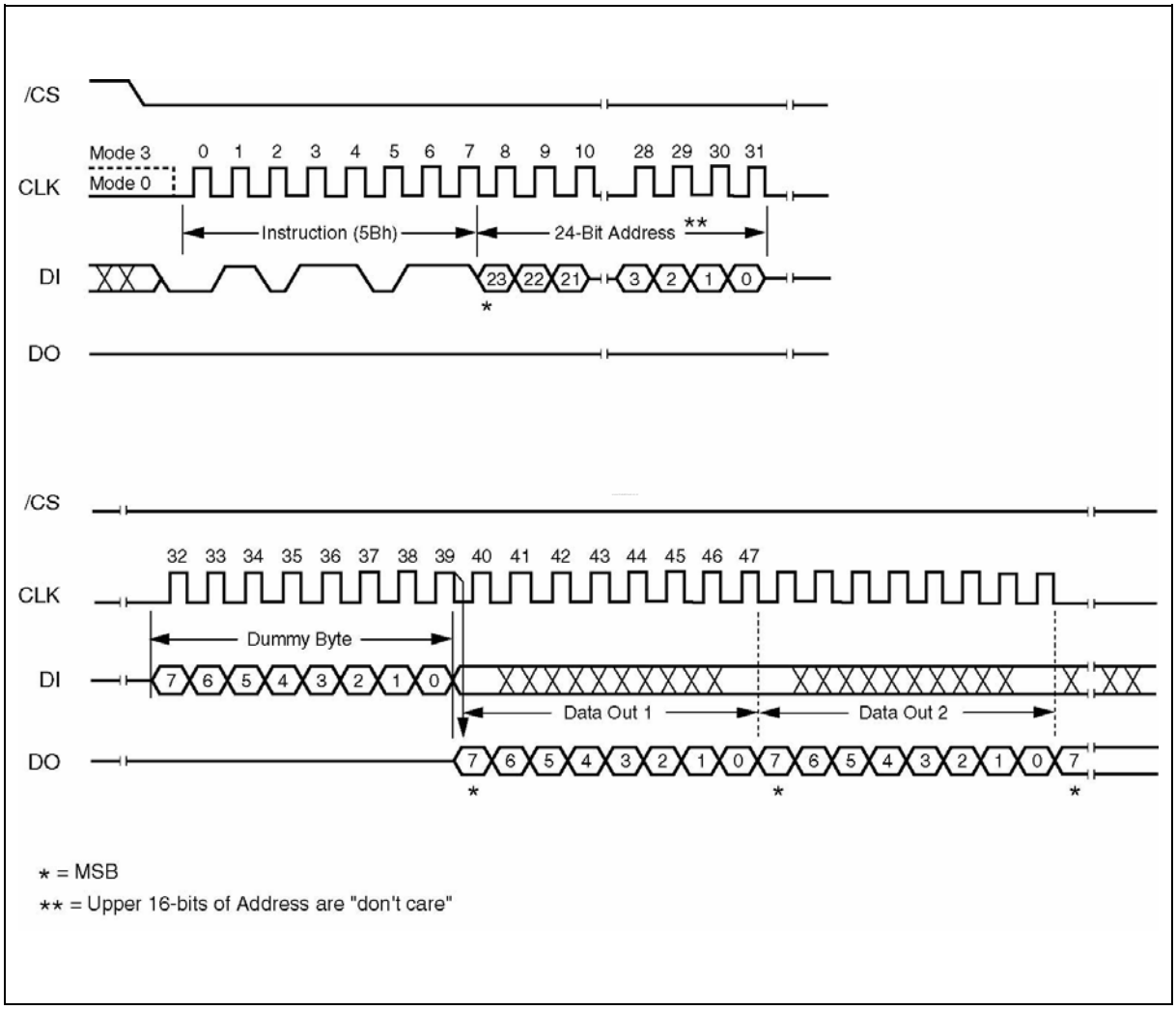



Figure 19. Fast Read Parameter Page Instruction Sequence Diagram

### 9.2.18 Program Parameter Page (52h)

The Program Parameter Page instruction allows up to 256 bytes (128 words) to be programmed at memory word locations that have been previously erased to all 1s “FFFFh” (see Erase Parameter Page instruction). A Write Enable instruction must be executed before the device will accept the Program Parameter Page instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “52h” followed by a 24-bit address (A23-A0) and the full 256 data bytes, into the DI pin. Only the lower 8 address bits (A7-A0) are used, the 16 upper most address bit (A23-A8) are ignored (don’t care). Because the W25P80/16 programs in increments of one word (two bytes) at a time, the address must be an even address (A0 must equal 0). The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Program Parameter Page instruction sequence is shown in figure 20.

The start address of the needs to be set to 00h on the Parameter Page. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page. If previously written data bytes are over-written the data will not be valid.

In most applications it is best to read the full 256-byte contents of the page into a temporary RAM. Data can then be modified as needed and the entire 256 bytes can then be reprogrammed into the Parameter Page at one time.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Parameter Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of $t_{PP}$ (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Parameter Page instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, BP0) bits (see Status Register Memory Protection table).

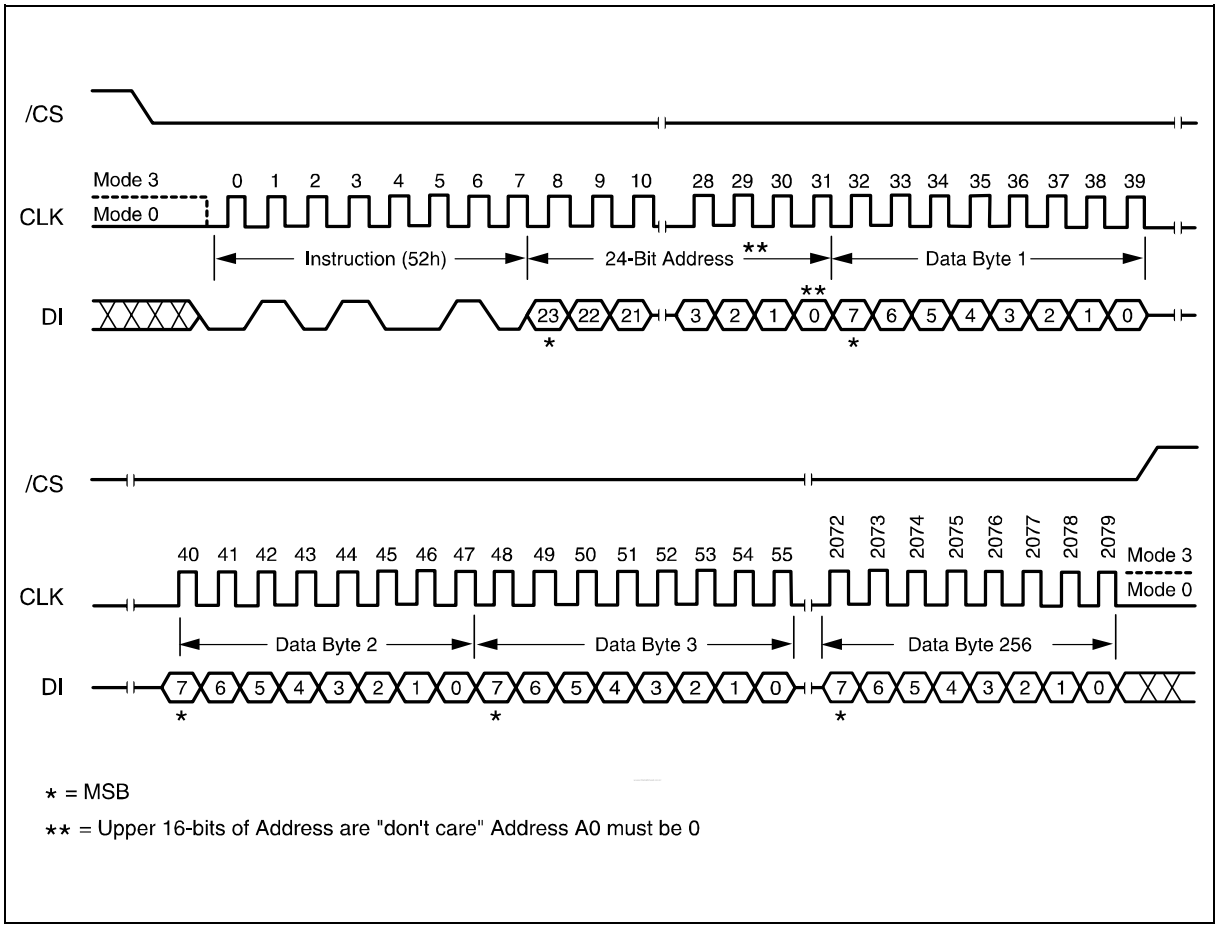



Figure 20. Parameter Page Program Instruction Sequence Diagram

### 9.2.19 Erase Parameter Page (D5h)

The Erase Parameter Page instruction sets all 256 bytes of memory in the Parameter Page to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Erase Parameter Page instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D5h”. The Erase Parameter Page instruction sequence is shown in figure 21.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Erase Parameter Page instruction will not be executed. After /CS is driven high, the self-timed Erase Parameter Page instruction will commence for a time duration of $t_{PE}$ (See AC Characteristics). While the Erase Parameter Page cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Erase Parameter Page cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Erase Parameter Page cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Erase Parameter Page instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, BP0) bits (see Status Register Memory Protection table).

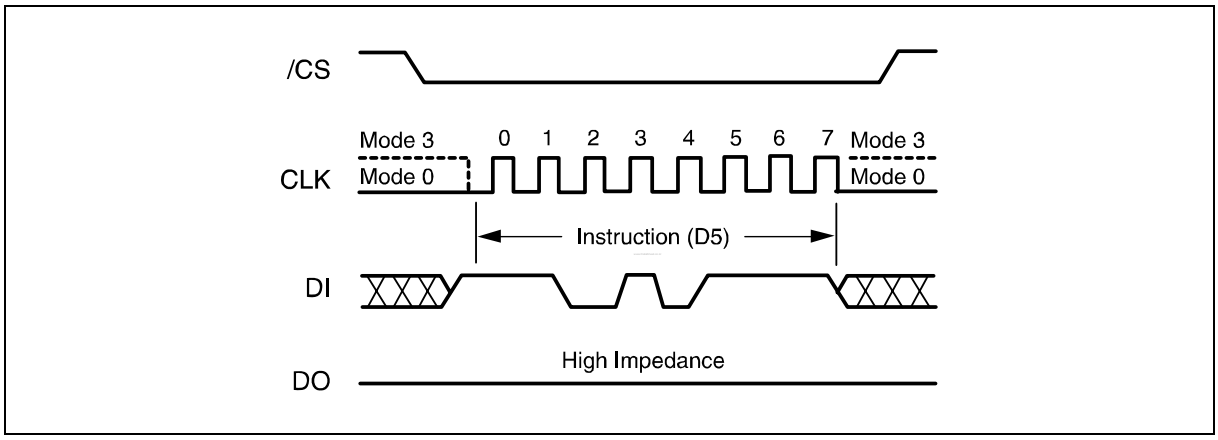



Figure 21. Parameter Page Erase Instruction Sequence Diagram

# 10. ELECTRICAL CHARACTERISTICS

## 10.1 Absolute Maximum Ratings (1)

| PARAMETERS | SYMBOL | CONDITIONS | RANGE | UNIT |
|---|---|---|---|---|
| Supply Voltage | VCC | | –0.6 to +4.0 | V |
| Voltage Applied to Any Pin | VIO | Relative to Ground | –0.6 to VCC +0.4 | V |
| Storage Temperature | TSTG | | –65 to +150 | °C |
| Lead Temperature | TLEAD | | See Note 2 | °C |
| Electrostatic Discharge Voltage | VESD | Human Body Model(3) | –2000 to +2000 | V |

**Notes:**

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

## 10.2 Operating Ranges

| PARAMETER | SYMBOL | CONDITIONS | SPEC | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Supply Voltage(1) | VCC | FR = 33MHz, fR = 25MHz | 2.7 | 3.6 | V |
| | | FR = 50MHz, fR = 25MHz | 3.0 | 3.6 | V |
| Ambient Temperature, Operating | TA | Industrial | –40 | +85 | °C |

**Note:**

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

## 10.3 Power-up Timing and Write Inhibit Threshold

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| VCC (min) to /CS Low | $t_{VSL}$(1) | 10 | | µs |
| Time Delay Before Write Instruction | $t_{PUW}$(1) | 1 | 10 | ms |
| Write Inhibit Threshold Voltage | $V_{WI}$(1) | 1 | 2 | V |

**Note:**

1. These parameters are characterized only.

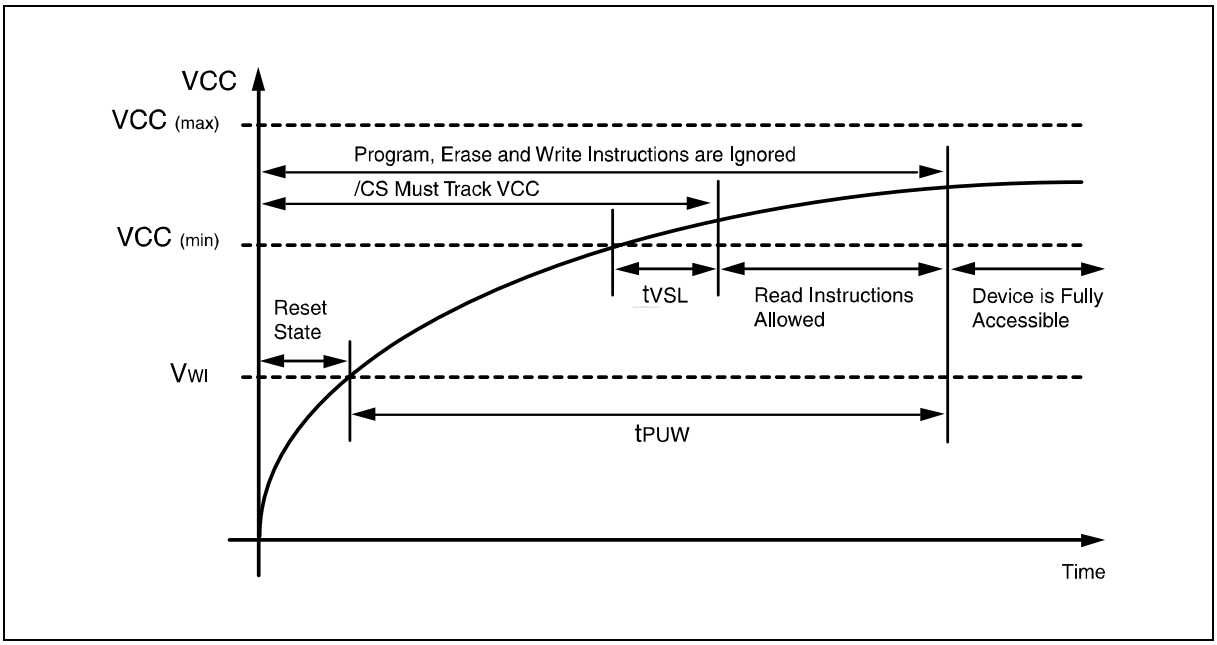



Figure 22. Power-up Timing and Voltage Levels

## 10.4 DC Electrical Characteristics (Preliminary)[1]

| PARAMETER | SYMBOL | CONDITIONS | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Input Capacitance | $C_{IN}$[2] | $V_{IN}$ = 0V[2] | | | 6 | pf |
| Output Capacitance | Cout[2] | $V_{OUT}$ = 0V[2] | | | 8 | pf |
| Input Leakage | $I_{LI}$ | | | | ±2 | µA |
| I/O Leakage | $I_{LO}$ | | | | ±2 | µA |
| Standby Current | $I_{CC1}$ | /CS = VCC,<br>VIN = GND or VCC | | 25 | 50 | µA |
| Power-down Current | $I_{CC2}$ | /CS = VCC,<br>VIN = GND or VCC | | <1 | 5 | µA |
| Current Read Data 1MHz[3] | $I_{CC3}$ | C = 0.1 VCC / 0.9 VCC<br>DO = Open | | 4 | 8 | mA |
| Current Read Data 20MHz[3] | | C = 0.1 VCC / 0.9 VCC<br>DO = Open | | 8 | 12 | mA |
| Current Read Data 33MHz[3] | | C = 0.1 VCC / 0.9 VCC<br>DO = Open | | 9 | 15 | mA |
| Current Page Program | $I_{CC4}$ | /CS = VCC | | 23 | 27 | mA |
| Current Write Status Register | $I_{CC5}$ | /CS = VCC | | 10 | 15 | mA |
| Current Sector Erase | $I_{CC6}$ | /CS = VCC | | 23 | 27 | mA |
| Current Chip Erase | $I_{CC7}$ | /CS = VCC | | 23 | 27 | mA |
| Input Low Voltage | $V_{IL}$ | | –0.5 | | VCC x0.3 | V |
| Input High Voltage | $V_{IH}$ | | VCC x0.7 | | VCC +0.4 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = –100 µA | VCC –0.2 | | | V |

**Notes:**

1 .See Preliminary Designation.

2. Tested on sample basis and specified through design and characterization data. TA=25° C, VCC 3V

3. Checker Board Pattern.

## 10.5 AC Measurement Conditions

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Load Capacitance | $C_L$ | 30 | 30 | pF |
| Input Rise and Fall Times | $T_R$, $T_F$ | | 5 | ns |
| Input Pulse Voltages | $V_{IN}$ | 0.2 VCC to | 0.8 VCC | V |
| Output Timing Reference Voltages | $O_{UT}$ | 0.3 VCC to | 0.7 VCC | V |

**Note:**

1. Output Hi-Z is defined as the point where data out is no longer driven.

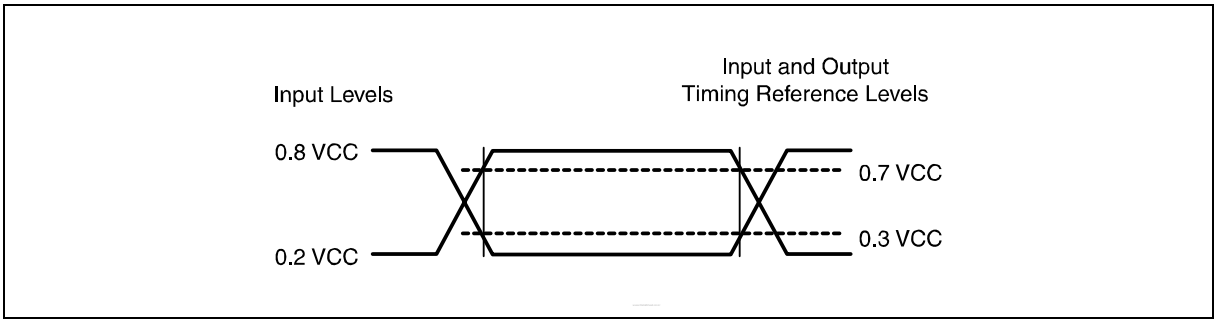



Figure 23. AC Measurement I/O Waveform

## 10.6 AC Electrical Characteristics

| DESCRIPTION | SYMBOL | ALT | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Clock frequency, for Fast Read (0Bh) and all other instructions except Read Data (03h)<br>2.7V-3.6V VCC<br>3.0V-3.6V VCC | $F_R$ | $f_C$ | <br>D.C.<br>D.C. | | <br>33<br>50 | <br>MHz<br>MHz |
| Clock freq. Read Data instruction 03h | $f_R$ | | D.C. | | 25 | MHz |
| Clock High, Low Time, for Fast Read (0Bh) and all other instructions except Read Data (03h) | $t_{CLH}$, $t_{CLL}$(1) | | 9 | | | ns |
| Clock High, Low Time for Read Data instruction | $t_{CRLH}$, $t_{CRLL}$(1) | | 9 | | | ns |
| Clock Rise Time peak to peak | $t_{CLCH}$(2) | | 0.1 | | | V/ns |
| Clock Fall Time peak to peak | $t_{CHCL}$(2) | | 0.1 | | | V/ns |
| /CS Active Setup Time relative to CLK | $t_{SLCH}$ | $t_{CSS}$ | 5 | | | ns |
| /CS Not Active Hold Time relative to CLK | $t_{CHSL}$ | | 5 | | | ns |
| Data In Setup Time | $t_{DVCH}$ | $t_{DSU}$ | 2 | | | ns |
| Data In Hold Time | $t_{CHDX}$ | $t_{DH}$ | 5 | | | ns |
| /CS Active Hold Time relative to CLK<br>(2.7V-3.6V / 3.0V-3.6V) | $t_{CHSH}$ | | 10/8 | | | ns |
| /CS Not Active Setup Time relative to CLK | $t_{SHCH}$ | | 5 | | | ns |
| /CS Deselect Time | $t_{SHSL}$ | $t_{CSH}$ | 100 | | | ns |
| Output Disable Time<br>(2.7V-3.6V / 3.0V-3.6V) | $t_{SHQZ}$(2) | $t_{DIS}$ | | | 12/10 | ns |
| Clock Low to Output Valid<br>(2.7V-3.6V / 3.0V-3.6V) | $t_{CLQV}$ | $t_V$ | | | 12/8 | ns |
| Output Hold Time | $t_{CLQX}$ | $t_{HO}$ | 0 | | | ns |
| /HOLD Active Setup Time relative to CLK<br>(2.7V-3.6V / 3.0V-3.6V) | $t_{HLCH}$ | | 5 | | | ns |
| /HOLD Active Hold Time relative to CLK | tchhh | | 5 | | | ns |

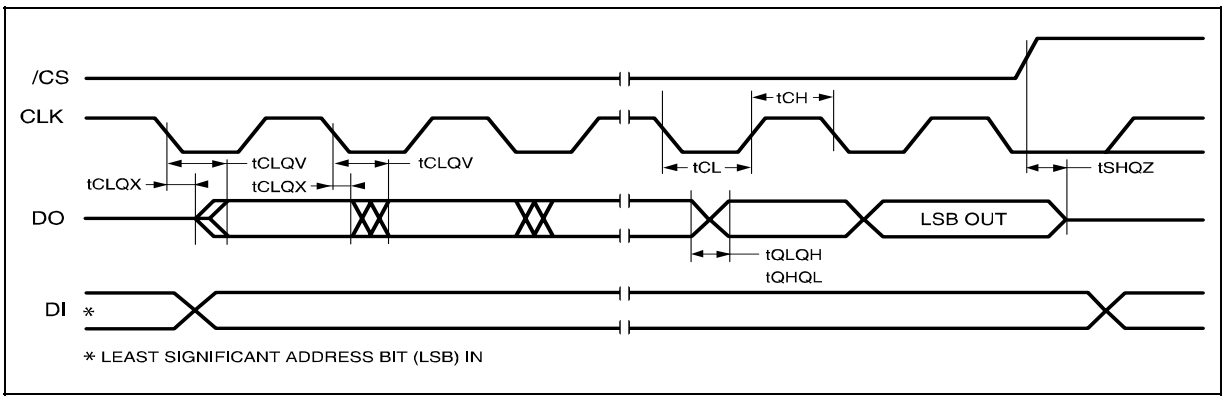
## AC Electrical Characteristics, continued

| DESCRIPTION | SYMBOL | ALT | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| /HOLD Not Active Setup Time relative to CLK | $t_{HHCH}$ | | 5 | | | ns |
| /HOLD Not Active Hold Time relative to CLK | $t_{CHHL}$ | | 5 | | | ns |
| /HOLD to Output Low-Z | $t_{HHQX}$[2] | $t_{LZ}$ | | | 9 | ns |
| /HOLD to Output High-Z | $t_{HLQZ}$[2] | $t_{HZ}$ | | | 9 | ns |
| Write Protect Setup Time Before /CS Low | $t_{WHSL}$[4] | | 20 | | | ns |
| Write Protect Hold Time After /CS High | $t_{SHWL}$[4] | | 100 | | | ns |
| /CS High to Power-down Mode | $t_{DP}$[2] | | | | 3 | µs |
| /CS High to Standby Mode without Electronic Signature Read | $t_{RES1}$[2] | | | | 30 | µs |
| /CS High to Standby Mode with Electronic Signature Read | $t_{RES2}$[2] | | | | 30 | µs |
| Write Status Register Cycle Time | $t_W$ | | | 17 | 25 | ms |
| Page Program Cycle Time [5]<br>3.0V-3.6V VCC<br>2.7V-3.6V VCC | $t_{PP}$ | | | <br>3.5<br>4 | <br>7<br>8 | <br>ms<br>ms |
| Sector Erase Cycle Time | $t_{SE}$ | | | 0.6 | 1.5 | s |
| Chip Erase Cycle Time W25P80<br>Chip Erase Cycle Time W25P16 | $t_{CE}$ | | | 7<br>12 | 15<br>25 | s<br>s |
| Parameter Page Erase Cycle Time | $t_{PE}$ | | | 100 | 200 | ms |

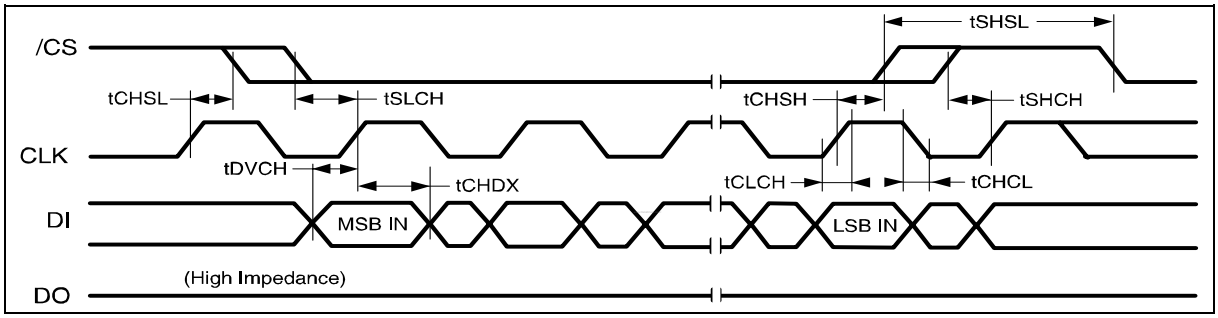
**Notes:**

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set at 1.
5. Maximum Tpp uses worse-case user pattern at 85°C.

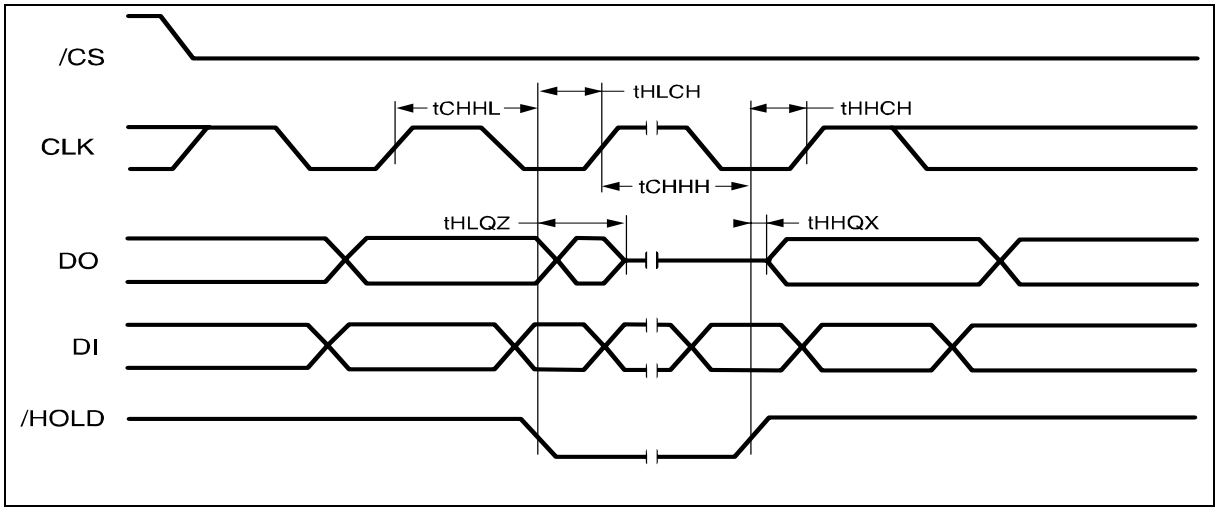
## 10.7 Serial Output Timing




## 10.8 Input Timing

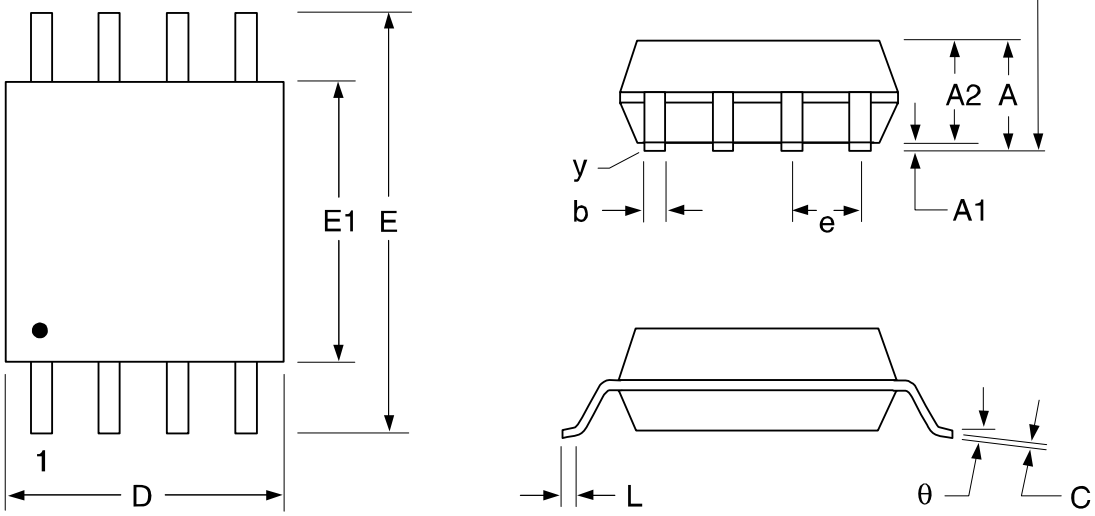



## 10.9 Hold Timing



## 11. PACKAGE SPECIFICATION

### 11.1 8-Pin SOIC 208-mil (Winbond Package Code SS)

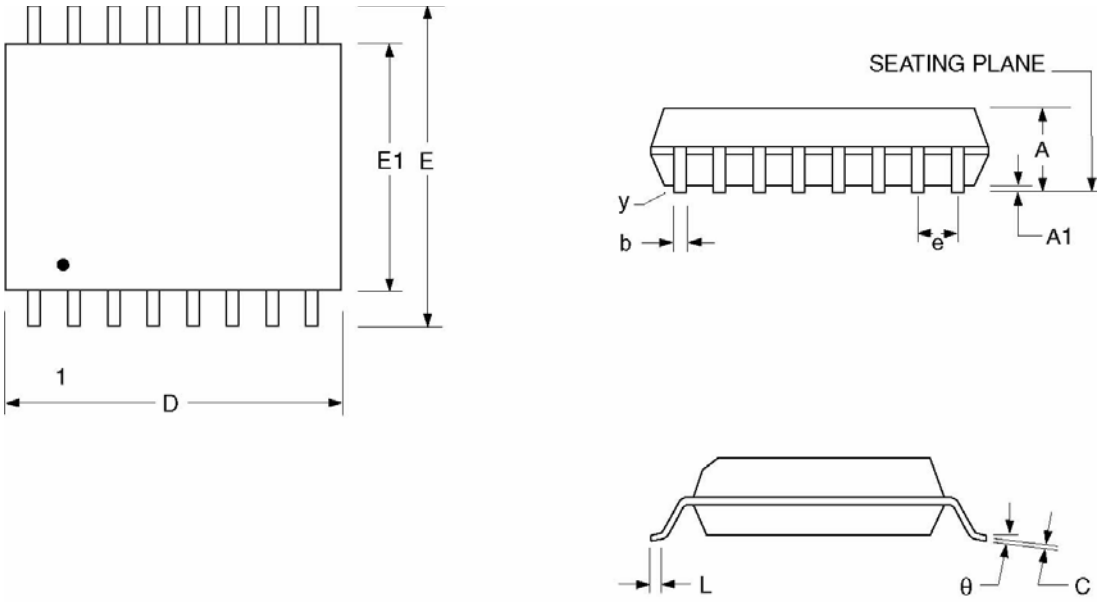



| SYMBOL | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.75 | 2.16 | 0.069 | 0.085 |
| A1 | 0.05 | 0.25 | 0.002 | 0.010 |
| A2 | 1.70 | 1.91 | 0.067 | 0.075 |
| b | 0.35 | 0.48 | 0.014 | 0.019 |
| C | 0.19 | 0.25 | 0.007 | 0.010 |
| D | 5.18 | 5.38 | 0.204 | 0.212 |
| E | 7.70 | 8.10 | 0.303 | 0.319 |
| E1 | 5.18 | 5.38 | 0.204 | 0.212 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 0.50 | 0.80 | 0.020 | 0.031 |
| θ | 0° | 8° | 0° | 8° |
| y | --- | 0.10 | --- | 0.004 |

**Notes:**

1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.

## 11.2 16-Pin SOIC 300-mil (Winbond Package Code SF)




| SYMBOL | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.36 | 2.64 | 0.093 | 0.104 |
| A1 | 0.10 | 0.30 | 0.004 | 0.012 |
| b | 0.33 | 0.51 | 0.013 | 0.020 |
| C | 0.18 | 0.28 | 0.007 | 0.011 |
| D(3) | 10.08 | 10.49 | 0.397 | 0.413 |
| E | 10.01 | 10.64 | 0.394 | 0.419 |
| E1(3) | 7.39 | 7.59 | 0.291 | 0.299 |
| e(2) | 1.27 BSC | | 0.050 BSC | |
| L | 0.39 | 1.27 | 0.015 | 0.050 |
| θ | 0° | 8° | 0° | 8° |
| y | --- | 0.076 | --- | 0.003 |

**Notes:**

1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.

## 12. ORDERING INFORMATION [3]

x 25P xx V xx I xx..

**Winbond Company Prefix**

W = Winbond [1]
NX = NexFlash

**Product Family**

25P = spiFlash Serial Flash Memory

**Product Number / Density**

80 = 8M-bit
16 = 16M-bit

**Supply Voltage**

V = 2.7V to 3.6V

**Package Type** [2]

SS = 8-pin SOIC 208-mil (Winbond)
SF = 16-pin SOIC 300-mil (Winbond)
S = 8-pin SOIC 208-mil (NexFlash)
F = 16-pin SOIC 300-mil (NexFlash)

**Temperature Range**

I = Industrial (–40°C to +85°C)

**Special Options**

(Blank) = Standard Package
G = Green Package (Lead-Free, RoHS compliant)

1. The Winbond W25P80/16 are fully compatible with the previous NexFlash NX25P80/16 Serial Flash Memories. The "W" prefix is not included on the part marking.
2. Only the second letter is used for part marking.
3. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T), when placing orders

## 13. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A | 03/05/04 | | New Create |
| B | 03/24/04 | | MLP metal die pad notification; Under "Package Types," figure 1 and packaging information. |
| C | 04/19/04 | | Corrected timing diagrams for figure 16 (Read Manufacturer / Device ID Diagram) and figure 17 (Read JEDEC ID). Added 8x6mm MLP Package for W25P16. |
| D | 05/06/04 | | Corrected dimensions in Packaging Information section for 6x5mm and 8x6mm MLP. |
| E | 06/28/04 | | Changed 200-mil SOIC reference to 208-mil SOIC. Updated dimensional table for the 208milSOIC in the packaging information. Added 208milSOIC and removed 5x6mm MLP for W25P16. |
| F | 10/07/04 | | Added Parameter Page data to Features, Block Diagram (Figure 2), Status Register Memory Protection, Instruction Set and Manufacturer and Device Identification. Added Parameter Page timing diagrams (Figures 20, 21, 22 and 23). Updated FR, tCH AND tPE data in AC Electrical Characteristics |
| G | 04/22/05 | | Updated AC and DC parameters and package type descriptions. Removed 8-contact 6x5 and 8x6 MLP packages from document. Corrected data in Instruction Set. Updated package dimension symbols for compliance. |
| H | 06/14/05 | | Updated Important Notice |
| I | 06/28/05 | | Changed NexFlash part numbers to Winbond part numbers and updated ordering and contact information |
| J | 12/11/05 | ALL | Updated data sheet to comply with Winbond standard.<br>Updated FR and fR values in Operating Ranges Table and AC Characteristics Table. Updated Read Data (fR) values in Operating Range and AC Characteristics Tables from 33MHz to 25MHz.<br>Corrected the pin assignment on table of pin description of page 5. |
| K | 08/01/06 | ALL | Removed 25P32, see 25X32 data sheet for 32Mb density<br>Updated ICC1 to ICC 7 specs. |
| L | 09/22/06 | 15 & 41 | Corrected Write Enable/Disable text.<br>Added footnotes in the ordering information table. |

## Preliminary Designation

The "Preliminary" designation on a *Winbond* data sheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *Winbond* or an authorized sales representative should be consulted for current information before using this product.

## Trademarks

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**Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.**

NEXFLASH® Technologies, Inc.

The Winbond W25P80/16 are fully compatible with the previous NexFlash NX25P80/16 Serial Flash memories.

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