

## Features

- Fast Read Access Time - 90 ns
- Low Power CMOS Operation
  - 100  $\mu$ A max. Standby
  - 40 mA max. Active at 5 MHz
- JEDEC Standard Packages
  - 32 Lead PLCC
  - 32-Lead 600-mil PDIP and Cerdip
  - 32-Lead 450-mil SOIC (SOP)
  - 32-Lead TSOP
- 5V  $\pm$  10% Supply
- High-Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 50  $\mu$ s/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Industrial and Commercial Temperature Ranges

## Description

The AT27C080 chip is a low-power, high-performance 8,388,608-bit ultraviolet erasable programmable read only memory (EPROM) organized as 1M by 8 bits. The AT27C080 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 90 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

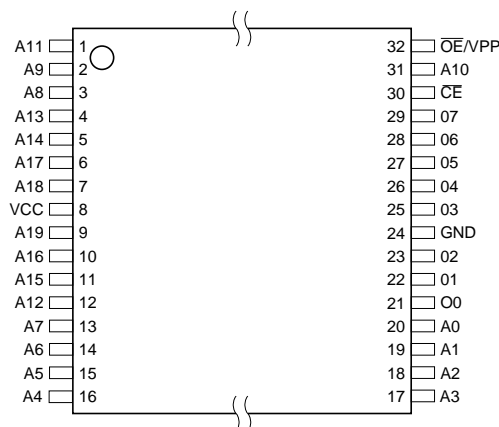
Atmel's scaled CMOS technology provides low active power consumption and fast programming. Power consumption is typically 10 mA in active mode and less than 10  $\mu$ A in standby mode.

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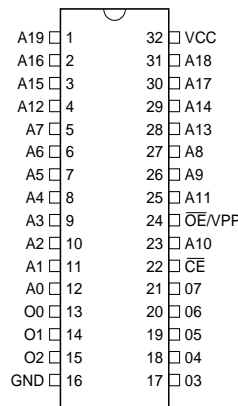
## Pin Configurations

Pin Name	Function
A0 - A19	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

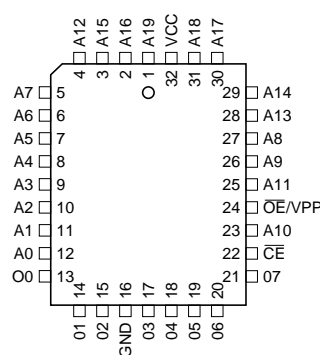
TSOP Top View  
Type 1



CDIP, PDIP, SOIC Top View



PLCC Top View



# 8-Megabit (1M x 8) UV Erasable CMOS EPROM

## AT27C080



The AT27C080 is available in a choice of packages, including; one-time programmable (OTP) plastic PLCC, PDIP, SOIC (SOP), and TSOP, as well as windowed ceramic Cerdip. All devices feature two-line control ( $\overline{CE}$ ,  $\overline{OE}$ ) to give designers the flexibility to prevent bus contention.

With high density 1M byte storage capability, the AT27C080 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C080 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50  $\mu$ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

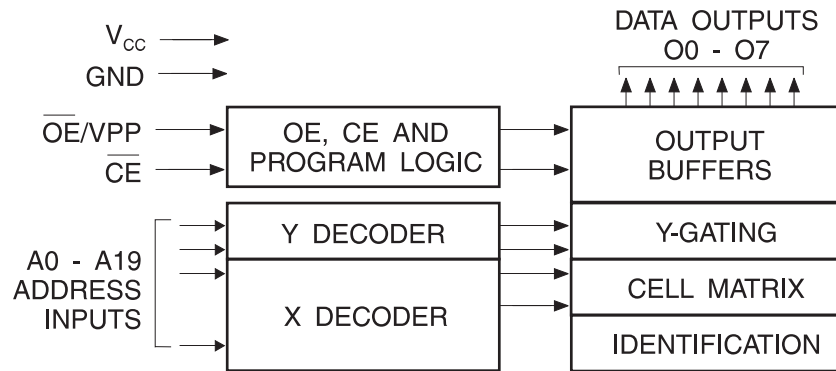
## Erase Characteristics

The entire memory array of the AT27C080 is erased (all outputs read as  $V_{OH}$ ) after exposure to ultraviolet light at a wavelength of 2,537Å. Complete erasure is assured after a minimum of 20 minutes of exposure using 12,000  $\mu$ W/cm<sup>2</sup> intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W.sec/cm<sup>2</sup>. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM that will be subjected to continuous fluorescent indoor lighting or sunlight.

## System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu$ F high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the  $V_{CC}$  and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu$ F bulk electrolytic capacitor should be utilized, again connected between the  $V_{CC}$  and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## Block Diagram



## Absolute Maximum Ratings\*

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
$V_{PP}$ Supply Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
Integrated UV Erase Dose.....	7258 W•sec/cm <sup>2</sup>

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC which may overshoot to +7.0V for pulses of less than 20 ns.

## Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	$A_i$	Outputs
Read	$V_{IL}$	$V_{IL}$	$A_i$	$D_{OUT}$
Output Disable	X	$V_{IH}$	$X^{(1)}$	High Z
Standby	$V_{IH}$	X	X	High Z
Rapid Program <sup>(2)</sup>	$V_{IL}$	$V_{PP}$	$A_i$	$D_{IN}$
PGM Verify	$V_{IL}$	$V_{IL}$	$A_i$	$D_{OUT}$
PGM Inhibit	$V_{IH}$	$V_{PP}$	X	High Z
Product Identification <sup>(4)</sup>	$V_{IL}$	$V_{IL}$	$A_9 = V_H^{(3)}$ $A_0 = V_{IH}$ or $V_{IL}$ $A_1 - A_{19} = V_{IL}$	Identification Code

- Notes: 1. X can be  $V_{IL}$  or  $V_{IH}$ .  
 2. Refer to Programming Characteristics.  
 3.  $V_H = 12.0 \pm 0.5V$ .  
 4. Two identifier bytes may be selected. All  $A_i$  inputs are held low ( $V_{IL}$ ), except  $A_9$  which is set to  $V_H$  and  $A_0$  which is toggled low ( $V_{IL}$ ) to select the Manufacturer's Identification byte and high ( $V_{IH}$ ) to select the Device Code byte.



## DC and AC Operating Conditions for Read Operation

		AT27C080			
		-90	-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V <sub>CC</sub> Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

## DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> (Com., Ind.)		±1.0	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub> (Com., Ind.)		±5.0	μA
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	I <sub>SB1</sub> (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I <sub>SB2</sub> (TTL), $\overline{CE} = 2.0$ to V <sub>CC</sub> + 0.5V		1.0	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz, I <sub>OUT</sub> = 0 mA, $\overline{CE} = V_{IL}$		40	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V

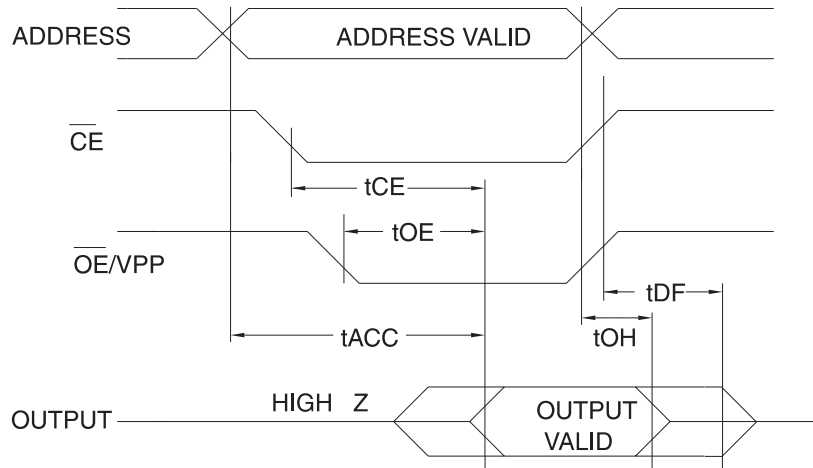
Note: 1. V<sub>CC</sub> must be applied simultaneously or before  $\overline{OE}/V_{PP}$ , and removed simultaneously or after  $\overline{OE}/V_{PP}$ .

## AC Characteristics for Read Operation

Symbol	Parameter	Condition	AT27C080								Units
			-90		-10		-12		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>ACC</sub> <sup>(4)</sup>	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		90		100		120		150	ns
t <sub>CE</sub> <sup>(3)</sup>	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		90		100		120		150	ns
t <sub>OE</sub> <sup>(3)(4)</sup>	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		20		20		30		35	ns
t <sub>DF</sub> <sup>(2)(5)</sup>	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		30		35		40	ns
t <sub>OH</sub>	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ whichever occurred first		0		0		0		0		ns

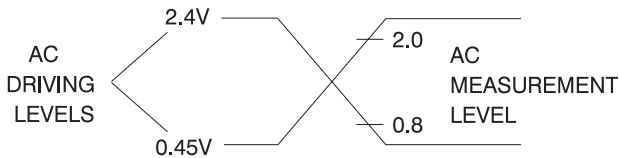
Note: 2, 3, 4, 5. See AC Waveforms for Read Operation.

## AC Waveforms for Read Operation<sup>(1)</sup>



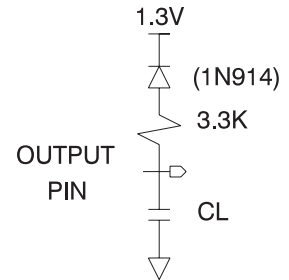
- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
  2.  $t_{DF}$  is specified from OE/VPP or CE, whichever occurs first. Output float is defined as the point when data is no longer driven.
  3.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
  4.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
  5. This parameter is only sampled and is not 100% tested.

## Input Test Waveform and Measurement Levels



$t_R, t_F < 20$  ns (10% to 90%)

## Output Test Load



- Note: 1.  $CL = 100$  pF including jig capacitance.

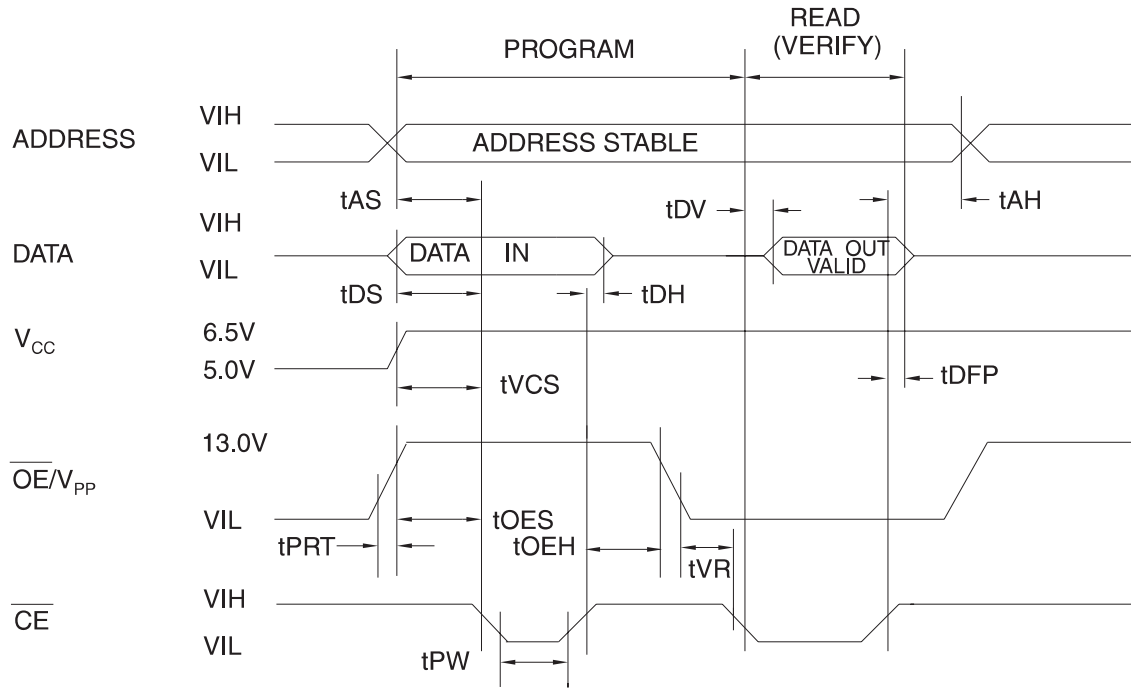
## Pin Capacitance

$f = 1$  MHz,  $T = 25^\circ\text{C}$ <sup>(1)</sup>

	Typ	Max	Units	Conditions
$C_{IN}$	4	8	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

- Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## Programming Waveforms



- Notes:
1. The Input Timing reference is 0.8V for  $V_{IL}$  and 2.0V for  $V_{IH}$ .
  2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device but must be accommodated by the programmer.

## DC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $\overline{OE}/V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$I_{LI}$	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		$\pm 10$	$\mu\text{A}$
$V_{IL}$	Input Low Level		-0.6	0.8	V
$V_{IH}$	Input High Level		2.0	$V_{CC} + 1.0$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1 \text{ mA}$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -400 \mu\text{A}$	2.4		V
$I_{CC2}$	$V_{CC}$ Supply Current (Program and Verify)			40	mA
$I_{PP2}$	$\overline{OE}/V_{PP}$ Supply Current	$\overline{CE} = V_{IL}$		25	mA
$V_{ID}$	A9 Product Identification Voltage		11.5	12.5	V

## AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $\overline{\text{OE}}/V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Limits		Units
			Min	Max	
$t_{AS}$	Address Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns.	2.0		$\mu\text{s}$
$t_{OES}$	$\overline{\text{OE}}/V_{PP}$ Setup Time		2.0		$\mu\text{s}$
$t_{OEH}$	$\overline{\text{OE}}/V_{PP}$ Hold Time		2.0		$\mu\text{s}$
$t_{DS}$	Data Setup Time		2.0		$\mu\text{s}$
$t_{AH}$	Address Hold Time	Input Pulse Levels: 0.45V to 2.4V	0.0		$\mu\text{s}$
$t_{DH}$	Data Hold Time		2.0		$\mu\text{s}$
$t_{DFP}$	$\overline{\text{CE}}$ High to Output Float Delay <sup>(2)</sup>	Input Timing Reference Level: 0.8V to 2.0V	0.0	130	ns
$t_{VCS}$	$V_{CC}$ Setup Time		2.0		$\mu\text{s}$
$t_{PW}$	$\overline{\text{CE}}$ Program Pulse Width <sup>(3)</sup>	Output Timing Reference Level: 0.8V to 2.0V	47.5	52.5	$\mu\text{s}$
$t_{DV}$	Data Valid from $\overline{\text{CE}}$			1.0	$\mu\text{s}$
$t_{VR}$	$\overline{\text{OE}}/V_{PP}$ Recovery Time		2.0		ns
$t_{PRT}$	$\overline{\text{OE}}/V_{PP}$ Pulse Rise Time During Programming		50		ns

- Notes:
- $V_{CC}$  must be applied simultaneously or before  $\overline{\text{OE}}/V_{PP}$  and removed simultaneously or after  $\overline{\text{OE}}/V_{PP}$ .
  - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
  - Program Pulse width tolerance is  $50 \mu\text{s} \pm 5\%$ .

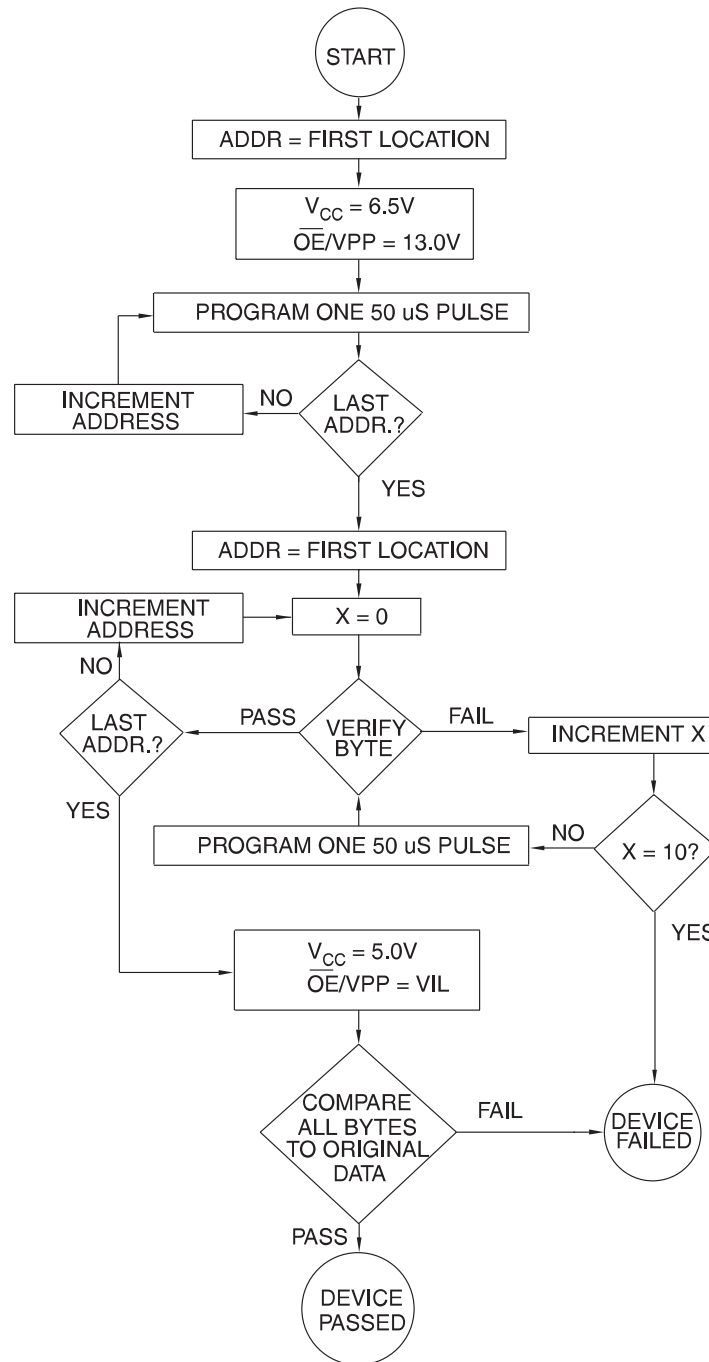
## Atmel's 27C080 Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	0	1	0	8A

## Rapid Programming Algorithm

A 50  $\mu\text{s}$   $\overline{\text{CE}}$  pulse width is used to program. The address is set to the first location.  $V_{\text{CC}}$  is raised to 6.5V and  $\overline{\text{OE}}/V_{\text{PP}}$  is raised to 13.0V. Each address is first programmed with one 50  $\mu\text{s}$   $\overline{\text{CE}}$  pulse without verification. Then a verification reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 50  $\mu\text{s}$  pulses are applied with a verification after each

pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $\overline{\text{OE}}/V_{\text{PP}}$  is then lowered to  $V_{\text{IL}}$  and  $V_{\text{CC}}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.





## Ordering Information

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	40	0.1	AT27C080-90DC AT27C080-90JC AT27C080-90PC AT27C080-90RC AT27C080-90TC	32DW6 32J 32P6 32R 32T	Commercial (0°C to 70°C)
	40	0.1	AT27C080-90DI AT27C080-90JI AT27C080-90PI AT27C080-90RI AT27C080-90TI	32DW6 32J 32P6 32R 32T	Industrial (-40°C to 85°C)
100	40	0.1	AT27C080-10DC AT27C080-10JC AT27C080-10PC AT27C080-10RC AT27C080-10TC	32DW6 32J 32P6 32R 32T	Commercial (0°C to 70°C)
	40	0.1	AT27C080-10DI AT27C080-10JI AT27C080-10PI AT27C080-10RI AT27C080-10TI	32DW6 32J 32P6 32R 32T	Industrial (-40°C to 85°C)

(continued)

Package Type	
<b>32DW6</b>	32-Lead, 0.600" Windowed, Ceramic Dual Inline Package (Cerdip)
<b>32J</b>	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
<b>32P6</b>	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
<b>32R</b>	32-Lead, 0.450" Wide, Plastic Gull Wing Small Outline (SOIC)
<b>32T</b>	32-Lead, Plastic Thin Small Outline Package (TSOP)



## Ordering Information (Continued)

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.1	AT27C080-12DC AT27C080-12JC AT27C080-12PC AT27C080-12RC AT27C080-12TC	32DW6 32J 32P6 32R 32T	Commercial (0°C to 70°C)
	40	0.1	AT27C080-12DI AT27C080-12JI AT27C080-12PI AT27C080-12RI AT27C080-12TI	32DW6 32J 32P6 32R 32T	Industrial (-40°C to 85°C)
150	40	0.1	AT27C080-15DC AT27C080-15JC AT27C080-15PC AT27C080-15RC AT27C080-15TC	32DW6 32J 32P6 32R 32T	Commercial (0°C to 70°C)
	40	0.1	AT27C080-15DI AT27C080-15JI AT27C080-15PI AT27C080-15RI AT27C080-15TI	32DW6 32J 32P6 32R 32T	Industrial (-40°C to 85°C)

Package Type	
<b>32DW6</b>	32-Lead, 0.600" Windowed, Ceramic Dual Inline Package (Cerdip)
<b>32J</b>	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
<b>32P6</b>	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
<b>32R</b>	32-Lead, 0.450" Wide, Plastic Gull Wing Small Outline (SOIC)
<b>32T</b>	32-Lead, Plastic Thin Small Outline Package (TSOP)