

128K (16K x 8) CMOS EPROM

FEATURES

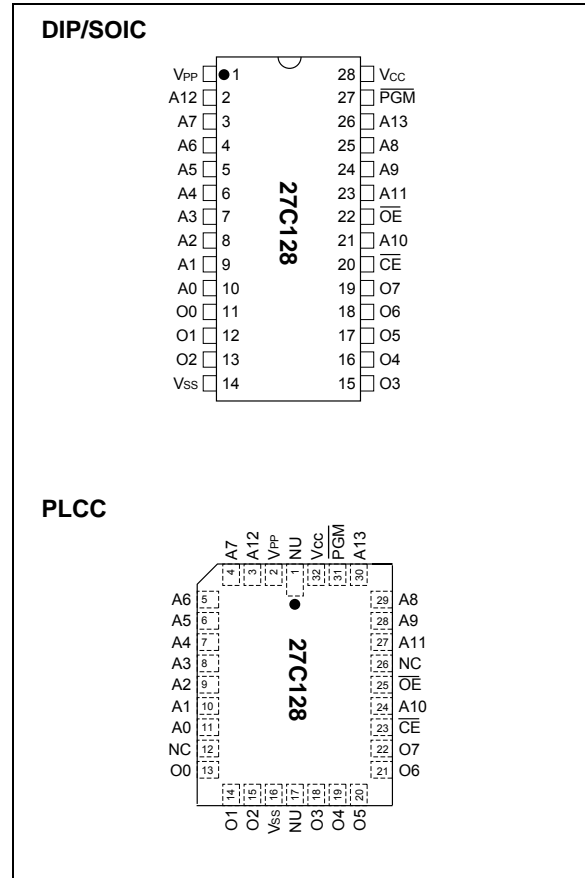
- High speed performance
 - 120 ns access time available
- CMOS Technology for low power consumption
 - 20 mA Active current
 - 100 μ A Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 16K x 8: JEDEC standard pinouts
 - 28-pin Dual-in-line package
 - 32-pin PLCC Package
 - 28-pin SOIC package
 - Tape and reel
- Available for the following temperature ranges:
 - Commercial: 0°C to +70°C
 - Industrial: -40°C to +85°C
 - Automotive: -40°C to +125°C

DESCRIPTION

The Microchip Technology Inc. 27C128 is a CMOS 128K bit (electrically) Programmable Read Only Memory. The device is organized as 16K words by 8 bits (16K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements. A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

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PACKAGE TYPES



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS -0.6V to +7.25V
 VPP voltage w.r.t. VSS during programming -0.6V to +14V
 Voltage on A9 w.r.t. VSS -0.6V to +13.5V
 Output voltage w.r.t. VSS -0.6V to VCC +1.0V
 Storage temperature -65°C to +150°C
 Ambient temp. with power applied -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A13	Address Inputs
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
\overline{PGM}	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V (±10%) Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Extended (Automotive): Tamb = -40°C to +125°C							
Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1"	V _{IH}	2.0	V _{CC} +1	V	
		Logic "0"	V _{IL}	-0.5	0.8	V	
Input Leakage	all	—	I _{LI}	-10	10	μA	V _{IN} = 0 to V _{CC}
Output Voltages	all	Logic "1"	V _{OH}	2.4		V	I _{OH} = -400 μA I _{OL} = 2.1 mA
		Logic "0"	V _{OL}		0.45	V	
Output Leakage	all	—	I _{LO}	-10	10	μA	V _{OUT} = 0V to V _{CC}
Input Capacitance	all	—	C _{IN}	—	6	pF	V _{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	C _{OUT}	—	12	pF	V _{OUT} = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input	I _{CC1}	—	20	mA	V _{CC} = 5.5V; V _{PP} = V _{CC} f = 1 MHz; $\overline{OE} = \overline{CE} = V_{IL}$; I _{OUT} = 0 mA; V _{IL} = -0.1 to 0.8V; V _{IH} = 2.0 to V _{CC} ; Note 1
		TTL input	I _{CC2}	—	25	mA	
Power Supply Current, Standby	C	TTL input	I _{CC} (s)	—	2	mA	$\overline{CE} = V_{CC} \pm 0.2V$
	I, E	TTL input		—	3	mA	
	all	CMOS input		—	100	μA	
IPP Read Current	all	Read Mode	I _{PP}		100	μA	V _{PP} = 5.5V
VPP Read Voltage	all	Read Mode	V _{PP}	V _{CC} -0.7	V _{CC}	V	

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

Parameter	Sym	AC Testing Waveform: $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$; $V_{OH} = 2.0V$ $V_{OL} = 0.8V$ Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ Industrial: $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ Extended (Automotive): $T_{amb} = -40^{\circ}C$ to $+125^{\circ}C$										Units	Conditions
		27C128-12		27C128-15		27C128-17		27C128-20		27C128-25			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}=\overline{OE}=V_{IL}$
\overline{CE} to Output Delay	tCE	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}=V_{IL}$
\overline{OE} to Output Delay	tOE	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}=V_{IL}$
\overline{CE} or \overline{OE} to O/P High Impedance	tOFF	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address \overline{CE} or \overline{OE} , whichever occurs first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS

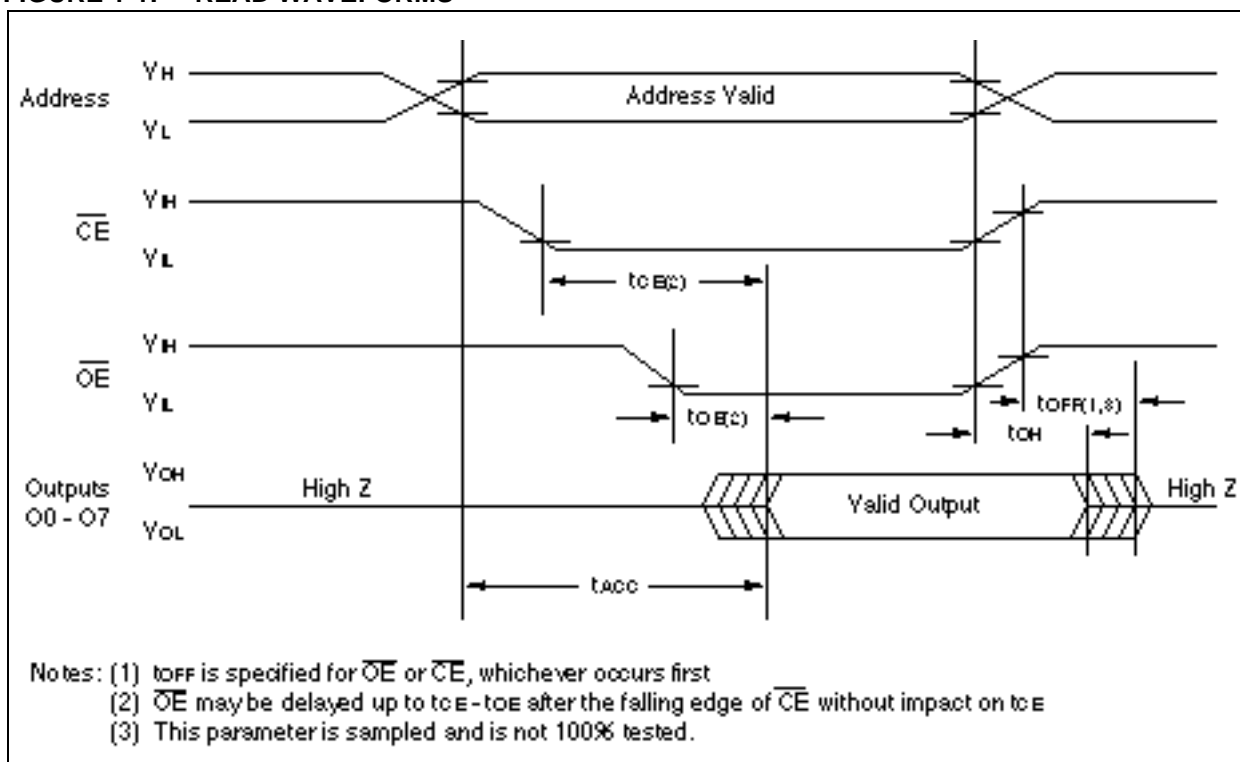


TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: $T_{amb} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC} = 6.5\text{V} \pm 0.25\text{V}$, $V_{PP} = 13.0\text{V} \pm 0.25\text{V}$						
Parameter	Status	Symbol	Min	Max.	Units	Conditions
Input Voltages	Logic"1"	V_{IH}	2.0	$V_{CC}+1$	V	
	Logic"0"	V_{IL}	-0.1	0.8	V	
Input Leakage	—	I_{LI}	-10	10	μA	$V_{IN} = 0\text{V to } V_{CC}$
Output Voltages	Logic"1"	V_{OH}	2.4	0.45	V	$I_{OH} = -400 \mu\text{A}$ $I_{OL} = 2.1 \text{mA}$
	Logic"0"	V_{OL}			V	
VCC Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
VPP Current, program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: $V_{IH}=2.4\text{V}$ and $V_{IL}=0.45\text{V}$; $V_{OH}=2.0\text{V}$; $V_{OL}=0.8\text{V}$ Ambient Temperature: $T_{amb}=25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC}= 6.5\text{V} \pm 0.25\text{V}$, $V_{PP} = V_H = 13.0\text{V} \pm 0.25\text{V}$				
Parameter	Symbol	Min	Max	Units	Remarks	
Address Set-Up Time	tAS	2	—	μs		
Data Set-Up Time	tDS	2	—	μs		
Data Hold Time	tDH	2	—	μs		
Address Hold Time	tAH	0	—	μs		
Float Delay (2)	tDF	0	130	ns		
VCC Set-Up Time	tVCS	2	—	μs		
Program Pulse Width (1)	tPW	95	105	μs	100 μs typical	
$\overline{\text{CE}}$ Set-Up Time	tCES	2	—	μs		
$\overline{\text{OE}}$ Set-Up Time	tOES	2	—	μs		
VPP Set-Up Time	tVPS	2	—	μs		
Data Valid from $\overline{\text{OE}}$	tOE	—	100	ns		

Note 1: For express algorithm, initial programming width tolerance is 100 $\mu\text{s} \pm 5\%$.

2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)

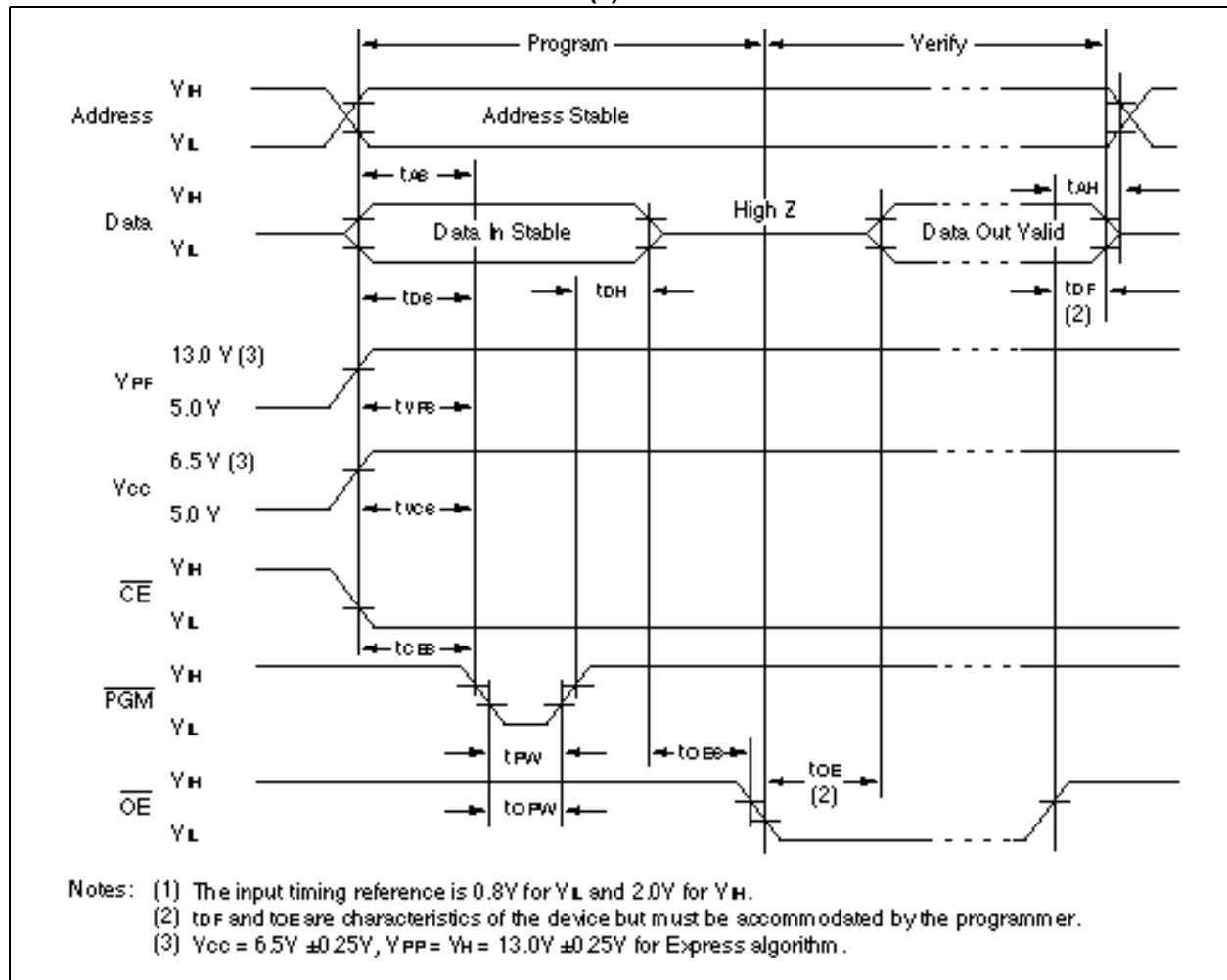


TABLE 1-6: MODES

Operation Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	V _{PP}	A ₉	O ₀ - O ₇
Read	V _{IL}	V _{IL}	V _{IH}	V _{CC}	X	DOUT
Program	V _{IL}	V _{IH}	V _{IL}	V _H	X	DIN
Program Verify	V _{IL}	V _{IL}	V _{IH}	V _H	X	DOUT
Program Inhibit	V _{IH}	X	X	V _H	X	High Z
Standby	V _{IH}	X	X	V _{CC}	X	High Z
Output Disable	V _{IL}	V _{IH}	V _{IH}	V _{CC}	X	High Z
Identity	V _{IL}	V _{IL}	V _{IH}	V _{CC}	V _H	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

- the $\overline{\text{CE}}$ pin is low to power up (enable) the chip
- the $\overline{\text{OE}}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{\text{OE}}$ (t_{OE}).

1.3 Standby Mode

The standby mode is defined when the \overline{CE} pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 μ A.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The \overline{OE} and \overline{PGM} pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 μ W/cm² for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

- VCC is brought to the proper voltage,
- VPP is brought to the proper VH level,
- the \overline{CE} pin is low,
- the \overline{OE} pin is high, and
- the \overline{PGM} pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A13 and the data to be programmed is presented to pins O0-O7. When data and address are stable, \overline{OE} is high, \overline{CE} is low and a low-going pulse on the \overline{PGM} line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

- VCC is at the proper level,
- VPP is at the proper VH level,
- the \overline{CE} line is low,
- the \overline{PGM} line is high, and
- the \overline{OE} line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only \overline{CE} or \overline{PGM} need be under separate control to each device. By pulsing the \overline{CE} or \overline{PGM} line low on a particular device in conjunction with the \overline{PGM} or \overline{CE} line low, that device will be programmed; all other devices with \overline{CE} or \overline{PGM} held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on \overline{CE} or \overline{PGM}); and the device is inhibited from programming.

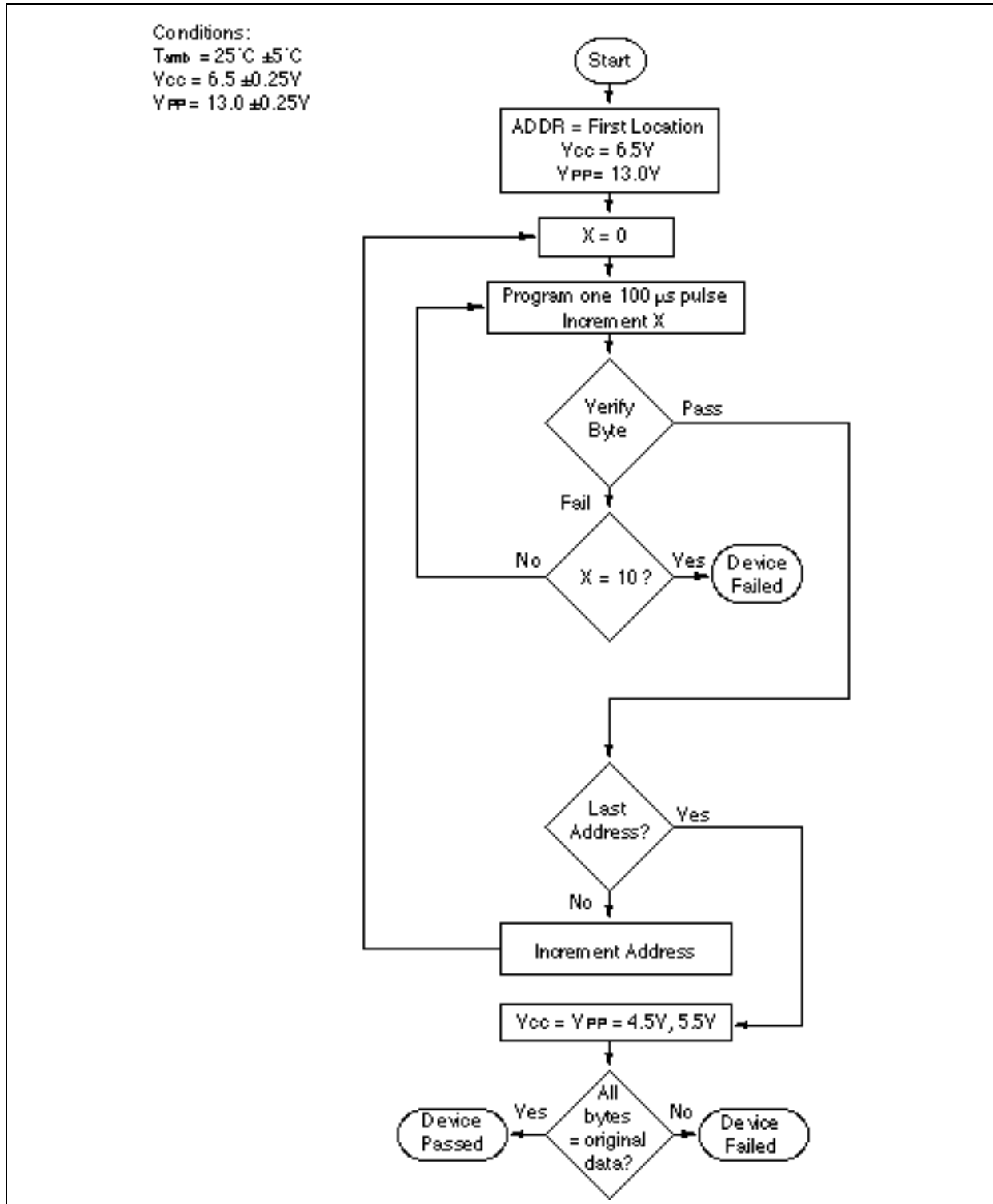
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The \overline{CE} and \overline{OE} lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin \rightarrow	Input	Output								
Identity \downarrow	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	H e x
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	0	0	1	1	83

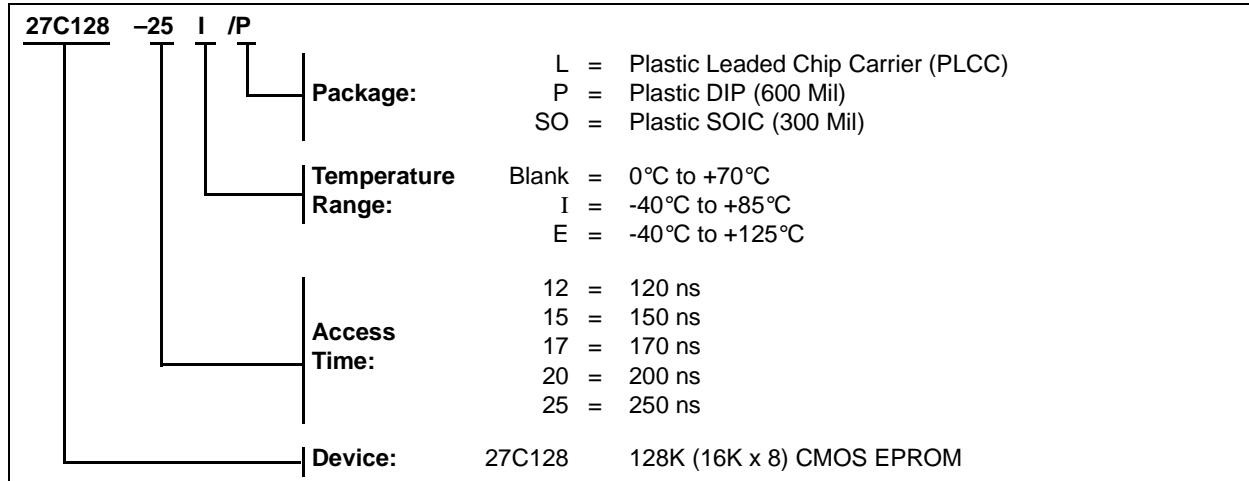
* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C128 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: www.microchip.com

Atlanta

3780 Mansell Road, Suite 130
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Tel: 770-640-0034
Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
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Fax: 630-285-0075

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Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, IN 46902
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Fax: 765-864-8387

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25950 Acero St., Suite 200
Mission Viejo, CA 92691
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Fax: 949-462-9608

San Jose

1300 Terra Bella Avenue
Mountain View, CA 94043
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Fax: 650-961-0286

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Unit 32 41 Rawson Street
Epping 2121, NSW
Sydney, Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Unit 706B
Wan Tai Bei Hai Bldg.
No. 6 Chaoyangmen Bei Str.
Beijing, 100027, China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu

Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou

Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR

Unit 901-6, Tower 2, Metroplaza
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Kwai Fong, N.T., Hong Kong
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Fax: 852-2401-3431

China - Shanghai

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Far East International Plaza
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Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen

Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde

Room 401, Hongjian Building, No. 2
Fengxiangnan Road, Ronggui Town, Shunde
District, Foshan City, Guangdong 528303, China
Tel: 86-757-28395507 Fax: 86-757-28395571

China - Qingdao

Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India

Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessey Road
Bangalore, 560 025, India
Tel: 91-80-22290061 Fax: 91-80-22290062

Japan

Yusen Shin Yokohama Building 10F
3-17-2, Shin Yokohama, Kohoku-ku,
Yokohama, Kanagawa, 222-0033, Japan
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Korea

168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
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Taiwan

Kaohsiung Branch
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Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4816
Fax: 886-7-536-4817

Taiwan

Taiwan Branch
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Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

Taiwan

Taiwan Branch
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Hsinchu City 300, Taiwan
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Germany

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Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy

Via Salvatore Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands

Waegenburghtplein 4
NL-5152 JR, Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom

505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820