27C512
512K (64K x 8) CHMOS EPROM

- **Software Carrier Capability**
- **120 ns Access Time**
- **Two-Line Control**
- **Int$_e$ligent Identifier™ Mode**
  — Automated Programming Operations
- **CMOS and TTL Compatible**
- **Low Power**
  — 30 mA Max. Active
  — 100 μA Max. Standby
- **Fast Programming**
  — Quick-Pulse Programming™ Algorithm
  — Programming Time as Fast as 8 Seconds

The Intel 27C512 is a 5V-only, 524, 288-bit Erasable Programmable Read Only Memory (EPROM), organized as 65,536 words of 8 bits. Individual bytes are accessed in 120 ns. This ensures compatibility with high-performance microprocessors, such as the Intel 12 MHz iAPX 286, allowing full speed operation without the addition of performance-degrading WAIT states. The 27C512 is also directly compatible with Intel's 80C51 family of microcontrollers.

The 27C512 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the 27C512's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabyte addressing capability provides designers with opportunities to engineer user-friendly, high-reliability, high-performance systems.

The 27C512's large storage capability of 64 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27C512 directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

Intel's Quick-Pulse Programming™ algorithm enables the 27C512 to be programmed as fast as eight seconds (plus programmer overhead). Programming equipment which takes advantage of the int$_e$ligent Identifier™ will electronically identify the EPROM and automatically program it using a superior programming method.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of the 27C512. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

CHMOS is a patented process of Intel Corporation.

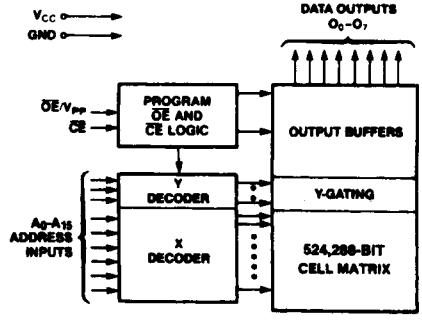

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Figure 1. Block Diagram

October 1990
Order Number: 290228-003

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family receives additional processing to enhance product characteristics. EXPRESS processing is available for several densities allowing the appropriate memory size to match system requirements. EXPRESS EPROMs are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This processing meets or exceeds most industry burn-in specifications. The EXPRESS product family is available in both 0°C to 70°C and −40°C to 85°C operating temperature range versions. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

EXPRESS EPROM FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to 70°C	168 ± 8
T	−40°C to 85°C	None
L	−40°C to 85°C	168 ± 8

OPTIONS

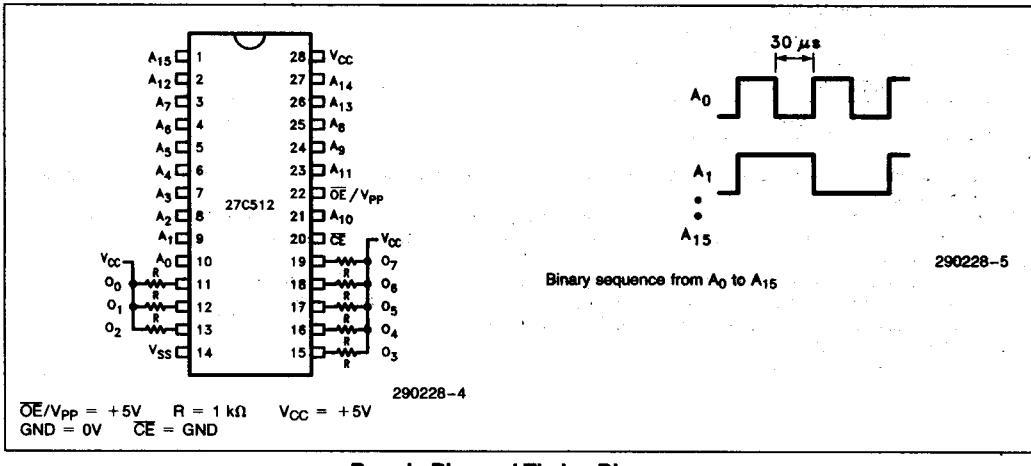
Packaging	
Speed	CERDIP
−120V10	Q, T, L

READ OPERATION DC CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27C512(2) LD27C512		Test Condition
		Min	Max	
I_{CC}(1)	V_{CC} Operating Current (mA)		50	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V_{CC} Operating Current at High Temperature (mA)		50	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$ $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.
2. D refers to the CERDIP package.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C(1)

Temperature Under Bias . . . . . −10°C to +80°C

Storage Temperature . . . . . −65°C to +125°C

All Input or Output Voltages (except A_9, V_{CC} and V_{PP}) with Respect to GND . . . . . −2.0V to 7.0V(2)

Voltage on A_9 with Respect to GND . . . . . −2.0V to 13.5V(2)

V_{PP} Supply Voltage with Respect to GND . . . . . −2.0V to 14V(2)

V_{CC} Supply Voltage with Respect to GND . . . . . −2.0V to 7.0V(2)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	V_{IN} = 0V to +5.5V
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to +5.5V
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE}$ = V_{IH}
					100	µA	$\overline{CE}$ = V_{CC} ±0.2V
I_{CC}	V_{CC} Operating Current	3			30	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA
I_{PP}	V_{PP} Operating Current	3			10	µA	V_{PP} = V_{CC}
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA

NOTES:

1. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS versions.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum I_{PP} + I_{CC}. Maximum current value is with outputs O_0 to O_7 unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
6. Sampled, not 100% tested.
7. Typical limits are at V_{CC} = 5V, T_A = 25°C.

READ OPERATION AC CHARACTERISTICS V_{CC} = 5.0V ±10%

Versions(4)	V_{CC} ± 10%		27C512-120V10		27C512-150V10		27C512-200V10		Unit
Symbol	Parameter	Notes	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		120		150		200	ns
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay	2		55		60		70	ns
t_{DF}	$\overline{OE}/V_{PP}$ High to Output High Z	3	0	30	0	50	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First	3	0		0		0		ns

NOTES:
1. See AC input/output reference waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. Packaging Options: No Prefix = CERDIP.
5. Typical values are for T_A = 25°C and nominal supply voltages.

CAPACITANCE(3) T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ(5)	Max	Unit	Condition
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{OE}/V_{PP}	$\overline{OE}/V_{PP}$ Capacitance	18	25	pF	V_{IN} = 0V

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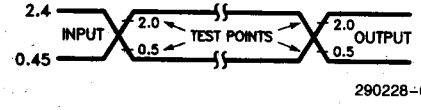
AC INPUT/OUTPUT REFERENCE WAVEFORM



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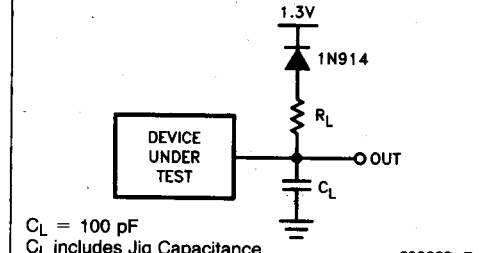
NOTE:
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤ 10 ns.

AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance
R_L = 3.3 kΩ

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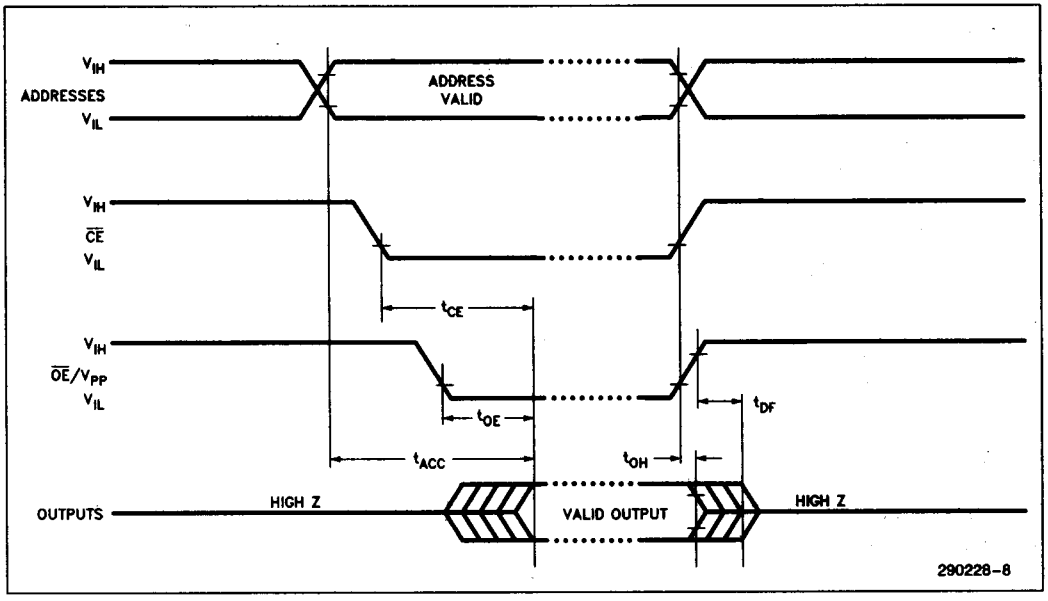
AC WAVEFORMS



DEVICE OPERATION

The Mode Selection table lists 27C512 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and $\overline{OE}/V_{PP}$, and A_9 during inteligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode	Notes	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	A_0	V_{CC}	Outputs
Read	1	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Standby		V_{IH}	X	X	X	V_{CC}	High Z
Program	2	V_{IL}	V_{PP}	X	X	V_{CP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	V_{CP}	D_{OUT}
Program Inhibit		V_{IH}	V_{PP}	X	X	V_{CP}	High Z
Inteligent Identifier — Manufacturer	2, 3	V_{IL}	V_{IL}	V_{ID}	V_{IL}	V_{CC}	89H
Inteligent Identifier — Device		V_{IL}	V_{IL}	V_{ID}	V_{IH}	V_{CC}	FDH

NOTES:
1. X can be V_{IH} or V_{IL}.
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{15} = V_{IL}.

Read Mode

The 27C512 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}/V_{PP}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}/V_{PP}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the outputs are in a high impedance state, independent of $\overline{OE}/V_{PP}$.

Two Line Output Control

EPROMS are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}/V_{PP}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Program Mode

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when $\overline{OE}/V_{PP}$ is raised to 12.75V. Data is introduced by applying an 8 bit word to the output pins. Pulsing $\overline{CE}$ low programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V, a substantial program margin is ensured. The verify is performed with $\overline{OE}/V_{PP}$ at V_{IL}. Valid data is available t_{DV} after $\overline{CE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}/V_{PP}$, parallel EPROMS may have common inputs.

Int$_e$ligent Identifier Mode

The Int$_e$ligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V ± 0.5V on A_9. With $\overline{CE}$, $\overline{OE}/V_{PP}$, A_1–A_8 and A_{10}–A_{15} at V_{IL}, A_0 = V_{IL} will present the manufacturer code and A_0 = V_{IH} the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by the falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

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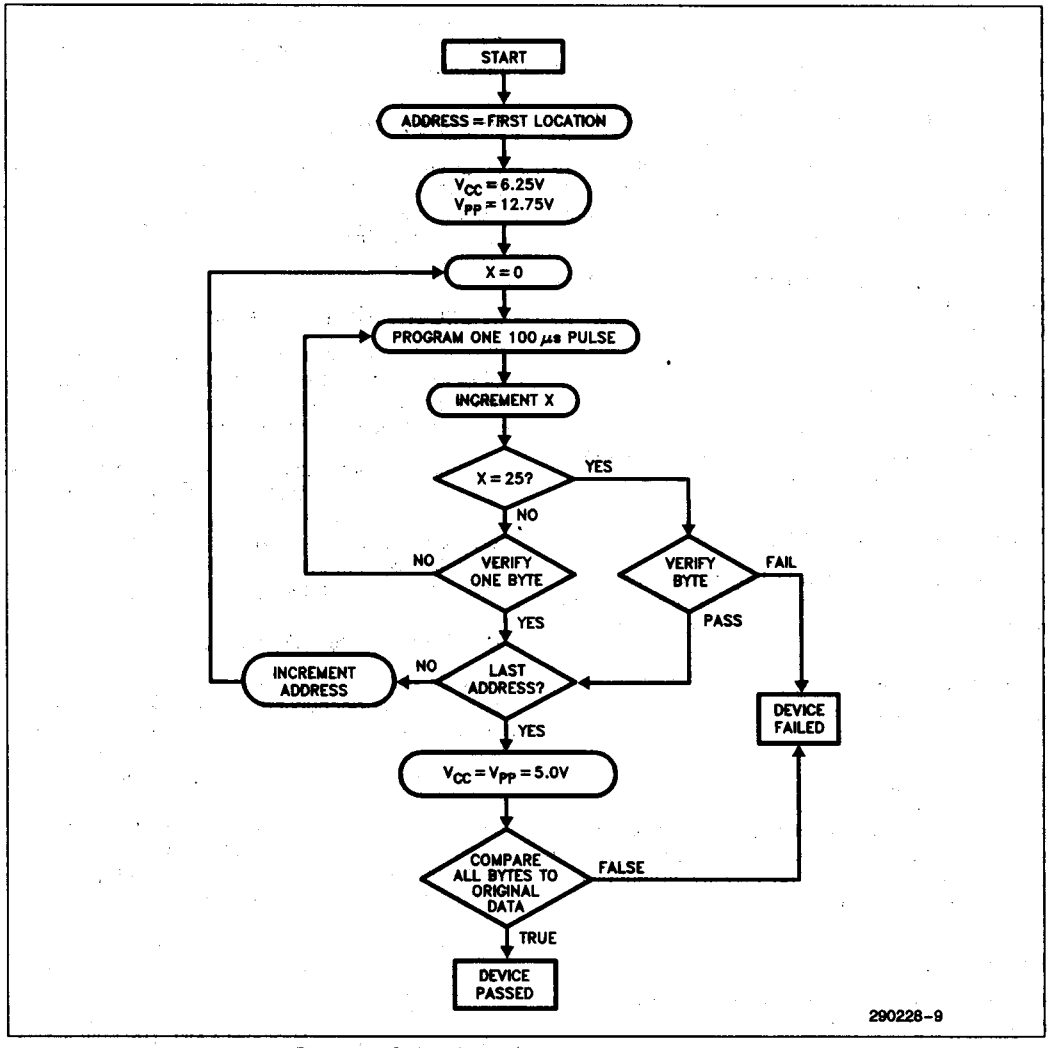

Figure 3. Quick-Pulse Programming Algorithm

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2).

Quick-Pulse Programming Algorithm

The Quick-Pulse Programming algorithm programs Intel's 27C512. Developed to substantially reduce programming throughput, this algorithm can program the 27C512 as fast as 8 seconds. Actual programming time depends on the programmer overhead.

The Quick-Pulse Programming algorithm employs a 100 μs pulse followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program pulse/byte verify sequence is performed with V_{CC} = 6.25V. $\overline{OE}/V_{PP}$ toggles between 12.75V and V_{IL} for program and verify operations. When programming is complete, all bytes are compared to the original data with V_{CC} = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25 \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			40	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 int$_e$ligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25 \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50			ns
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2, 3	2			μs
t_{PW}	$\overline{CE}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2			μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2			μs
t_{DV}	Data Valid from $\overline{CE}$	5			1	μs
t_{DFP}	Output Disable to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current value is with outputs O_0 to O_7 unloaded.
2. V_{CP} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
3. When programming, a 0.1 μF capacitor is required across $\overline{OE}/V_{PP}$ and GND to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveforms for timing measurements.
5. t_{DV} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

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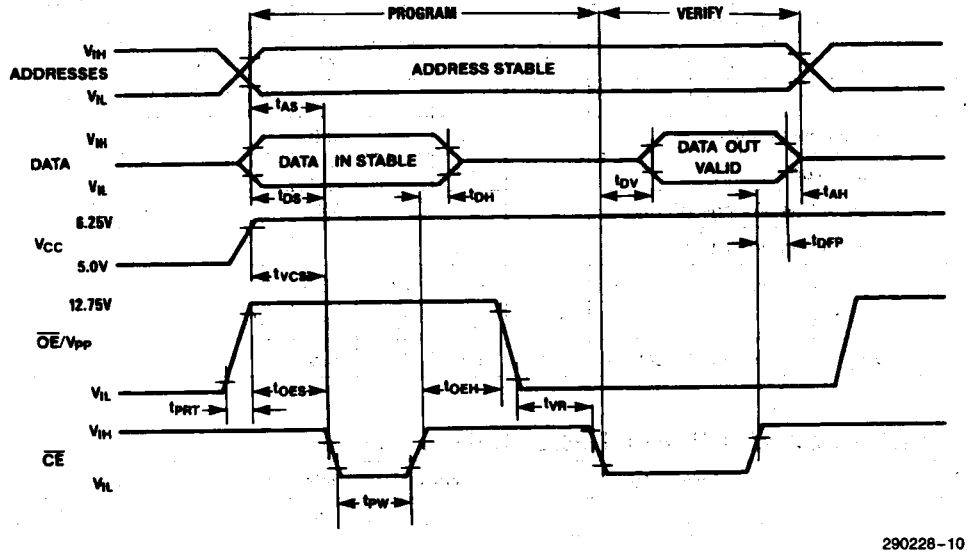
PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
003	Deleted preliminary classification.