



27C513 PAGE-ADDRESSED 512K (4 x 16K x 8) UV ERASABLE PROM

- **Paged Organization**
 - Reduced Physical Address Requirement
 - No Bank Switching Logic Needed
- **Software Carrier Capacity**
- **Automatic Page Clear**
 - Resets to Page 0 on Power Up and On Demand with \overline{RST} Signal
- **TTL and CMOS Compatible**
- **170 ns Access Time**
- **Two Line Control**
- **Low Power**
 - 30 mA max. Active
 - 100 μ A max. Standby
- **Compatible with Industry Standard EPROM Pinouts**
 - Direct 27128A Compatibility
 - 28-Pin Cerdip

The Intel 27C513 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory. It is organized as 4 pages of 16K 8-bit words. The 27C513's paged organization brings 64 Kbyte storage capacity to existing 128K EPROM-based designs and to popular 8-bit microprocessor or microcontroller systems that have 64 Kbyte total addressing capability. The 27C513 provides an ideal means of quadrupling current 16 Kbyte code space.

The 27C513's large storage capability of 64 Kbytes and 170 ns access time enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27C513 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

The 27C513 has an automatic page clear circuit for ease of use of the page-addressed organization. The page-select latch is automatically cleared to the lowest order page upon system power up.

Two-line control and industry standard 28-pin packaging are features common to all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27C513 is manufactured using Intel's 1 micron CHMOS* III-E technology.

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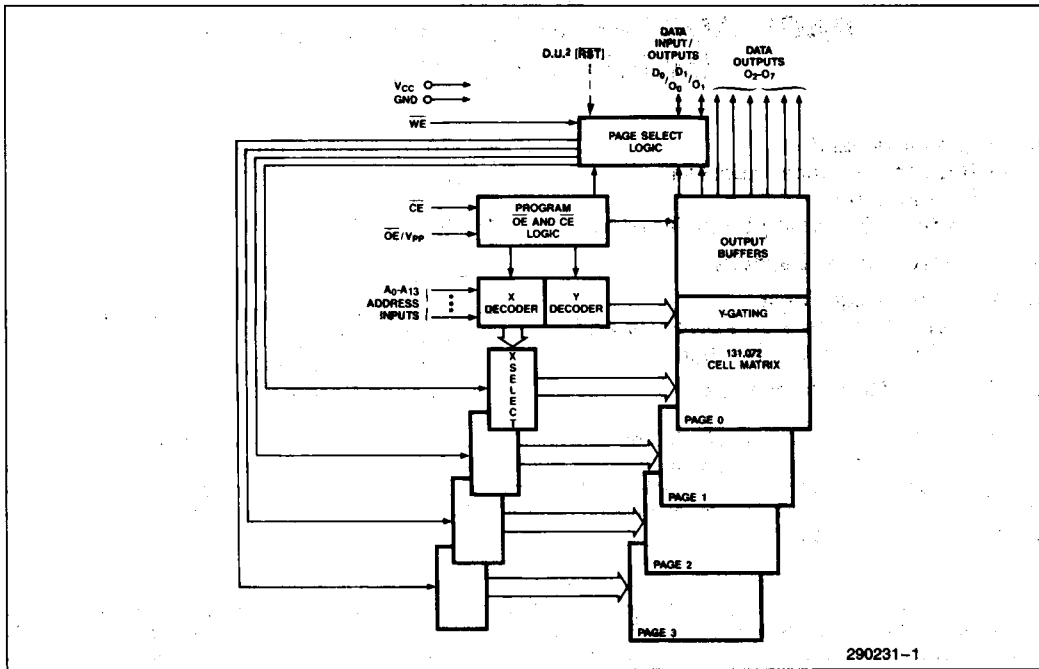


Figure 1. Block Diagram

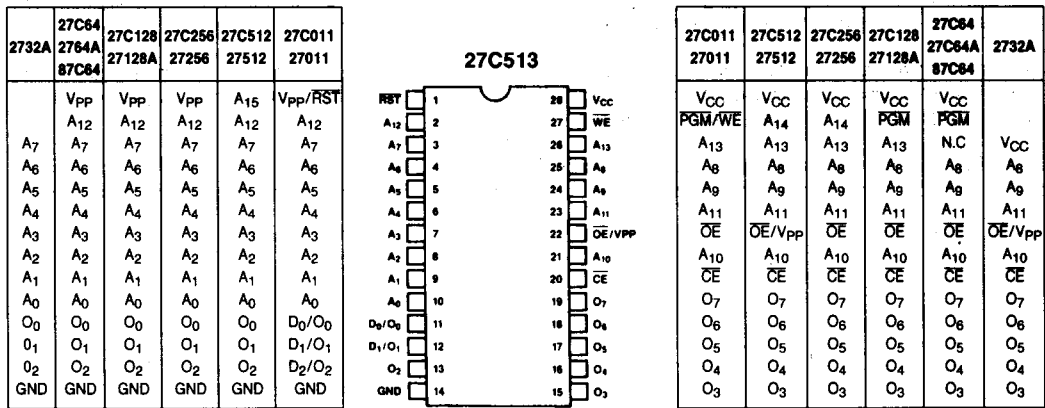


Figure 2. Pin Configuration

NOTES:

1. Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27C513 pins.

Pin Names

A ₀ -A ₁₅	Addresses
CE	Chip Enable
OE/V _{pp}	Output Enable/V _{pp}
WE	Page-Select Write Enable
O ₂ -O ₇	Outputs
D ₀ /O ₀ , D ₁ /O ₁	Input/Outputs
RST	Page Reset

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are

available with 168 ± 8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (-40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.15 electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ± 8
T	-40°C to +85°C	None
L	-40°C to +85°C	168 ± 8

EXPRESS OPTIONS

27C513 VERSIONS

Packaging Options	
Speed Versions	Cerddip
-200V10	Q, T, L

READ OPERATION

DC CHARACTERISTICS

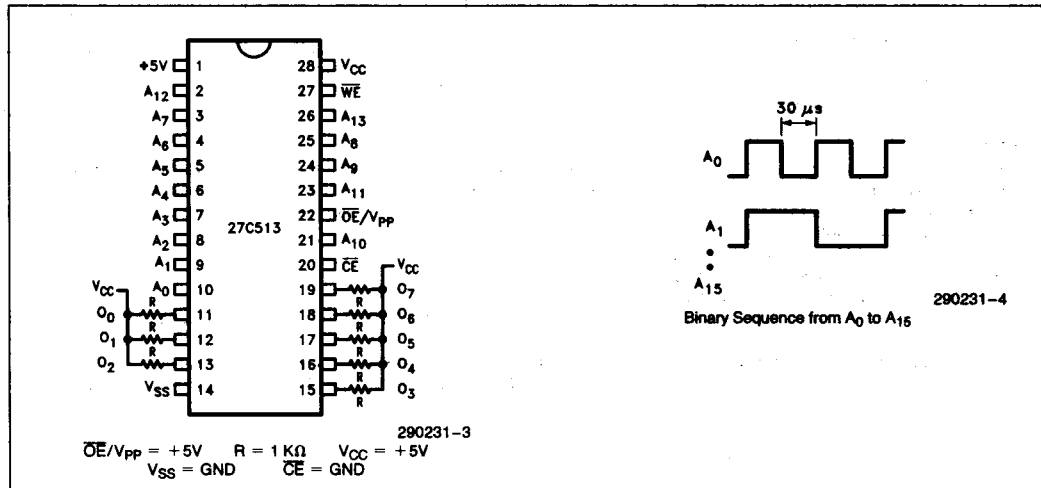
Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27C513 LD27C513		Test Conditions
		Min	Max	
I _{SB}	V _{CC} Standby Current (mA)		1.0	$\overline{CE} = V_{IH}, \overline{OE}/V_{PP} = V_{IL}$
I _{CC1} (1)	V _{CC} Active Current (mA)		50	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V _{CC} Active Current at High Temperature (mA)		50	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}, T_{Ambient} = 85^\circ C$

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NOTE:

1. The maximum current value is with outputs O₀ to O₇ unloaded.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

- Operating Temperature
 - During Read 0°C to + 70°C(2)
- Temperature Under Bias - 10°C to + 80°C(2)
- Storage Temperature - 65°C to + 125°C
- Voltage on Any Pin with Respect to Ground - 2V to + 7V(1)
- Voltage on A₉ with Respect to Ground - 2V to + 13.5V(1)
- V_{PP} Supply Voltage with Respect to Ground during Programming - 2V to + 14.0V(1)
- V_{CC} Supply Voltage with Respect to Ground - 2V to + 7.0V(1)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

DC CHARACTERISTICS TTL and NMOS Inputs

Symbol	Parameter	Notes	Min	Typ ⁽³⁾	Max	Units	Test Condition
I _{LI}	Input Load Current			0.01	1.0	μA	V _{IN} = 0V to 5.5V
I _{LO}	Output Leakage Current				± 10	μA	V _{OUT} = 0V to 5.5V
I _{SB}	V _{CC} Current Standby				1.0	mA	CE = V _{IH}
I _{CC1}	V _{CC} Current Active	5			30	mA	CE = V _{IL} f = 5 MHz, I _{OUT} = 0 mA
I _{PP1}	V _{PP} Current Read	8			10	μA	V _{PP} = V _{CC}
V _{IL}	Input Low Voltage (± 10% Supply)	1	-0.5		0.8	V	
V _{IH}	Input High Voltage (± 10% Supply)		2.0		V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage				0.45	V	I _{OL} = 2.1 mA
V _{OH}	Output High Voltage		2.4			V	I _{OH} = 400 μA
I _{OS}	Output Short Circuit Current	6			100	mA	
V _{PP}	V _{PP} Read Voltage	7	V _{CC} - 0.7		V _{CC}	V	
V _{CLR}	Page Latch Clear V _{CC} Supply Voltage			3.5	4.0	V	

NOTES:

1. Minimum DC input voltage is -0.5V. During transitions, the inputs may undershoot to -2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Automotive versions.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. CE is V_{CC} ± 0.2V. All other inputs can have any value within spec.
5. Maximum current value is with outputs O₀ to O₇ unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. V_{CC} must be applied simultaneously or before OE/V_{PP} and removed simultaneously or after OE/V_{PP}.
8. Maximum active power usage is the sum of I_{PP} and I_{CC}. The maximum current value is with no loading on outputs O₀ to O₇.

DC CHARACTERISTICS CMOS Inputs

Symbol	Parameter	Notes	Min	Typ ⁽³⁾	Max	Units	Test Condition
I_{LI}	Input Load Current			0.01	1.0	μA	$V_{IN} = 0\text{V to } 5.5\text{V}$
I_{LO}	Output Leakage Current				± 10	μA	$V_{OUT} = 0\text{V to } 5.5\text{V}$
I_{SB}	V_{CC} Current Standby with Inputs—	Switching	4		6	mA	$\overline{CE} = V_{IH}$
		Stable			100	μA	$\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Current Active	5			30	mA	$\overline{CE} = V_{IL}$ $f = 5\text{ MHz}, I_{OUT} = 0\text{ mA}$
V_{IL}	Input Low Voltage ($\pm 10\%$ Supply)		-0.2		0.8	V	
V_{IH}	Input High Voltage ($\pm 10\%$ Supply)		$0.7 V_{CC}$		$V_{CC} + 0.2$	V	
V_{OL}	Output Low Voltage				0.4	V	$I_{OL} = 2.1\text{ mA}$
V_{OH}	Output High Voltage		$V_{CC} - 0.8$			V	$I_{OH} = -2.5\text{ mA}$
I_{OS}	Output Short Circuit Current	6			100	mA	

NOTES:

- Minimum DC input voltage is -0.5V . During transitions, the inputs may undershoot to -2.0V for periods less than 20 ns. Maximum DC voltage on output pins is $V_{CC} + 0.5\text{V}$ which may overshoot to $V_{CC} + 2\text{V}$ for periods less than 20 ns.
- Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Automotive versions.
- Typical limits are at $V_{CC} = 5\text{V}$, $T_A = +25^\circ\text{C}$.
- \overline{CE} is $V_{CC} \pm 0.2\text{V}$. All other inputs can have any value within spec.
- Maximum current value is with outputs O_0 to O_7 unloaded.
- Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
- V_{CC} must be applied simultaneously or before \overline{OE}/V_{PP} and removed simultaneously or after \overline{OE}/V_{PP} .
- Maximum active power usage is the sum of I_{PP} and I_{CC} . The maximum current value is with no loading on outputs O_0 to O_7 .

PAGE-SELECT WRITE AND PAGE-RESET OPERATION

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AC CHARACTERISTICS

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{CW}	\overline{CE} to End of Write	100		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WP}	Write Pulse Width	100		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{DH}	Data Hold Time	20		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{CS}	\overline{CE} to Write Setup Time	0		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WH}	\overline{WE} Low from \overline{OE}/V_{PP} High Delay Time	55		ns	
t_{RST}	Reset Low Time	100		ns	
t_{RAV}	Reset to Address Valid	150		ns	

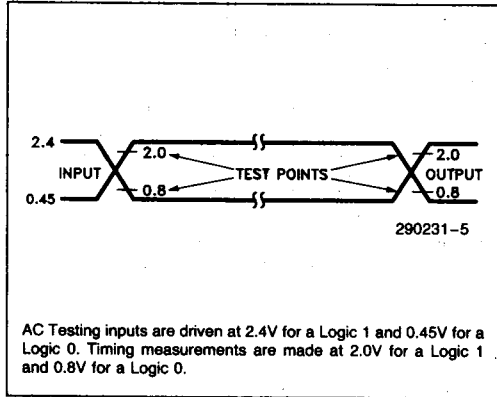
NOTES:

- V_{CC} must be applied simultaneously or before \overline{OE}/V_{PP} and removed simultaneously or after \overline{OE}/V_{PP} .
- Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.
- This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
- The maximum current value is with outputs O_0 – O_7 unloaded.
- Packaging Options: No prefix = Cerdp.
- RST function is available only on parts with 6-digit suffix.

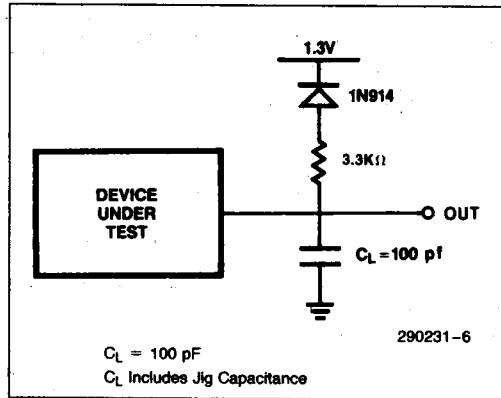
CAPACITANCE(2) $T_A = +25^\circ\text{C}$, $f = 1\text{ MHz}$

Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	8	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
$C_{OE/V_{PP}}$	\overline{OE}/V_{PP} Capacitance	18	25	pF	$V_{IN} = 0V$

AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT



AC CHARACTERISTICS $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$

Versions(4)	$V_{CC} \pm 10\%$	27C513-170V10		27C513-200V10		27C513-250V10		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		170		200		250	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
t_{CE}	\overline{CE} to Output Delay		170		200		250	ns	$\overline{OE}/V_{PP} = V_{IL}$
t_{OE}	\overline{OE}/V_{PP} to Output Delay		65		65		100	ns	$\overline{CE} = V_{IL}$
$t_{DF}^{(3)}$	\overline{OE}/V_{PP} High to Output Float	0	55	0	55	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses \overline{CE} or \overline{OE}/V_{PP} , Whichever Occurred First	0		0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

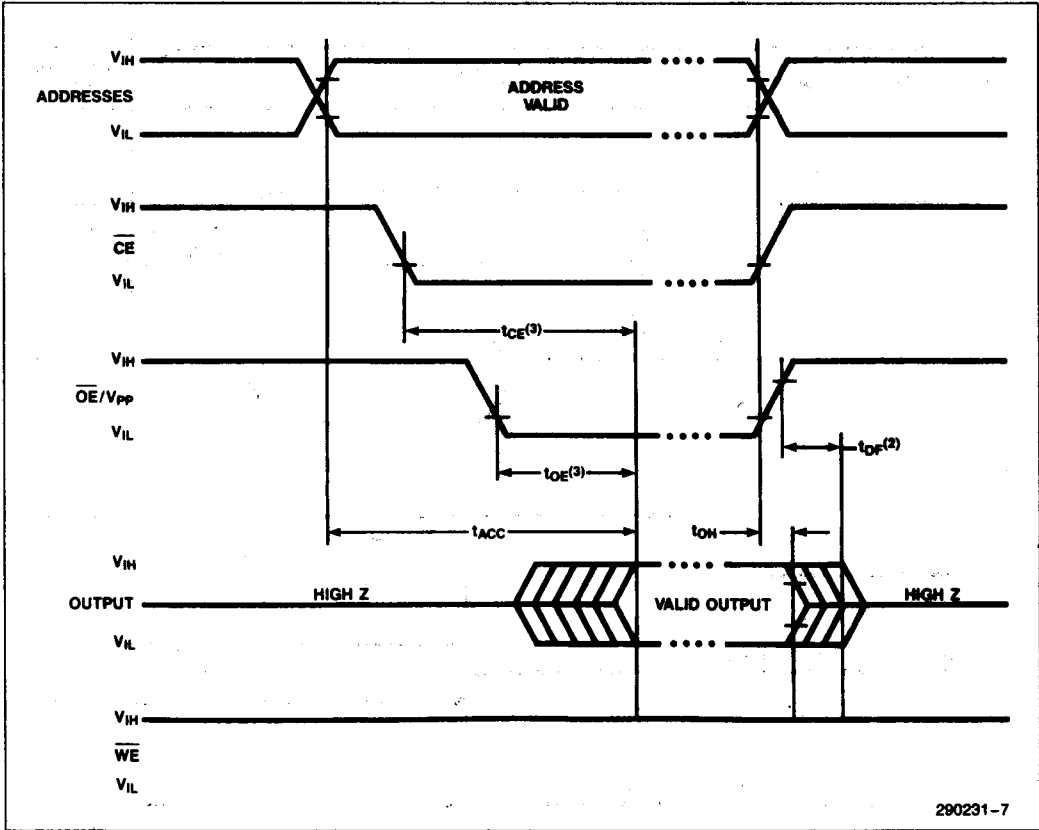
NOTES:

1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0-O_7 unloaded.
4. Packaging: No prefix = Cerdip.

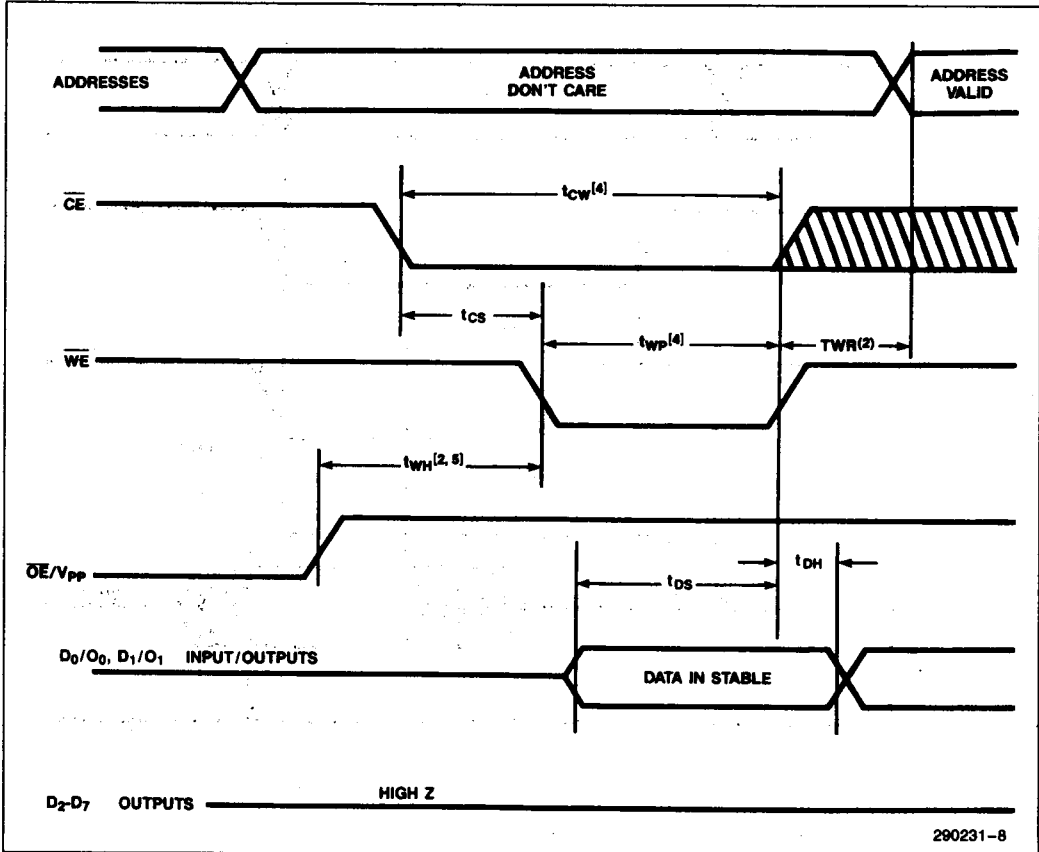
AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 10 ns
 Input Pulse Levels V_{OL} to V_{OH}
 Input Timing Reference Level 1.5V
 Output Timing Reference Level V_{IL} and V_{IH}

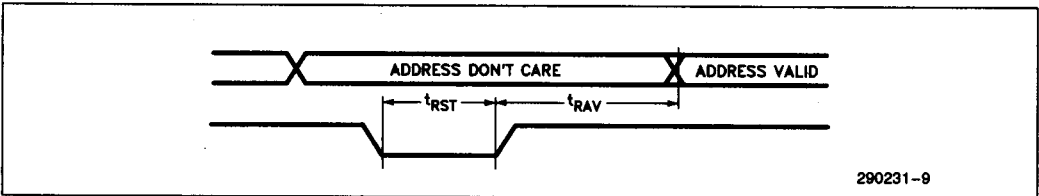
AC WAVEFORMS FOR READ OPERATION



AC WAVEFORMS FOR PAGE-SELECT WRITE OPERATION



AC WAVEFORMS FOR PAGE-RESET OPERATIONS



NOTES:

1. Typical values are for $T_A = +25^\circ\text{C}$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. OE/V_{pp} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of CE without impact on t_{CE} .
4. Write may be terminated by either CE or WE , providing that the minimum t_{cw} requirement is met before bringing WE high or that the minimum t_{wp} requirement is met before bringing CE high.
5. OE/V_{pp} must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27C513 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for \overline{OE}/V_{PP} and 12V on A_9 for intelligent Identifier mode.

Table 1. Operating Modes

Pins	\overline{CE}	\overline{OE}/V_{PP}	\overline{WE}	\overline{RST}	A_9	A_0	V_{CC}	Outputs	Input/Outputs
Mode									
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X ⁽¹⁾	X	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	V_{IH}	X	X	V_{CC}	High Z	High Z
Programming	V_{IL}	V_{PP} ⁽³⁾	V_{IH}	V_{IH}	X	X	(Note 3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	(Note 3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	V_{PP} ⁽³⁾	V_{IH}	V_{IH}	X	X	(Note 3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	V_{CC} ⁽⁵⁾	High Z	Page ⁽²⁾ D_{IN}
Page-Reset	X	X	X	V_{IL}	X	X	V_{CC} ⁽⁵⁾	High Z	X
intelligent ⁽⁴⁾ —Manufacturer Identifier	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H ⁽⁶⁾	V_{IL}	5.0V	89H	89H
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H ⁽⁶⁾	V_{IH}	5.0V	F9H	F9H

NOTES:

1. X can be V_{IH} or V_{IL} .
2. Addresses don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 2 for V_{CC} and V_{PP} voltages.
4. $A_1-A_8, A_{10}-A_{13} = V_{IL}$.
5. Page 0 is automatically selected at power-up ($V_{CC} < 4.0V$).
6. $V_H = 12.0V \pm 0.5\%$.

Read Mode

The 27C513 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}/V_{PP}) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of \overline{OE}/V_{PP} , assuming that \overline{CE} has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. \overline{WE} is held high during read operations.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the \overline{CE} input. When in standby mode, the outputs are in a high impedance state, independent of the \overline{OE}/V_{PP} and \overline{WE} inputs.

Page-Select Write Mode

The 27C513 is addressed by first selecting one of four 16 Kbyte pages. Individual bytes are then selected by normal random access within the 16 Kbyte page using the proper combination of A_0-A_{13} address inputs. By applying a TTL low signal to the \overline{WE} input with \overline{CE} low and \overline{OE} high, the desired page is latched in according to the combination of D_0/O_0 and D_1/O_1 . Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output (Pin) Page Selection	D_1/O_1 (12)	D_0/O_0 (11)
Select Page 0	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IH}
Select Page 2	V_{IH}	V_{IL}
Select Page 3	V_{IH}	V_{IH}

Page Reset

The 27C513 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case -10% V_{CC} supply condition) against spurious page latch clearing.

The 27C513 also has a page reset pin: \overline{RST} . This pin should be tied to an active low system reset signal. These 27C513s will be reset to page 0 when this line is brought to TTL Low (V_{IL}).

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

- the lowest possible memory power dissipation, and
- complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, \overline{CE} should be decoded and used as the primary device selecting function, while \overline{OE}/V_{PP} should be made a common connection to all devices in the array and connected to the \overline{READ} line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, \overline{CE} deselects other 27C513s or RAMs during page select write operation while \overline{WE} is in common with other devices in the array. \overline{WE} is connected to the \overline{WRITE} system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC} , has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by

properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on $\overline{\text{OE}}/V_{\text{PP}}$ will permanently damage the 27C513.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the $\overline{\text{OE}}/V_{\text{PP}}$ input is raised to its programming voltage (see Table 2) and $\overline{\text{CE}}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27C513s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{\text{CE}}$ input inhibits the other 27C513s from being programmed.

Except for $\overline{\text{CE}}$, all inputs of the parallel 27C513s may be common. A TTL low-level pulse applied to the $\overline{\text{CE}}$ input with $\overline{\text{OE}}/V_{\text{PP}}$ at its programming voltage will program the selected 27C513.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{\text{OE}}/V_{\text{PP}}$ and $\overline{\text{CE}}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{\text{CE}}$.

Intelligent Identifier Mode

The Intelligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A_9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during the intelligent Identifier Mode.

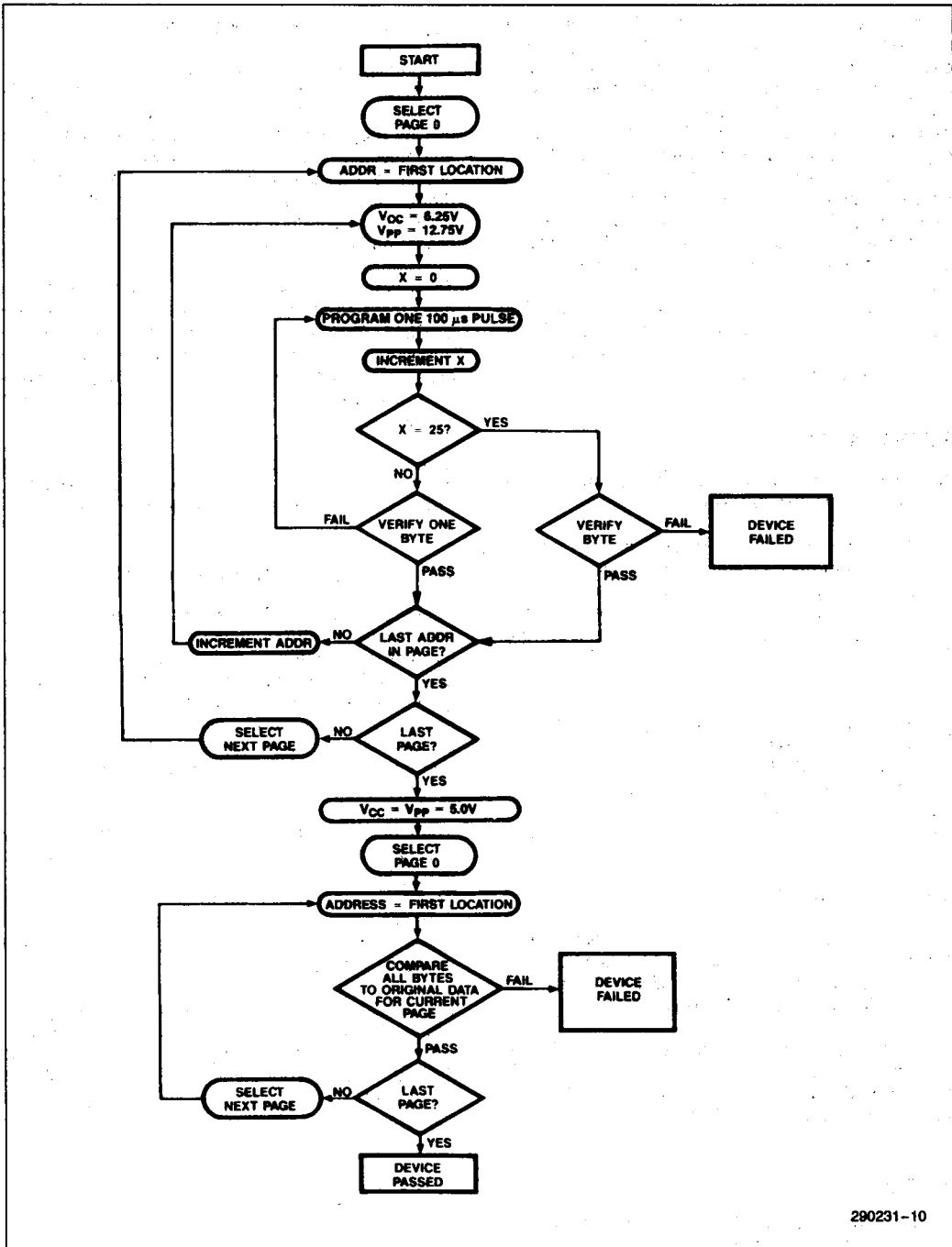
Byte 0 ($A_0 = V_{\text{IL}}$) represents the manufacturer code and byte 1 ($A_0 = V_{\text{IH}}$) the device identifier code. These two identifier bytes are given in Table 1.

Quick Pulse Programming Algorithm

Intel's 27C513 EPROM can be programmed using the Quick-Pulse Programming algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed as fast as fourteen seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming algorithm uses initial pulses of 100 μs followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming algorithm, the entire sequence of programming pulses and byte verifications is performed at $V_{\text{CC}} = 6.25\text{V}$ and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{\text{CC}} = V_{\text{PP}} = 5.0\text{V}$.



290231-10

Figure 3. 27C513 Quick-Pulse Programming Flowchart

ERASURE CHARACTERISTICS (FOR Cerdip EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm² power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm² (1 week @ 12000 μW/cm²). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

TABLE 2. DC PROGRAMMING CHARACTERISTICS

T_A = 25°C ± 5°C

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I _{LI}	Input Current (All Inputs)		1	μA	V _{IN} = V _{IL} or V _{IH}
V _{IL}	Input Low Level (All Inputs)	-0.1	0.8	V	
V _{IH}	Input High Level	2.4	6.5	V	
V _{OL}	Output Low Voltage During Verify		0.45	V	I _{OL} = 2.1 mA
V _{OH}	Output High Voltage During Verify	3.5		V	I _{OH} = -2.5 mA
I _{CC2} (²)	V _{CC} Supply Current (Program and Verify)		40	mA	
I _{PP2} (²)	V _{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V _{ID}	A _g intelligent Identifier Voltage	11.5	12.5	V	
V _{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V _{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

NOTES:

- V_{CC} must be applied simultaneously or before \overline{OE}/V_{PP} and removed simultaneously or after \overline{OE}/V_{PP} .
- The maximum current value is with outputs O₀–O₇ unloaded.

AC PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t _{AS}	Address Setup Time	2			μs	
t _{OES}	\overline{OE}/V_{PP} Setup Time	2			μs	
t _{DS}	Data Setup Time	2			μs	
t _{AH}	Address Hold Time	0			μs	
t _{DH}	Data Hold Time	2			μs	
t _{DFP}	Output Enable to Output Float Delay	0		130	ns	(Note 2)
t _{VCS}	V _{CC} Setup Time	2			μs	(Note 1)
t _{PW}	\overline{CE} Initial Program Pulse Width	95	100	105	μs	
t _{OEH}	\overline{OE}/V_{PP} Hold Time	2			μs	
t _{DV}	Data Valid from \overline{CE}			1	μs	
t _{VR}	\overline{OE}/V_{PP} Recovery Time	2			μs	
t _{PRT}	\overline{OE}/V_{PP} Pulse Rise Time During Programming	50			ns	

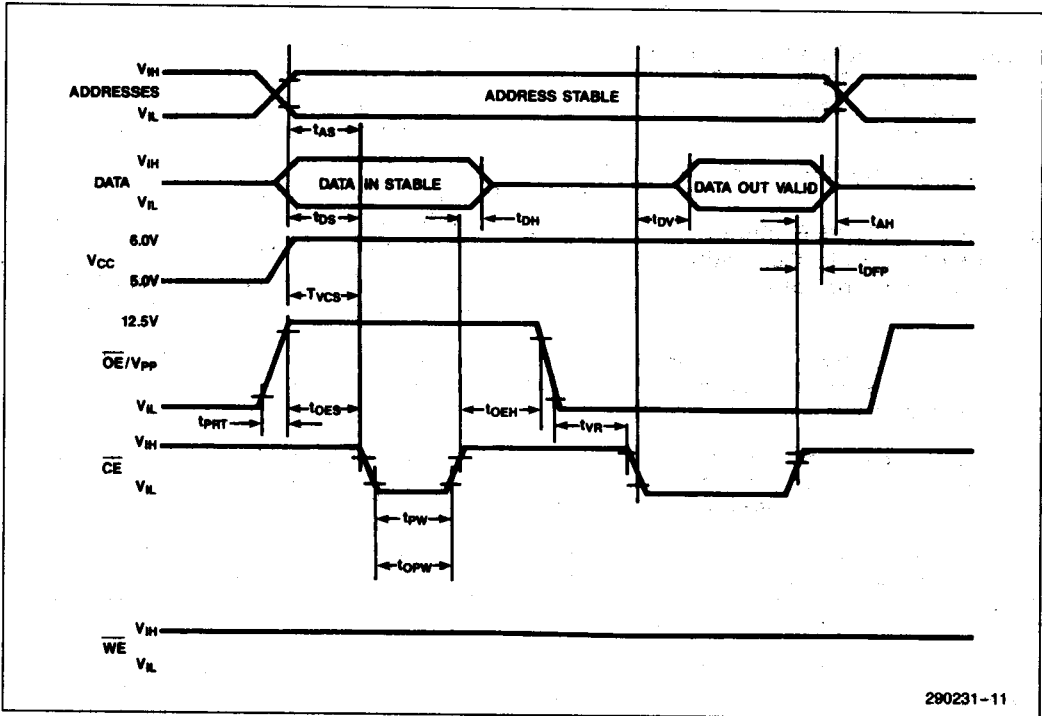
***AC CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) 20 ns
 Input Pulse Levels 0.45V to 2.4V
 Input Timing Reference Level 0.8V and 2.0V
 Output Timing Reference Level 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before \overline{OE}/V_{PP} and removed simultaneously or after \overline{OE}/V_{PP} .
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

PROGRAMMING WAVEFORMS



290231-11

NOTES:

1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH} .
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 Kbyte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.

REVISION HISTORY

Number	Description
003	Removed "Advance Information" Classification. Revised t_{WP} from 50 ns to 100 ns Revised V_{CLR} (3.5V) from Min to Typ