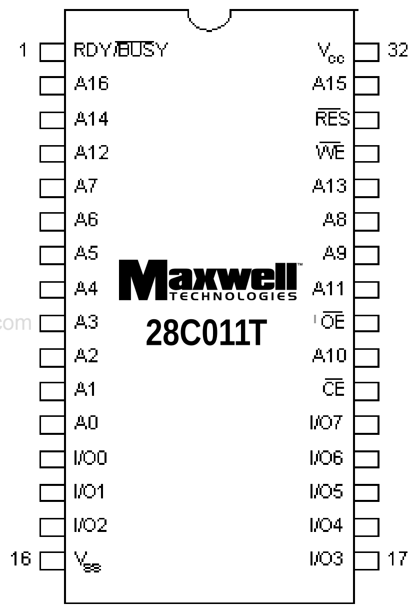
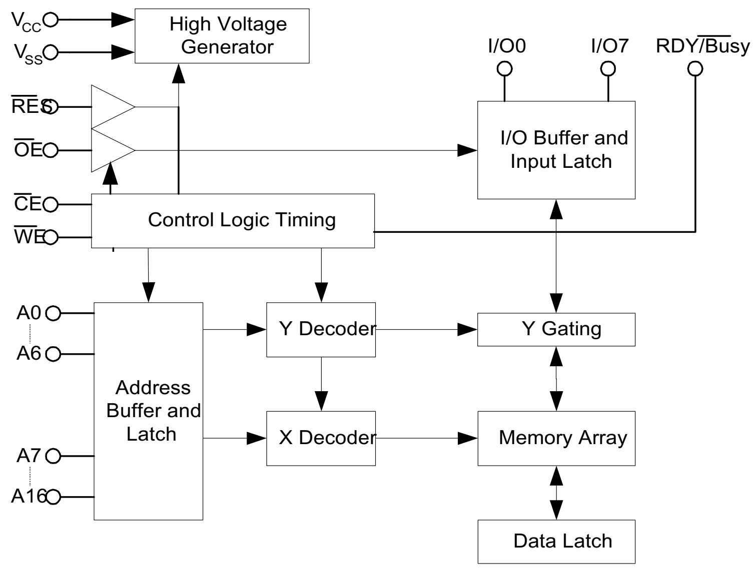
28C011T

1 Megabit (128K x 8-Bit) EEPROM





Logic Diagram

Features:

- 128k x 8-bit EEPROM
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  - \> 100 krad (Si), depending upon space mission
- Excellent Single Event Effects:
  - No Latchup > 120 MeV/mg/cm^2
  - SEU > 90 MeV/mg/cm^2 read mode
- Package:
  - 32-pin RAD-PAK® flat package
  - 32-pin Rad-Tolerant flat package
  - JEDEC-approved byte-wide pinout
- High speed:
  - 120, 150, and 200 ns maximum access times available
- High endurance:
  - 10,000 erase/write (in Page Mode),
  - 10 year data retention
- Page write mode:
  - 1 to 128 bytes
- Low power dissipation
  - 20 mW/MHz active (typical)
  - 110 µW standby (maximum)

Description:

Maxwell Technologies' 28C011T high-density 1 Megabit (128K x 8-Bit) EEPROM microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The 28C011T is capable of in-system electrical byte and page programmability. It has a 128-byte page programming function to make its erase and write operations faster. It also features data polling and a Ready/Busy signal to indicate the completion of erase and programming operations. In the 28C010T, hardware data protection is provided with the RES pin, in addition to noise protection on the WE signal and write inhibit on power on and off. Software data protection is implemented using the JEDEC optional standard algorithm.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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Table 1. 28C011T Pinout Description

Pin	Symbol	Description
12-5, 27, 26, 23, 25, 4, 28, 3, 31, 2	A0-A16	Address
24	$\overline{OE}$	Output Enable
22	$\overline{CE}$	Chip Enable
29	$\overline{WE}$	Write Enable
32	V_{CC}	Power Supply
16	V_{SS}	Ground
1	RDY/$\overline{BUSY}$	Ready/Busy
30	$\overline{RES}$	Reset

Table 2. 28C011T Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage (Relative to V_{SS})	V_{CC}	-0.6	+7.0	V
Input Voltage (Relative to V_{SS})	V_{IN}	-0.5 [1]	+7.0	V
Operating Temperature Range	T_{OPR}	-55	+125	˚C
Storage Temperature Range	T_{STG}	-65	+150	˚C

1. V_{IN} min = -3.0V for pulse width $\leq$ 50ns.

Table 3. Delta Limits

Parameter	Variation
$I_{CC}1$	±10%
$I_{CC}2$	±10%
$I_{CC}3A$	±10%
$I_{CC}3B$	±10%

Table 4. 28C011T Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	4.5	5.5	V
Input Voltage	V_{IL}	-0.3[1]	0.8	V
	V_{IH}	2.2	V_{CC} +0.3	
$\overline{RES}$_PIN	V_H	V_{CC} -0.5	V_{CC} +1	
Operating Temperature Range	T_{OPR}	-55	+125	˚C

1. V_{IL} min = -1.0V for pulse width $\leq$ 50 ns

Table 5. 28C011T Capacitance

(T_A = 25 °C, f = 1 MHZ)

Parameter	Symbol	Min	Max	Units
Input Capacitance: V_{IN} = 0V [1]	C_{IN}	--	6	pF
Output Capacitance: V_{OUT} = 0V [1]	C_{OUT}	--	12	pF

1. Guaranteed by design.

Table 6. 28C011T DC Electrical Characteristics

(V_{CC} = 5V ± 10%, T_A = -55 to +125 °C, unless otherwise specified)

Parameter	Test Condition	Subgroups	Symbol	Min	Max	Units
Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 5.5V	1, 2, 3	I_{IL}	--	2 [1]	µA
Output Leakage Current	V_{CC} = 5.5V, V_{OUT} = 5.5V/0.4V	1, 2, 3	I_{LO}	--	2	µA
Standby V_{CC} Current	$\overline{CE}$ = V_{CC}	1, 2, 3	I_{CC1}	--	20	µA
	$\overline{CE}$ = V_{IH}		I_{CC2}	--	1	mA
Operating V_{CC} Current	I_{OUT} = 0mA, Duty = 100%, Cycle = 1µs at V_{CC} = 5.5V	1, 2, 3	I_{CC3A}	--	15	mA
	I_{OUT} = 0mA, Duty = 100%, Cycle = 150ns at V_{CC} = 5.5V	1, 2, 3	I_{CC3B}	--	50	
Input Voltage		1, 2, 3	V_{IL}	--	0.8	V
			V_{IH}	2.2	--	
$\overline{RES}$_PIN			V_H	V_{CC} -0.5	--	
Output Voltage	I_{OL} = 2.1 mA	1, 2, 3	V_{OL}	--	0.4	V
	I_{OH} = -0.4 mA		V_{OH}	2.4	--	

1. I_{LI} on RES = 100 uA max.

Table 7. 28C011T AC Electrical Characteristics for Read Operation [1]

(V_{CC} = 5V ± 10%, T_A = -55 to +125 °C)

Parameter	Symbol	Subgroups	Min	Max	Units
Address Access Time $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -120 -150 -200	t_{ACC}	9, 10, 11	 -- -- --	 120 150 200	ns
Chip Enable Access Time $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -120 -150 -200	t_{CE}	9, 10, 11	 -- -- --	 120 150 200	ns

Table 7. 28C011T AC Electrical Characteristics for Read Operation [1]

(V_{CC} = 5V ± 10%, T_A = -55 to +125 °C)

Parameter	Symbol	Subgroups	Min	Max	Units
Output Enable Access Time	t_{OE}	9, 10, 11			ns
$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$					
-120			0	75	
-150			0	75	
-200			0	100	
Output Hold to Address Change	t_{OH}	9, 10, 11			ns
$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$					
-120			0	--	
-150			0	--	
-200			0	--	
Output Disable to High-Z [2]		9, 10, 11			ns
$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$	t_{DF}				
-120			0	50	
-150			0	50	
-200			0	60	
$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$					
-120	t_{DFR}		0	300	
-150			0	350	
-200			0	450	
$\overline{RES}$ to Output Delay[3]	t_{RR}	9, 10, 11			ns
$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$					
-120			--	400	
-150			--	450	
-200			--	650	

1. Test conditions: Input pulse levels - 0.4V to 2.4V; input rise and fall times < 20ns; output load - 1 TTL gate + 100pF (including scope and jig); reference levels for measuring timing - 0.8V/1.8V.
2. t_{DF} and t_{DFR} are defined as the time at which the output becomes an open circuit and data is no longer driven.
3. Guaranteed by design.

Table 8. 28C011T AC Electrical Characteristics for Page/Byte Erase and Byte Write Operations

(V_{CC} = 5V ± 10%, T_A = -55 to +125 °C)

Parameter	Symbol	Subgroups	Min [1]	Max	Units
Address Setup Time	t_{AS}	9, 10, 11			ns
-120			0	--	
-150			0	--	
-200			0	--	
Chip Enable to Write Setup Time ($\overline{WE}$ controlled)	t_{CS}	9, 10, 11			
-120			0	--	ns
-150			0	--	
-200			0	--	

Table 8. 28C011T AC Electrical Characteristics for Page/Byte Erase and Byte Write Operations

(V_{CC} = 5V ± 10%, T_A = -55 to +125 °C)

Parameter	Symbol	Subgroups	Min [1]	Max	Units
Write Pulse Width		9, 10, 11			
$\overline{CE}$ controlled	t_{CW}				ns
-120			200	--	
-150			250	--	
-200			350	--	
$\overline{WE}$ controlled	t_{WP}				
-120			200	--	
-150			250	--	
-200			350	--	
Address Hold Time	t_{AH}	9, 10, 11			ns
-120			150	--	
-150			150	--	
-200			200	--	
Data Setup Time	t_{DS}	9, 10, 11			ns
-120			75	--	
-150			100	--	
-200			150	--	
Data Hold Time	t_{DH}	9, 10, 11			ns
-120			10	--	
-150			10	--	
-200			10	--	
Chip Enable Hold Time ($\overline{WE}$ controlled)	t_{CH}	9, 10, 11			
-120			0	--	ns
-150			0	--	
-2000			0	--	
Write Enable to Write Setup Time ($\overline{CE}$ controlled)	t_{WS}	9, 10, 11			ns
-120			0	--	
-150			0	--	
-200			0	--	
Write Enable Hold Time ($\overline{CE}$ controlled)	t_{WH}	9, 10, 11			ns
-120			0	--	
-150			0	--	
-200			0	--	
Output Enable to Write Setup Time	t_{OES}	9, 10, 11			ns
-120			0	--	
-150			0	--	
-200			0	--	
Output Enable Hold Time	t_{OEH}	9, 10, 11			ns
-120			0	--	
-150			0	--	
-200			0	--	

Table 8. 28C011T AC Electrical Characteristics for Page/Byte Erase and Byte Write Operations

(V_{CC} = 5V ± 10%, T_A = -55 to +125 °C)

Parameter	Symbol	Subgroups	Min [1]	Max	Units
Write Cycle Time[2]	t_{WC}	9, 10, 11			ms
-120			--	10	
-150			--	10	
-200			--	10	
Data Latch Time	t_{DL}	9, 10, 11			ns
-120			250	--	
-150			300	--	
-200			400	--	
Byte Load Window	t_{BL}	9, 10, 11			µs
-120			100	--	
-150			100	--	
-200			200	--	
Byte Load Cycle	t_{BLC}	9, 10, 11			µs
-120			0.55	30	
-150			0.55	30	
-200			0.95	30	
Time to Device Busy	t_{DB}	9, 10, 11			ns
-120			100	--	
-150			120	--	
-200			170	--	
Write Start Time[3]	t_{DW}	9, 10, 11			ns
-120			150	--	
-150			150	--	
-200			250	--	
$\overline{RES}$ to Write Setup Time	t_{RP}	9, 10, 11			µs
-120			100	--	
-150			100	--	
-200			200	--	
V_{CC} to $\overline{RES}$ Setup Time[4]	t_{RES}	9, 10, 11			µs
-120			1	--	
-150			1	--	
-200			3	--	

1. Use this device in a longer cycle than this value.
2. t_{WC} must be longer than this value unless polling techniques or RDY/BUSY are used. This device automatically completes the internal write operation within this value.
3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/BUSY are used.
4. Gauranteed by design.

TABLE 9. 28C011T MODE SELECTION [1]

PARAMETER	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	$\overline{RES}$	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_H	High-Z
Standby	V_{IH}	X	X	High-Z	X	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_H	High-Z --> V_{OL}
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write Inhibit	X	X	V_{IH}	--	X	--
	X	V_{IL}	X	--	X	--
Data Polling	V_{IL}	V_{IL}	V_{IH}	Data Out (I/O7)	V_H	V_{OL}
Program	X	X	X	High-Z	V_{IL}	High-Z

1. X = Don't care.

FIGURE 1. READ TIMING WAVEFORM

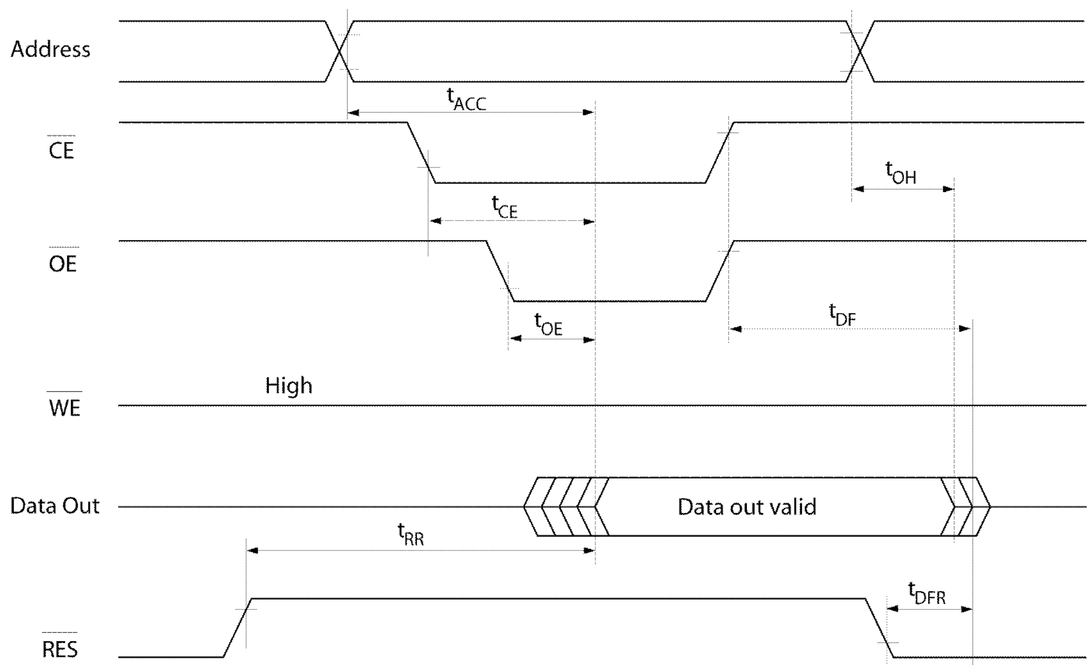


FIGURE 2. BYTE WRITE TIMING WAVEFORM(1) ($\overline{WE}$ CONTROLLED)

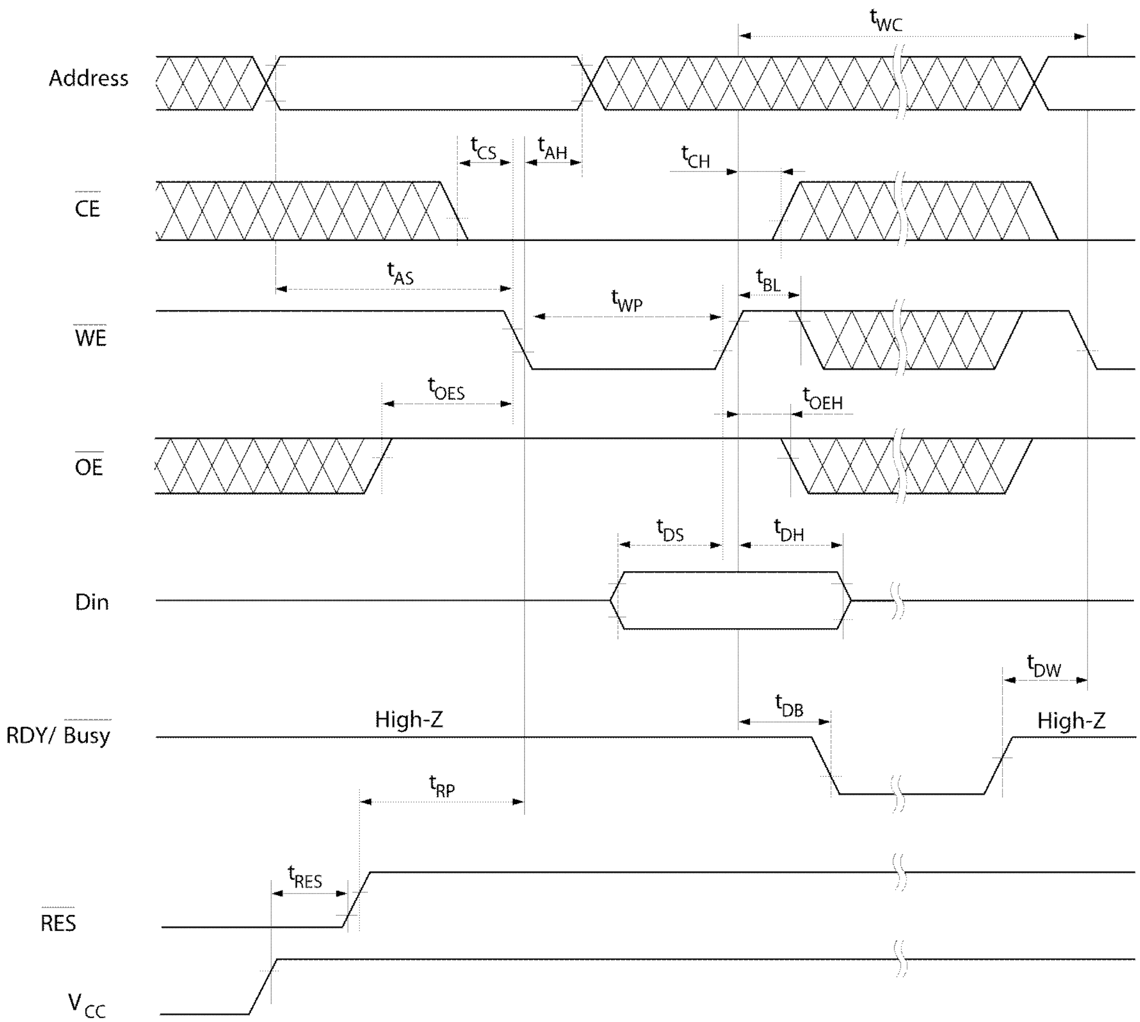


FIGURE 3. BYTE WRITE TIMING WAVEFORM (2) ($\overline{CE}$ CONTROLLED)

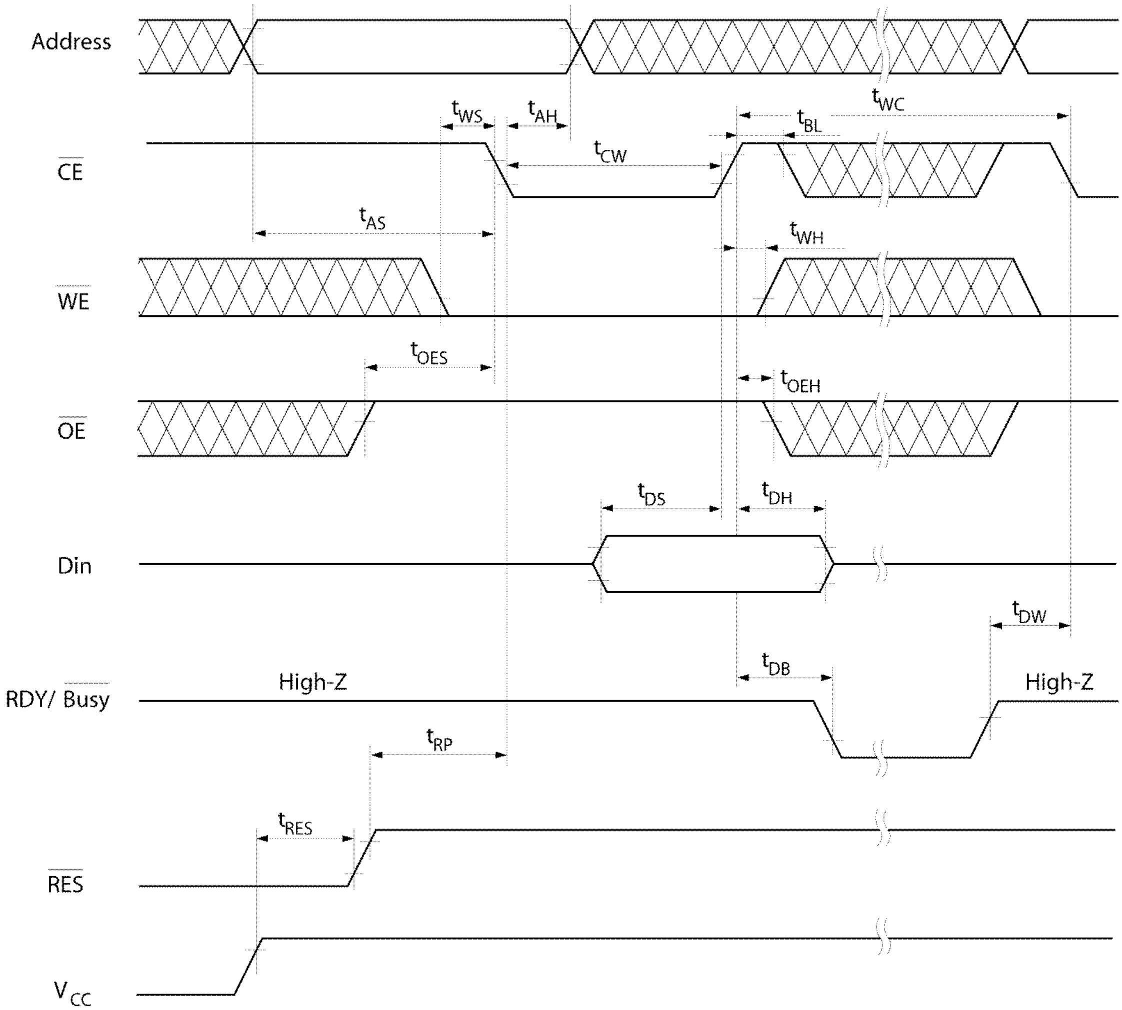


FIGURE 4. PAGE WRITE TIMING WAVEFORM(1) ($\overline{WE}$ CONTROLLED)

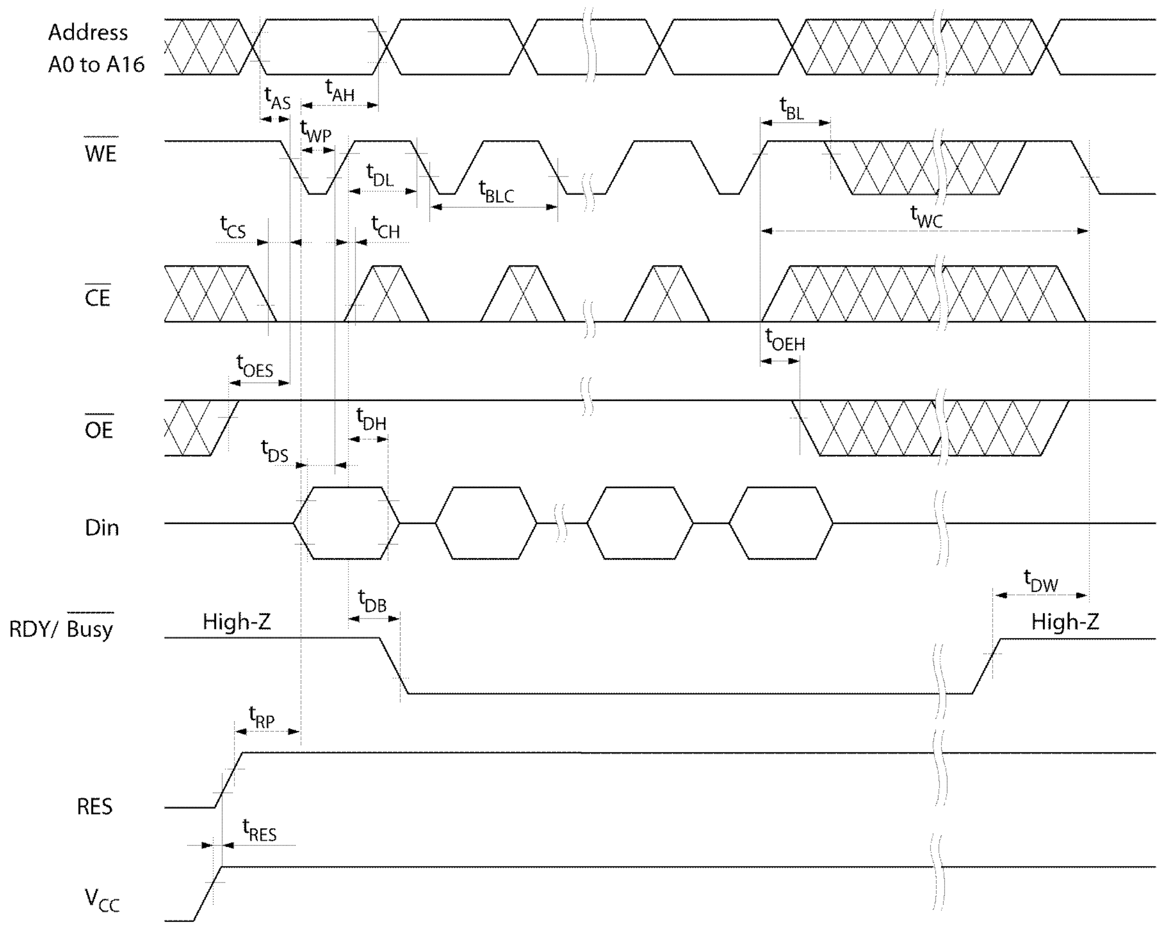


FIGURE 5. PAGE WRITE TIMING WAVEFORM(2) ($\overline{CE}$ CONTROLLED)

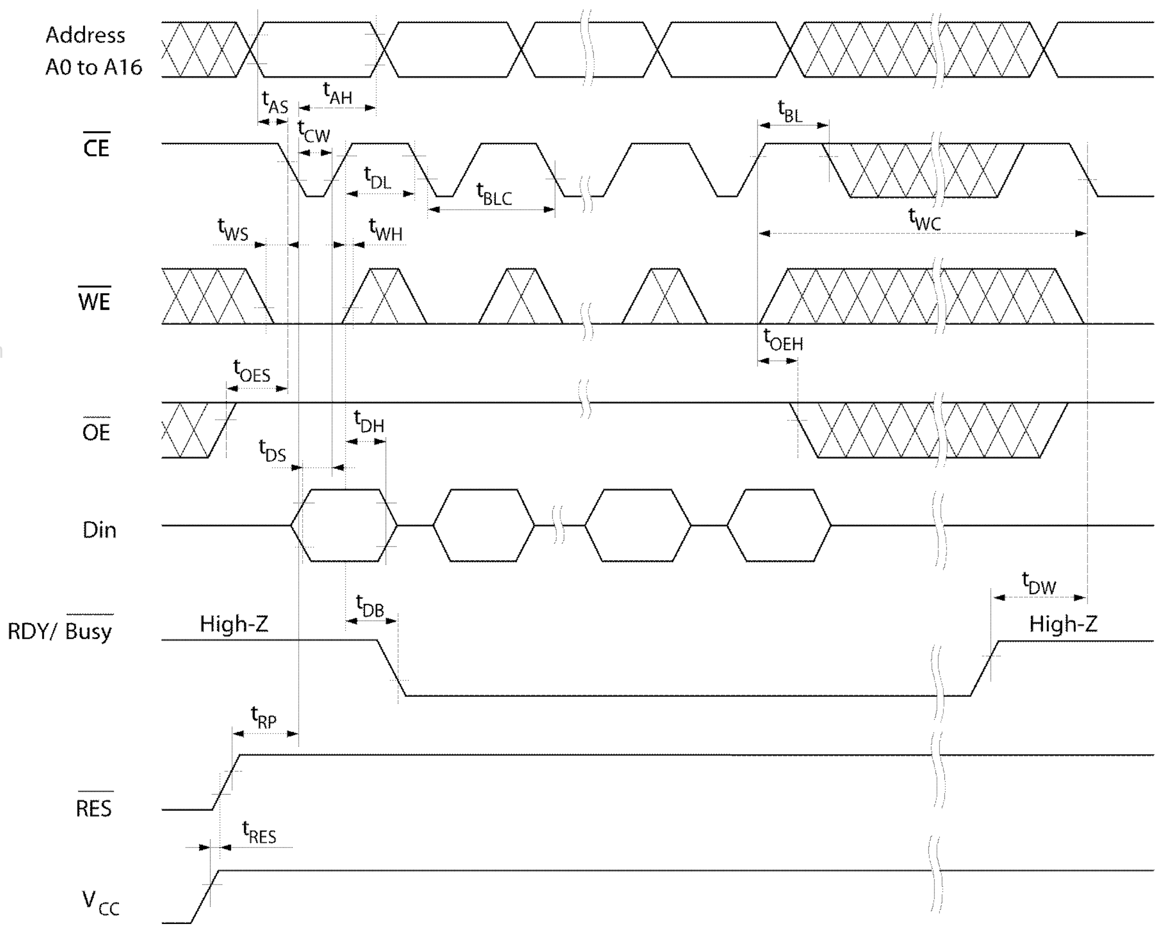


FIGURE 6. $\overline{DATA}$ POLLING TIMING WAVEFORM

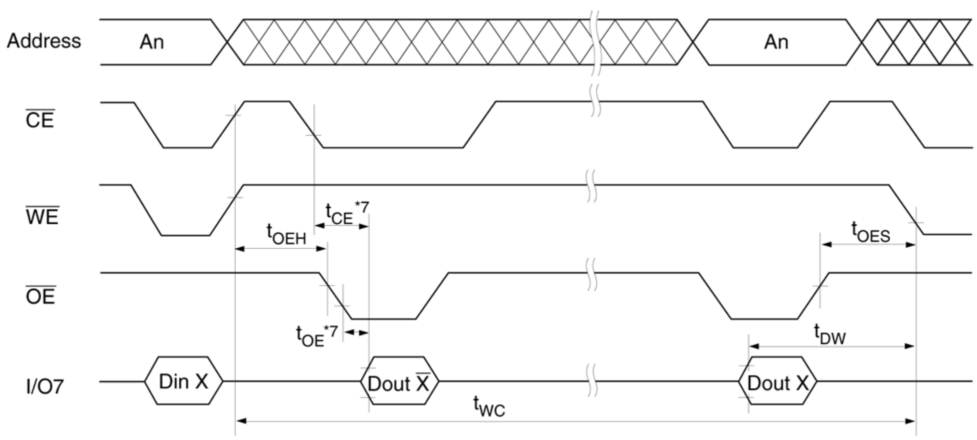


Figure 7. Software Data Protection Timing Waveform(1) (in protection mode)

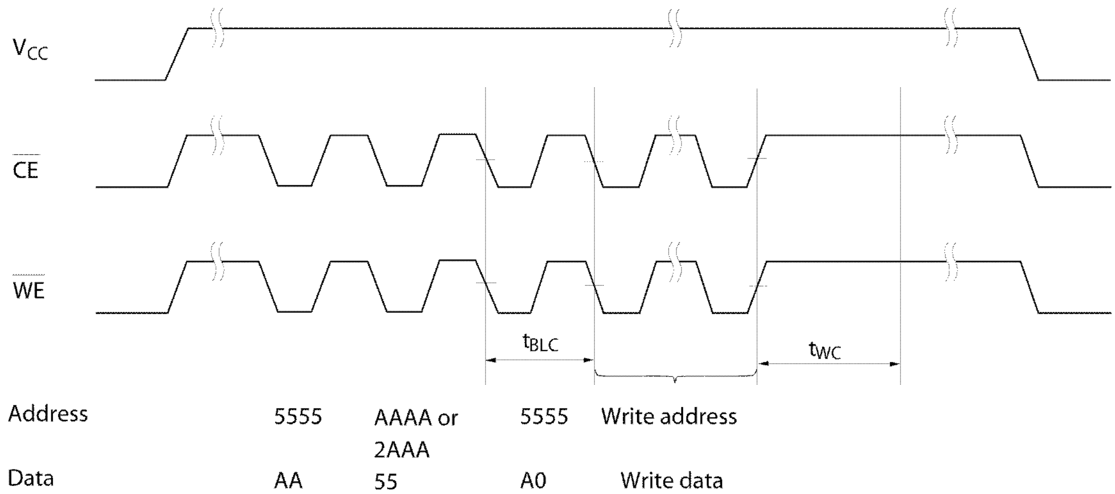
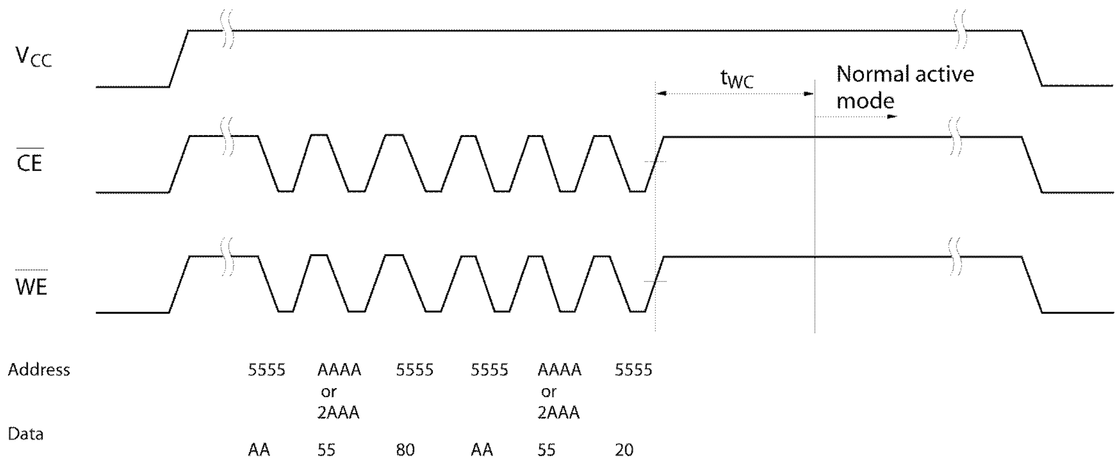


Figure 8. Software Data Protection Timing Waveform(2) (in non-protection mode)



EEPROM Application Notes

This application note describes the programming procedures for the EEPROM modules and with details of various techniques to preserve data protection.

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle, and allows the undefined data within 128 bytes to be written corresponding to the undefined address (A0 to A6). Loading the first byte of data, the data load window opens 30µs for the second byte. In the same manner each additional byte of data can be loaded within 30µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, EEPROM enters erase and write mode automatically and only the input data are written into the EEPROM.

$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

$\overline{\text{Data}}$ Polling

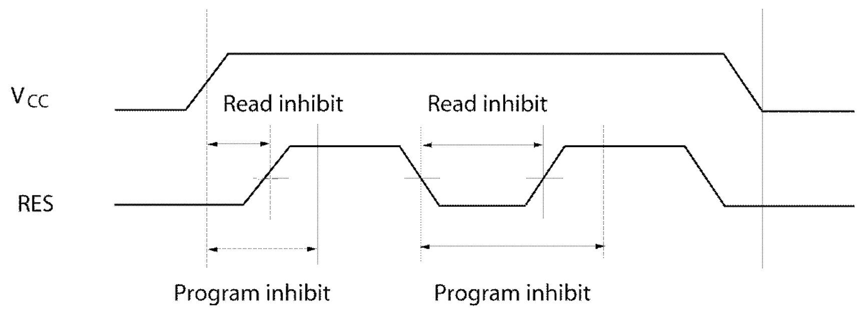
$\overline{\text{Data}}$ Polling function allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O 7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{\text{Busy}}$ Signal

RDY/$\overline{\text{Busy}}$ signal also allows a comparison operation to determine the status of the EEPROM. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the-end of a write cycle, the RDY/Busy signal changes state to high impedance.

$\overline{RES}$ Signal

When $\overline{RES}$ is LOW, the EEPROM cannot be read and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.

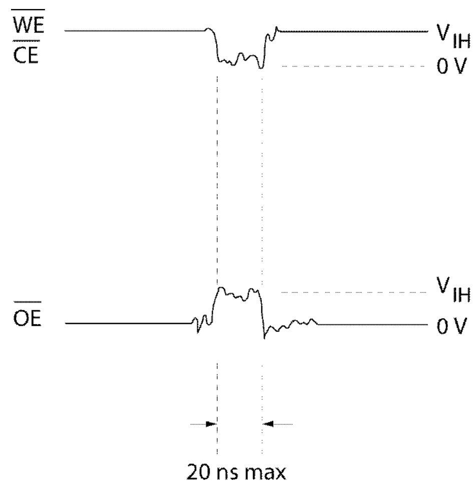


Data Protection

To protect the data during operation and power on/off, the EEPROM has the internal functions described below.

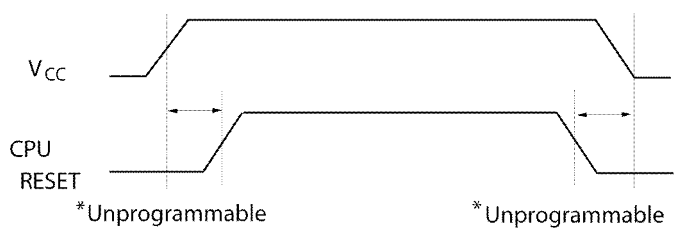
1. Data Protection against Noise of Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the EEPROM has a noise cancellation function that cuts noise if its width is 20ns or less in programming mode. Be careful not to allow noise of a width of more than 20ns on the control pins.

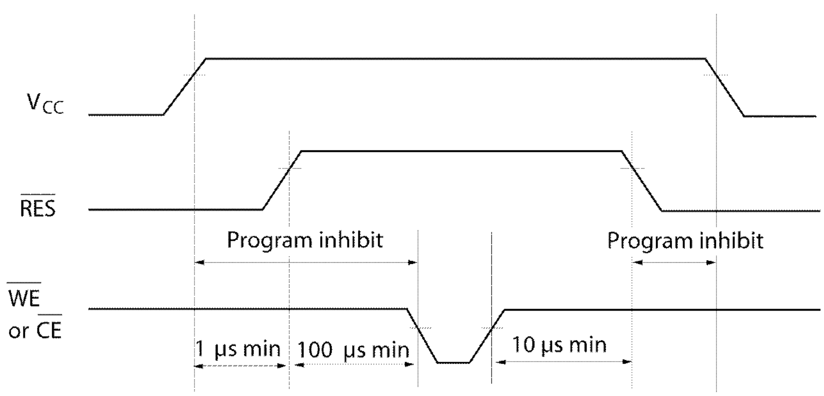


2. Data Protection at V_{CC} on/off

   When V_{CC} is turned on or off, noise on the control pins generated by external circuits, such as CPUs, may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state during V_{CC} on/off by using a CPU reset signal to $\overline{RES}$ pin.



$\overline{RES}$ should be kept at V_{SS} level when V_{CC} is turned on or off. The EEPROM breaks off programming operation when $\overline{RES}$ become low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.



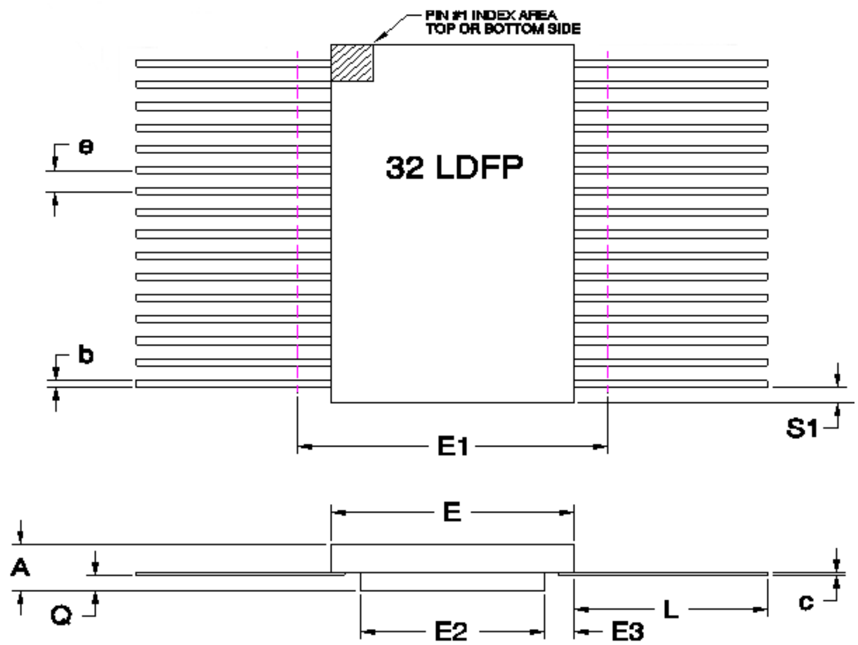
3. Software Data Protection

The software data protection function is to prevent unintentional programming caused by noise generated by external circuits. In software data protection mode, 3 bytes of data must be input before write data as follows. These bytes can switch the non-protection mode to the protection mode.

Address	Data	
5555	AA	
↓	↓	
AAAA or 2AAA	55	
↓	↓	
5555	A0	
↓	↓	
Write address	Write data }	Normal data input

Software data protection mode can be canceled by inputting the following 6 bytes. Then, the EEPROM turns to the non-protection mode and can write data normally. However, when the data is input in the canceling cycle, the data cannot be written.

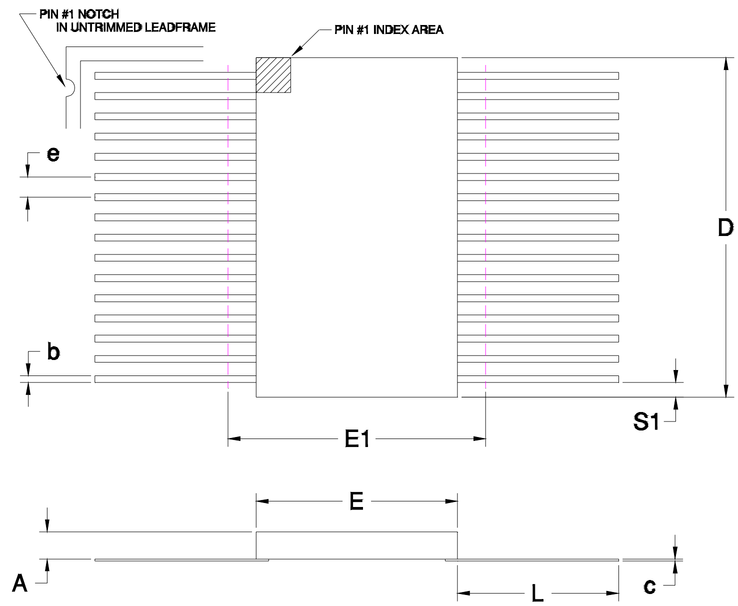
Address	Data
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	20



32-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.117	0.130	0.143
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.820	0.830
E	0.404	0.410	0.416
E1	--	--	0.440
e	0.050BSC		
L	0.350	0.370	0.390
Q	0.021	0.033	0.036
S1	0.005	0.027	--
N	32		

Note: All dimensions in inches



28C011T 32-Pin Rad-Tolerant Flat Package

Symbol	Dimension		
	Min	Nom	Max
A	0.078	0.087	0.096
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.820	0.830
E	0.404	0.410	0.416
E1	--	--	0.426
e	0.050BSC		
L	0.390	0.400	0.410
S1	0.005	0.027	--
N	32		

Note: All dimensions in inches.

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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Product Ordering Options

Model Number

28C011T XX F X -XX

Feature	Option Details
Access Time (-XX)	12 = 120 ns 15 = 150 ns 20 = 200 ns
Screening Flow (X)	Monolithic S = Maxwell Class S B = Maxwell Class B I = Industrial (testing @ -55°C, +25°C, +125°C) E = Engineering (testing @ +25°C)
Package (F)	F = Flat Pack
Radiation Feature (XX)	RP = RAD-PAK® package RT = No Radiation Guarentee CLass E and I Only RT1 = Guaranteed to 10 krad at die level RT2 = Guaranteed to 25 krad at die level RT4 = Guaranteed to 40 krad at
Base Product Nomenclature (28C011T)	1 Megabit (128k x 8-bit) EEPROM