28F016XD
16-MBIT (1 MBIT x 16)
DRAM-INTERFACE FLASH MEMORY

- **85 ns Access Time (t_{RAC})**
  - **— Supports both Standard and Fast-Page-Mode Accesses**
- **Multiplexed Address Bus**
  - **— RAS# and CAS# Control Inputs**
- **No-Glue Interface to Many Memory Controllers**
- **SmartVoltage Technology**
  - **— User-Selectable 3.3V or 5V V_{CC}**
  - **— User-Selectable 5V or 12V V_{PP}**
- **0.33 MB/sec Write Transfer Rate**
- **x16 Architecture**
- **56-Lead TSOP Type I Package**
- **Backwards-Compatible with 28F008SA Command Set**
- **2 µA Typical Deep Power-Down Current**
- **1 mA Typical I_{CC} Active Current in Static Mode**
- **32 Separately-Erasable/Lockable 64-Kbyte Blocks**
- **1 Million Erase Cycles per Block**
- **State-of-the-Art 0.6 µm ETOX™ IV Flash Technology**

Intel's 28F016XD 16-Mbit flash memory is a revolutionary architecture which is the ideal choice for designing truly revolutionary high-performance products. Combining its DRAM-like read performance and interface with the intrinsic nonvolatility of flash memory, the 28F016XD eliminates the traditional redundant memory paradigm of shadowing code from a slow nonvolatile storage source to a faster execution memory, such as DRAM, for improved system performance. The innovative capabilities of the 28F016XD enable the design of direct-execute code and mass storage data/file flash memory systems.

The 28F016XD's DRAM-like interface with a multiplexed address bus, flexible V_{CC} and V_{PP} voltages, power saving features, extended cycling, fast program and read performance, symmetrically-blocked architecture, and selective block locking provide a highly flexible memory component suitable for resident flash component arrays on the system board or SIMMs. The DRAM-like interface with RAS# and CAS# control inputs allows for easy migration to flash memory in existing DRAM-based systems. The 28F016XD's dual read voltage allows the same component to operate at either 3.3V or 5.0V V_{CC}. Programming voltage at 5.0V V_{PP} minimizes external circuitry in minimal-chip, space critical designs, while the 12.0V V_{PP} option maximizes program/erase performance. The x16 architecture allows optimization of the memory-to-processor interface. Its high read performance combined with flexible block locking enable both storage and execution of operating systems/application software and fast access to large data tables. The 28F016XD is manufactured on Intel's 0.6 µm ETOX IV process technology.

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CONTENTS

REVISION HISTORY

Number	Description
-001	Original Version
-002	Removed support of the following features: • All page buffer operations (read, write, programming, Upload Device Information) • Command queuing • Software Sleep and Abort • Erase All Unlocked Blocks • Device Configuration command Changed definition of "NC." Removed "No internal connection to die" from description. Added "xx" to Upper Byte of Command (Data) Definition in Sections 4.2 and 4.3. Modified parameters "V" and "I" of Section 5.1 to apply to "NC" pins. Increased I_{PPS} (V_{PP} Read Current) for $V_{PP} > V_{CC}$ to 200 µA at V_{CC} = 3.3V/5.0V. Changed V_{CC} = 5.0V DC Characteristics (Section 5.5) marked with Note 1 to indicate that these currents are specified for a CMOS rise/fall time (10% to 90%) of <5 ns and a TTL rise/fall time of <10 ns. Corrected "RP# high to RAS# going low" to be a "Min" specification at V_{CC} = 3.3V/5.0V. Increased Typical "Word/Block Program Times" (t_{WHRH1}/t_{WHRH3}) for V_{PP} = 5.0V: t_{WHRH1} from 24.0 µs to 35.0 µs and t_{WHRH3} from 0.8 sec to 1.2 sec at V_{CC} = 3.3V t_{WHRH1} from 16.0 µs to 25.0 µs and t_{WHRH3} from 0.6 sec to 0.85 sec at V_{CC} = 5.0V Changed "Time from Erase Suspend Command to WSM Ready" spec name to "Erase Suspend Latency Time to Read;" modified typical values and added Min/Max values at V_{CC} =3.3/5.0V and V_{PP} =5.0/12.0V (Section 5.10). Minor cosmetic changes throughout document.
-003	Added 3/5# pin to Pinout Configuration (Figure 2), Product Overview (Section 1.1) and Lead Descriptions (Section 2.1) Modified Block Diagram (Figure 1): Removed Address/Data Queues, Page Buffers, and Address Counter; Added 3/5# pin Added 3/5# pin to Test Conditions of $I_{CC}2$ and $I_{CC}5$ Specifications Modified Power-Up and Reset Timings (Section 5.9) to include 3/5# pin: Removed t_{5VPH} and t_{3VPH} specifications; Added t_{PLYL}, t_{PLYH}, t_{YLPH}, and t_{YHPH} specifications Corrected TSOP Mechanical Specification A1 from 0.50 mm to 0.050 mm (Section 6.0) Minor cosmetic changes throughout document.
-004	Updated DC Specifications $I_{CC}3$, $I_{CC}4$, $I_{CC}6$, $I_{CC}7$, I_{CCD} and I_{PPES} Updated AC Specifications t_{CAS}(min), t_{RCD}(max) and t_{CWD}(min)

1.0 INTRODUCTION

The documentation of the Intel 28F016XD flash memory device includes this datasheet, a detailed user's manual, and a number of application notes and design tools, all of which are referenced in Appendix B.

The datasheet is intended to give an overview of the chip feature-set and of the operating AC/DC specifications. *The 16-Mbit Flash Product Family User's Manual* provides complete descriptions of the user modes, system interface examples and detailed descriptions of all principles of operation. It also contains the full list of software algorithm flowcharts, and a brief section on compatibility with the Intel 28F008SA.

Significant 28F016XD feature revisions occurred between datasheet revisions 290533-001 and 290533-002. These revisions center around removal of the following features:

- All page buffer operations (read, write, programming, Upload Device Information)
- Command queuing
- Software Sleep and Abort
- Erase all Unlocked Blocks
- Device Configuration command

In addition, a significant 28F016XD change occurred between datasheet revisions 290532-002 and 290532-003. This change centers around the addition of a 3/5# pin to the device's pinout configuration. Figure 2 shows the 3/5# pin assignment for the TSOP Type 1 package.

Intel recommends that all customers obtain the latest revisions of 28F016XD documentation.

1.1 Product Overview

The 28F016XD is a high-performance, 16-Mbit (16,777,216-bit) block erasable, nonvolatile random access memory, organized as 1 Mword x 16. The 28F016XD includes thirty-two 32-KW (32,768 word) blocks. A chip memory map is shown in Figure 3.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and result in greater product reliability and ease-of-use as compared to other flash memories. Significant features of the 28F016XD include:

- No-Glue Interface to Memory Controllers
- Improved Word Program Performance
- SmartVoltage Technology
  - — Selectable 3.3V or 5.0V V_{CC}
  - — Selectable 5.0V or 12.0V V_{PP}
- Block Program/Erase Protection

The 28F016XD's multiplexed address bus with RAS# and CAS# inputs allows for a “No Glue” interface to many existing in-system memory controllers. As such, 28F016XD-based SIMMs (72-pin JEDEC Standard) offer attractive advantages over their DRAM counterparts in many applications. For more information on 28F016XD-based SIMM designs, see the application note referenced at the end of this datasheet.

The 28F016XD incorporates SmartVoltage technology, providing V_{CC} operation at both 3.3V and 5.0V and program and erase capability at V_{PP} = 12.0V or 5.0V. Operating at V_{CC} = 3.3V, the 28F016XD consumes less than 60% of the power consumption at 5.0V V_{CC}, while 5.0V V_{CC} provides the highest read performance capability. V_{PP} = 5.0V operation eliminates the need for a separate 12.0V converter, while V_{PP} = 12.0V maximizes program/erase performance. In addition to the flexible program and erase voltages, the dedicated V_{PP} gives complete code protection with $V_{PP} \leq V_{PPLK}$.

A 3/5# input pin configures the device's internal circuitry for optimal 3.3V or 5.0V read/program operation.

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows word programs and block erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the 28F008SA 8-Mbit FlashFile™ memory.

Software Locking of Memory Blocks is an added feature of the 28F016XD as compared to the 28F008SA. The 28F016XD provides selectable block locking to protect code or data such as direct-executable operating systems or application code. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the 28F016XD has a master Write Protect pin (WP#) which prevents any modifications to memory blocks whose lock-bits are set.

Writing of memory data is performed in word increments typically within 6 µs (12.0V V_{PP})—a 33% improvement over the 28F008SA. A block erase operation erases one of the 32 blocks in typically 0.6 sec (12.0V V_{PP}), independent of the other blocks, which is about a 65% improvement over the 28F008SA.

Each block can be written and erased a minimum of 100,000 cycles. Systems can achieve one million Block Erase Cycles by providing wear-leveling algorithms and graceful block retirement. These techniques have already been employed in many flash file systems and hard disk drive designs.

All operations are started by a sequence of Write commands to the device. Three types of Status Registers (described in detail later in this datasheet) and a RY/BY# output pin provide information on the progress of the requested operation.

The following Status Registers are used to provide device and WSM information to the user :

- A Compatible Status Register (CSR) which is 100% compatible with the 28F008SA FlashFile memory Status Register. The CSR, when used alone, provides a straightforward upgrade capability to the 28F016XD from a 28F008SA-based design.
- A Global Status Register (GSR) which also informs the system of overall Write State Machine (WSM) status.
- 32 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

The GSR and BSR memory maps are shown in Figure 4.

The 28F016XD incorporates an open drain RY/BY# output pin. This feature allows the user to OR-tie many RY/BY# pins together in a multiple memory configuration such as a Resident Flash Array.

The 28F016XD is specified for a maximum fast page mode cycle time of 65 ns ($t_{PC,R}$) at 5.0V operation (4.75V to 5.25V) over the commercial temperature range (0°C to +70°C). A corresponding maximum fast page mode cycle time of 75 ns at 3.3V (3.0V to 3.6V and 0°C to +70°C) is achieved for reduced power consumption applications.

The 28F016XD incorporates an Automatic Power Saving (APS) feature, which substantially reduces the active current when the device is in static mode of operation (addresses not switching). In APS mode, the typical I_{CC} current is 1 mA at 5.0V (3.0 mA at 3.3V).

A deep power-down mode of operation is invoked when the RP# (called PWD# on the 28F008SA) pin transitions low. This mode brings the device power consumption to less than 2.0 µA, typically, and provides additional write protection by acting as a device reset pin during power transitions. A reset time of 300 ns (5.0V V_{CC} operation) is required from RP# switching high until dropping RAS#. In the deep power-down state, the WSM is reset (any current operation will abort) and the CSR, GSR and BSR registers are cleared.

A CMOS standby mode of operation is enabled when RAS# and CAS# transition high and RP# stays high with all input control pins at CMOS levels. In this mode, the device typically draws an I_{CC} standby current of 70 µA at 5.0V V_{CC}.

The 28F016XD is available in a 56-Lead, 1.2 mm thick, 14 mm x 20 mm TSOP Type I package. This form factor and pinout allow for very high board layout densities.

2.0 DEVICE PINOUT

The 28F016XD 56-Lead TSOP Type I pinout configuration is shown in Figure 2.

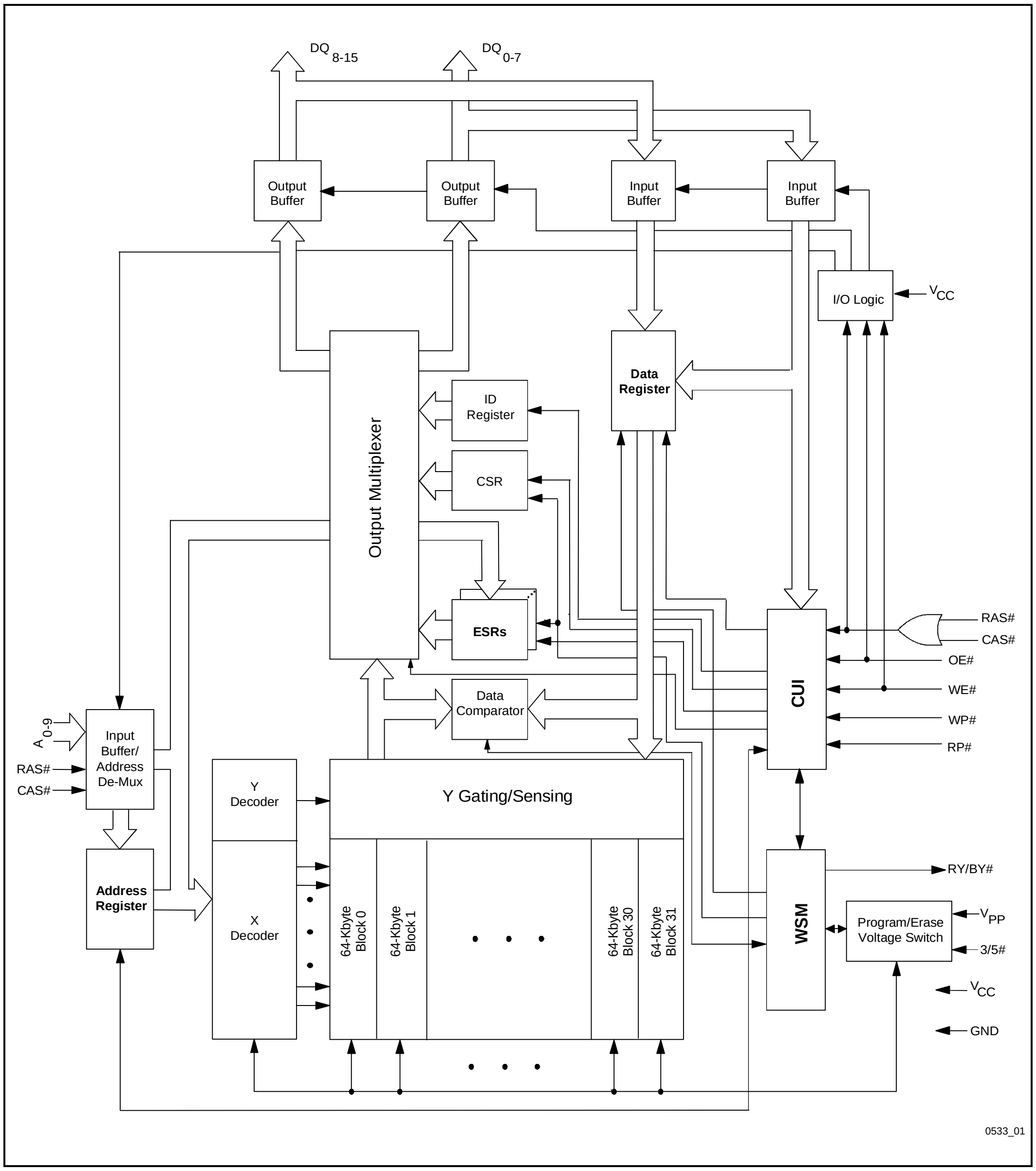

Figure 1. 28F016XD Block Diagram
Architectural Evolution Includes Multiplexed Address Bus, SmartVoltage Technology, and Extended Registers

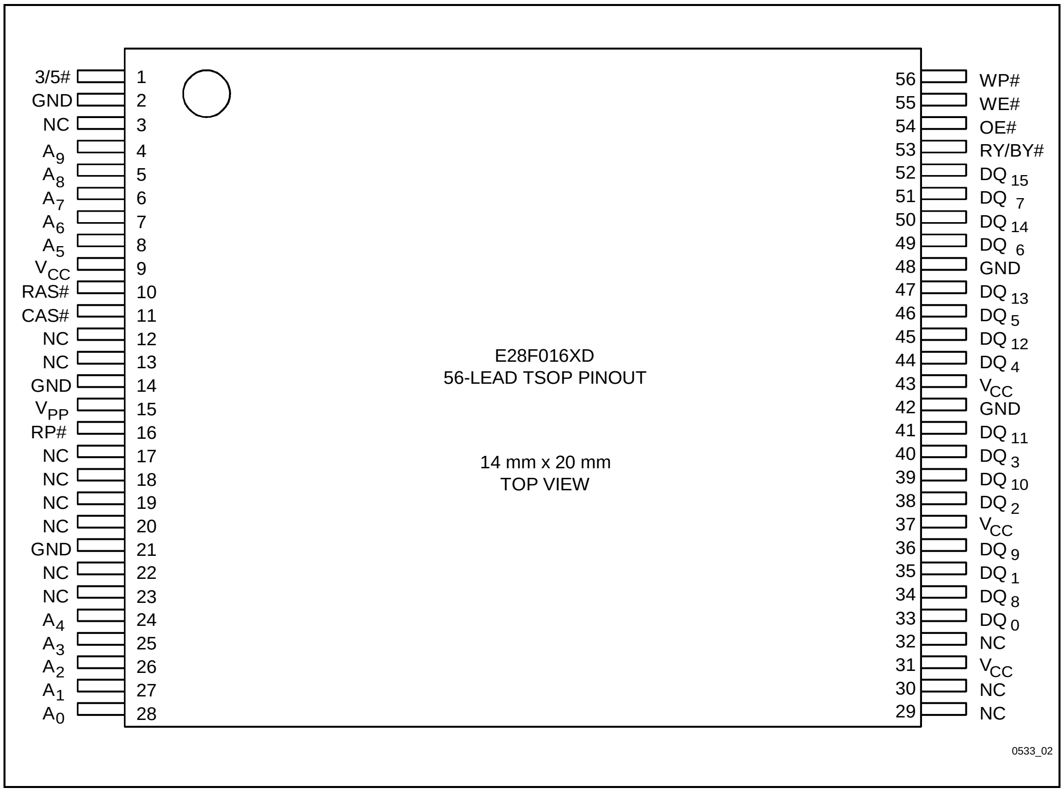

Figure 2. 28F016XD 56-Lead TSOP Type I Pinout Configuration

2.1 Lead Descriptions

Symbol	Type	Name and Function
A_0–A_9	INPUT	**MULTIPLEXED ROW/COLUMN ADDRESSES:** Selects a word within one of thirty-two 32-Kword blocks. Row (upper) addresses are latched on the falling edge of RAS#, while column (lower) addresses are latched on the falling edge of CAS#.
DQ_0–DQ_{15}	INPUT/OUTPUT	**DATA BUS:** Inputs data and commands during CUI write cycles. Outputs array, identifier or status data (DQ_{0-7}) in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled.
RAS#	INPUT	**ROW ADDRESS STROBE:** Latches row address information on inputs A_{9-0} when RAS# transitions low. A subsequent CAS# low transition initiates 28F016XD read or program operations.
CAS#	INPUT	**COLUMN ADDRESS STROBE:** Latches column address information on inputs A_{9-0} when CAS# transitions low. When preceded by a RAS# low transition, CAS# low initiates 28F016XD read or program operations, along with OE# and WE#. Subsequent CAS# low transitions, with RAS# held low, enable fast page mode reads/programs
RP#	INPUT	**RESET/POWER-DOWN:** RP# low places the device in a deep power-down state. All circuits that consume static power, even those circuits enabled in standby mode, are turned off. When returning from deep power-down, a recovery time of 300 ns at 5.0V V_{CC} is required to allow these circuits to power-up. When RP# goes low, the current WSM operation is terminated, and the device is reset. All Status Registers return to ready (with all status flags cleared). Exit from deep power-down places the device in read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates device data through the output buffers when low in combination with RAS# and CAS# low. The outputs float to tri-state off when OE# is high. OE# can be tied to GND if not controlled by the system memory controller. RAS# and CAS# high override OE# low. WE# low also overrides OE# low.
WE#	INPUT	**WRITE ENABLE:** Controls access to the CUI, Data Register and Address Register. WE# is active low and initiates programs in combination with RAS# and CAS# low. WE# low overrides OE# low. RAS# and CAS# high override WE# low.
RY/BY#	OPEN DRAIN OUTPUT	**READY/BUSY:** Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. RY/BY# floating indicates that the WSM is ready for new operations, erase is suspended, or the device is in deep power-down mode. This output is always active (i.e., not floated to tri-state off when OE#, RAS# or CAS# are high).
WP#	INPUT	**WRITE PROTECT:** Erase blocks can be locked by writing a nonvolatile lock-bit for each block. When WP# is low, those locked blocks as reflected by the Block-Lock Status bits (BSR.6), are protected from inadvertent data programs or erases. When WP# is high, all blocks can be written or erased regardless of the state of the lock-bits. The WP# input buffer is disabled when RP# transitions low (deep power-down mode).

2.1 Lead Descriptions (Continued)

Symbol	Type	Name and Function
3/5#	INPUT	**3.3/5.0 VOLT SELECT:** 3/5# high configures internal circuits for 3.3V operation. 3/5# low configures internal circuits for 5.0V operation. **NOTE:** Reading the array with 3/5# high in a 5.0V system could damage the device. Reference the power-up and reset timings (Section 5.9) for 3/5# switching delay to valid data.
V_{PP}	SUPPLY	**PROGRAM/ERASE POWER SUPPLY (12.0V ± 0.6V, 5.0V ± 0.5V):** For erasing memory array blocks or writing words into the flash array. V_{PP} = 5.0V ± 0.5V eliminates the need for a 12.0V converter, while connection to 12.0V ± 0.6V maximizes program/erase performance. **NOTE:** Successful completion of program and erase attempts is inhibited with V_{PP} at or below 1.5V. Program and erase attempts with V_{PP} between 1.5V and 4.5V, between 5.5V and 11.4V, and above 12.6V produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3V ± 0.3V, 5.0V ± 0.5V):** To switch 3.3V to 5.0V (or vice versa), first ramp V_{CC} down to GND, and then power to the new V_{CC} voltage. Do not leave any power pins floating.
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECT:** Lead may be driven or left floating.

3.0 MEMORY MAPS

$A_{[19-0]}$		
FFFFF–F8000	32-Kword Block	31
F7FFF–F0000	32-Kword Block	30
EFFFF–E8000	32-Kword Block	29
E7FFF–E0000	32-Kword Block	28
DFFFF–D8000	32-Kword Block	27
D7FFF–D0000	32-Kword Block	26
CFFFF–C8000	32-Kword Block	25
C7FFF–C0000	32-Kword Block	24
BFFFF–B8000	32-Kword Block	23
B7FFF–B0000	32-Kword Block	22
A8FFF–A8000	32-Kword Block	21
A7FFF–A0000	32-Kword Block	20
9FFFF–98000	32-Kword Block	19
97FFF–90000	32-Kword Block	18
8FFFF–88000	32-Kword Block	17
87FFF–80000	32-Kword Block	16
7FFFF–78000	32-Kword Block	15
77FFF–70000	32-Kword Block	14
6FFFF–68000	32-Kword Block	13
67FFF–60000	32-Kword Block	12
5FFFF–58000	32-Kword Block	11
57FFF–50000	32-Kword Block	10
4FFFF–48000	32-Kword Block	9
47FFF–40000	32-Kword Block	8
3FFFF–38000	32-Kword Block	7
37FFF–30000	32-Kword Block	6
2FFFF–28000	32-Kword Block	5
27FFF–20000	32-Kword Block	4
1FFFF–18000	32-Kword Block	3
17FFF–10000	32-Kword Block	2
0FFFF–08000	32-Kword Block	1
07FFF–00000	32-Kword Block	0

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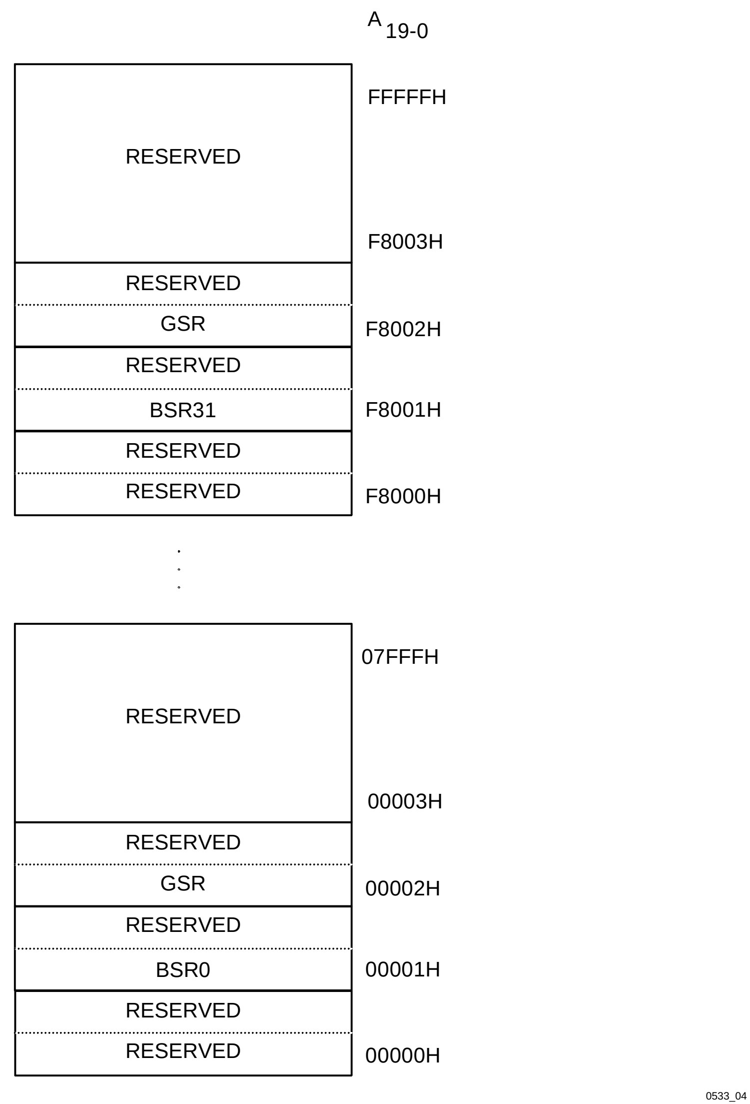
NOTE:
The upper 10 bits (A_{19-10}) reflect 28F016XD addresses A_{9-0}, latched by RAS#.
The lower 10 bits (A_{9-0}) reflect 28F016XD addresses A_{9-0}, latched by CAS#.

Figure 3. 28F016XD Memory Map

3.1 Extended Status Registers Memory Map



NOTE:

The upper 10 bits (A_{19-10}) reflect 28F016XD addresses A_{9-0}, latched by RAS#.

The lower 10 bits (A_{9-0}) reflect 28F016XD addresses A_{9-0}, latched by CAS#.

Figure 4. Extended Status Registers Memory Map

4.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

4.1 Bus Operations

Mode	Notes	RP#	RAS#	CAS#	OE#	WE#	DQ_{0-15}	RY/BY#
Row Address Latch	1,2,9	V_{IH}	↓	V_{IH}	X	X	X	X
Column Address Latch	1,2,9	V_{IH}	V_{IL}	↓	X	X	X	X
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High Z	X
Standby	1,6,7	V_{IH}	V_{IH}	V_{IH}	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4,8	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	0089H	V_{OH}
Device ID	4,8	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	66A8H	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IL}	X	V_{IL}	D_{IN}	X

NOTES:

1. X can be V_{IH} or V_{IL} for address or control pins except for RY/BY#, which is either V_{OL} or V_{OH}, or High Z or D_{OUT} for data pins depending on whether or not OE# is active.
2. RY/BY# output is open drain. When the WSM is ready, erase is suspended or the device is in deep power-down mode, RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. RY/BY# at V_{OH} is independent of OE# while a WSM operation is in progress.
3. RP# at GND ± 0.2V ensures the lowest deep power-down current.
4. A_0 (latched by CAS#) at V_{IL} provides the Manufacturer ID code. A_0 (latched by CAS#) at V_{IH} provides the Device ID code. All other addresses (row and column) should be set to zero.
5. Commands for erase, data program, or lock-block operations can only be completed successfully when $V_{PP} = V_{PPH1}$ or $V_{PP} = V_{PPH2}$.
6. While the WSM is running, RY/BY# stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
7. RY/BY# may be at V_{OL} while the WSM is busy performing various operations (for example, a Status Register read during a program operation).
8. The 28F016XD shares an identical device identifier with the 28F016XS.
9. Row (upper) addresses are latched via inputs A_{0-9} on the falling edge of RAS#. Column (lower) addresses are latched via inputs A_{0-9} on the falling edge of CAS#. Row addresses must be latched before column addresses are latched.

4.2 28F008SA—Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data(4)	Oper	Addr	Data(4)
Read Array		Write	X	xxFFH	Read	AA	AD
Intelligent Identifier	1	Write	X	xx90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	xx70H	Read	X	CSRD
Clear Status Register	3	Write	X	xx50H			
Word Program		Write	X	xx40H	Write	PA	PD
Alternate Word Program		Write	X	xx10H	Write	PA	PD
Block Erase/Confirm		Write	X	xx20H	Write	BA	xxD0H
Erase Suspend/Resume		Write	X	xxB0H	Write	X	xxD0H

ADDRESS	DATA
AA = Array Address	AD = Array Data
BA = Block Address	CSRD = CSR Data
IA = Identifier Address	ID = Identifier Data
PA = Program Address	PD = Program Data
X = Don't Care	

NOTES:

1. Following the Intelligent Identifier command, two read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters data program, erase, or suspend operations.
3. Clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and all BSR.5, BSR.4 and BSR.2 bits. See Status Register definitions.
4. The upper byte of the data bus (D_{8-15}) during command writes is a "Don't Care."

4.3 28F016XD—Enhanced Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data(3)	Oper	Addr	Data(3)
Read Extended Status Register	1	Write	X	xx71H	Read	RA	GSRD BSRD
Lock Block/Confirm		Write	X	xx77H	Write	BA	xxD0H
Upload Status Bits/Confirm	2	Write	X	xx97H	Write	X	xxD0H

ADDRESS
BA = Block Address
RA = Extended Register Address
PA = Program Address
X = Don't Care

DATA
AD = Array Data
BSRD = BSR Data
GSRD = GSR Data

NOTES:
1. RA can be the GSR address or any BSR address. See Figure 4 for the Extended Status Register memory map.
2. Upon device power-up, all BSR lock-bits come up locked. The Upload Status Bits command must be written to reflect the actual lock-bit status.
3. The upper byte of the data bus (D_{8-15}) during command writes is a "Don't Care."

4.4 Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
CSR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	RY/BY# output or WSMS bit must be checked to determine completion of an operation (erase, erase suspend, or data program) before the appropriate Status bit (ESS, ES or DWS) is checked for success.
CSR.6 = ERASE-SUSPEND STATUS 1 = Erase Suspended 0 = Erase In Progress/Completed	
CSR.5 = ERASE STATUS 1 = Error In Block Erasure 0 = Successful Block Erase	If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.
CSR.4 = DATA-WRITE STATUS 1 = Error in Data Program 0 = Data Program Successful	
CSR.3 = V_{PP} STATUS 1 = V_{PP} Error Detect, Operation Abort 0 = V_{PP} OK	The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}'s level only after the Data Program or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min) and above V_{PPH2}(max).
CSR.2–0 = RESERVED FOR FUTURE ENHANCEMENTS These bits are reserved for future use; mask them out when polling the CSR.	

4.5 Global Status Register

WSMS	OSS	DOS	R	R	R	R	R
7	6	5	4	3	2	1	0

GSR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

GSR.6 = OPERATION SUSPEND STATUS
1 = Operation Suspended
0 = Operation in Progress/Completed

GSR.5 = DEVICE OPERATION STATUS
1 = Operation Unsuccessful
0 = Operation Successful or Currently Running

NOTES:
RY/BY# output or WSMS bit must be checked to determine completion of an operation (block lock, suspend, Upload Status Bits, erase or data program) before the appropriate Status bit (OSS or DOS) is checked for success.

GSR.4–0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use; mask them out when polling the GSR.

4.6 Block Status Register

BS	BLS	BOS	R	R	VPPS	VPPL	R
7	6	5	4	3	2	1	0

BSR.7 = BLOCK STATUS 1 = Ready 0 = Busy	**NOTES:** RY/BY# output or BS bit must be checked to determine completion of an operation (block lock, suspend, erase or data program) before the appropriate Status bits (BOS, BLS) is checked for success.
BSR.6 = BLOCK LOCK STATUS 1 = Block Unlocked for Program/Erase 0 = Block Locked for Program/Erase	
BSR.5 = BLOCK OPERATION STATUS 1 = Operation Unsuccessful 0 = Operation Successful or Currently Running	
BSR.2 = V_{PP} STATUS 1 = V_{PP} Error Detect, Operation Abort 0 = V_{PP} OK	
BSR.1 = V_{PP} LEVEL 1 = V_{PP} Detected at 5.0V ± 10% 0 = V_{PP} Detected at 12.0V ± 5%	BSR.1 is not guaranteed to report accurate feedback between the V_{PPH1} and V_{PPH2} voltage ranges. Programs and erases with V_{PP} between V_{PPLK}(max) and V_{PPH1} (min), between V_{PPH1}(max) and V_{PPH2}(min), and above V_{PPH2}(max) produce spurious results and should not be attempted. BSR.1 was a RESERVED bit on the 28F016SA.
BSR.4,3,0 = RESERVED FOR FUTURE ENHANCEMENTS These bits are reserved for future use; mask them out when polling the BSRs.	

5.0 ELECTRICAL SPECIFICATIONS

NOTICE: This is a production datasheet. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

5.1 Absolute Maximum Ratings*

Temperature Under Bias ....0°C to +80°C

Storage Temperature ....–65°C to +125°C

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

V_{CC} = 3.3V ± 0.3V Systems

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	–0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2,3	–0.2	14.0	V	
V	Voltage on any Pin (except V_{CC},V_{PP}) with Respect to GND	2,5	–0.5	V_{CC} + 0.5	V	
I	Current into any Non-Supply Pin	5		± 30	mA	
I_{OUT}	Output Short Circuit Current	4		100	mA	

V_{CC} = 5.0V ± 0.5V Systems

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	–0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2,3	–0.2	14.0	V	
V	Voltage on any Pin (except V_{CC},V_{PP}) with Respect to GND	2,5	–2.0	7.0	V	
I	Current into any Non-Supply Pin	5		± 30	mA	
I_{OUT}	Output Short Circuit Current	4		100	mA	

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is –0.5V on input/output pins. During transitions, this level may undershoot to –2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. This specification also applies to pins marked "NC."

5.2 Capacitance

For a 3.3V ± 0.3V System:

Sym	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A = +25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = +25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1,2		50	pF	

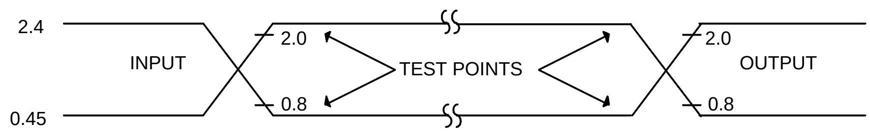
For 5.0V ± 0.5V System:

Sym	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A = +25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = +25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1,2		100	pF	

NOTE:

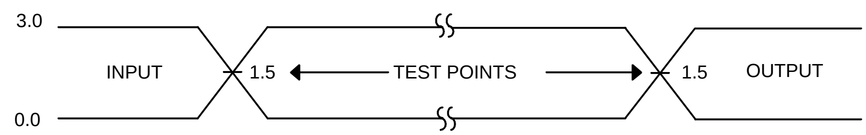
1. Sampled, not 100% tested.
2. To obtain iBIS models for the 28F016XD, please contact your local Intel/Distribution Sales Office.

5.3 Transient Input/Output Reference Waveforms



AC test inputs are driven at V_{OH} (2.4 VTTL) for a Logic "1" and V_{OL} (0.45 VTTL) for a Logic "0." Input timing begins at V_{IH} (2.0 VTTL) and V_{IL} (0.8 VTTL). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

Figure 5. Transient Input/Output Reference Waveform for V_{CC} = 5.0V ± 0.5V(1)



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

Figure 6. Transient Input/Output Reference Waveform for V_{CC} = 3.3V ± 0.3V(2)

NOTES:

1. Testing characteristics for 28F016XD-85.
2. Testing characteristics for 28F016XD-95.

5.4 DC Characteristics

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# = Pin Set High for 3.3V Operations

Sym	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
$I_{CC}1$	V_{CC} Word Read Current	1,4,5		50	70	mA	V_{CC} = V_{CC} Max RAS#, CAS# = V_{IL} RAS#, CAS#, Addr. Cycling @ t_{RC} = min I_{OUT} = 0 mA Inputs = TTL or CMOS
$I_{CC}2$	V_{CC} Standby Current	1,5		1	4	mA	V_{CC} = V_{CC} Max RAS#, CAS#, RP# = V_{IH} WP#, 3/5# = V_{IL} or V_{IH}
$I_{CC}3$	V_{CC} RAS#-Only Refresh Current	1,5		50	80	mA	V_{CC} = V_{CC} Max CAS# = V_{IH} RAS# = V_{IL} RAS#, Addr. Cycling @ t_{RC} = min Inputs = TTL or CMOS
$I_{CC}4$	V_{CC} Fast Page Mode Word Read Current	1,4,5		40	70	mA	V_{CC} = V_{CC} Max RAS#, CAS# = V_{IL} CAS#, Addr. Cycling @ t_{PC} = min I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
$I_{CC}5$	V_{CC} Standby Current	1,5		70	130	µA	V_{CC} = V_{CC} Max RAS# CAS# RP# = V_{CC} ± 0.2V WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
$I_{CC}6$	V_{CC} CAS#-before-RAS# Refresh Current	1,5		40	15	mA	V_{CC} = V_{CC} Max CAS#, RAS# = V_{IL} CAS#, RAS#, Addr. Cycling @ t_{RC} = min Inputs = TTL or CMOS
$I_{CC}7$	V_{CC} Standby Current (Self Refresh Mode)	1,5		40	10	mA	V_{CC} = V_{CC} Max RAS#, CAS# = V_{IL} I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
I_{LI}	Input Load Current	1			± 1	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1			± 10	µA	V_{CC} = V_{CC} Max V_{OUT} = V_{CC} or GND
I_{CCD}	V_{CC} Deep Power-Down Current	1		2	10	µA	RP# = GND ± 0.2V

5.4 DC Characteristics (Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# = Pin Set High for 3.3V Operations

Sym	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{CCW}	V_{CC} Word Program Current	1,6		8	12	mA	V_{PP} = 12.0V ± 5% Program in Progress
				8	17	mA	V_{PP} = 5.0V ± 10% Program in Progress
I_{CCE}	V_{CC} Block Erase Current	1,6		6	12	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
				9	17	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		1	4	mA	RAS#, CAS# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby/Read Current	1		± 1	± 10	µA	$V_{PP} \leq V_{CC}$
				30	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5	µA	RP# = GND ± 0.2V
I_{PPW}	V_{PP} Word Program Current	1,6		10	15	mA	V_{PP} = 12.0V ± 5% Program in Progress
				15	25	mA	V_{PP} = 5.0V ± 10% Program in Progress
I_{PPE}	V_{PP} Block Erase Current	1,6		4	10	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
				14	20	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		30	200	µA	Block Erase Suspended
V_{IL}	Input Low Voltage	6	-0.3		0.8	V	
V_{IH}	Input High Voltage	6	2.0		V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage	6			0.4	V	V_{CC} = V_{CC} Min I_{OL} = 4.0 mA
V_{OH1}	Output High Voltage	6	2.4			V	V_{CC} = V_{CC} Min I_{OH} = –2.0 mA
V_{OH2}		6	V_{CC}-0.2			V	V_{CC} = V_{CC} Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Erase/Program Lock Voltage	3,6	0.0		1.5	V	
$V_{PPH}1$	V_{PP} during Program/ Erase Operations	3	4.5	5.0	5.5	V	
$V_{PPH}2$	V_{PP} during Program/ Erase Operations	3	11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Program Lock Voltage		2.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3V, V_{PP} = 12.0V or 5.0V, T = +25°C.
2. I_{CCES} is specified with the device de-selected. If the device is read while in erasesuspend mode, current draw is the sum of I_{CCES} and I_{CC1}/I_{CC4}.
3. Block erases, word programs and lock block operations are inhibited when V_{PP} = V_{PPLK} and not guaranteed in the ranges between $V_{PPLK(max)}$ and $V_{PPH1(min)}$, between $V_{PPH1(max)}$ and $V_{PPH2(min)}$, and above $V_{PPH2(max)}$.
4. Automatic Power Saving (APS) reduces I_{CC1} and I_{CC4} to 3.0 mA typical in static operation.
5. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL inputs are either V_{IL} or V_{IH}.
6. Sampled, but not 100% tested. Guaranteed by design.

5.5 DC Characteristics

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to +70°C
3/5# = Pin Set Low for 5.0V Operations

Sym	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
$I_{CC}1$	V_{CC} Word Read Current	1,4,5		90	120	mA	V_{CC} = V_{CC} Max RAS#, CAS# = V_{IL} RAS#, CAS#, Addr. Cycling @ t_{RC} = min I_{OUT} = 0 mA Inputs = TTL or CMOS
$I_{CC}2$	V_{CC} Standby Current	1,5		2	4	mA	V_{CC} = V_{CC} Max RAS#, CAS#, RP# = V_{IH} WP#, 3/5# = V_{IL} or V_{IH}
$I_{CC}3$	V_{CC} RAS#-Only Refresh Current	1,5		90	145	mA	V_{CC} = V_{CC} Max CAS# = V_{IH} RAS# = V_{IL} RAS#, Addr. Cycling @ t_{RC} = min Inputs = TTL or CMOS
$I_{CC}4$	V_{CC} Fast Page Mode Word Read Current	1,4,5		80	130	mA	V_{CC} = V_{CC} Max RAS#, CAS# = V_{IL} CAS#, Addr. Cycling @ t_{PC} = min I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
$I_{CC}5$	V_{CC} Standby Current	1,5		70	130	µA	V_{CC} = V_{CC} Max RAS#,CAS#,RP# = V_{CC} ± 0.2V WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
$I_{CC}6$	V_{CC} CAS#-before-RAS# Refresh Current	1,5		50	15	mA	V_{CC} = V_{CC} Max CAS#, RAS# = V_{IL} CAS#, RAS#, Addr. Cycling @ t_{RC} = min Inputs = TTL or CMOS
$I_{CC}7$	V_{CC} Standby Current (Self Refresh Mode)	1,5		50	10	mA	V_{CC} = V_{CC} Max RAS#, CAS# = V_{IL} I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
I_{LI}	Input Load Current	1			± 1	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1			± 10	µA	V_{CC} = V_{CC} Max V_{OUT} = V_{CC} or GND
I_{CCD}	V_{CC} Deep Power-Down Current	1		2	10	µA	RP# = GND ± 0.2V

5.5 DC Characteristics (Continued)

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to +70°C
3/5# = Pin Set Low for 5.0V Operations

Sym	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{CCW}	V_{CC} Word Program Current	1,6		25	35	mA	V_{PP} = 12.0V ± 5% Word Program in Progress
				25	40	mA	V_{PP} = 5.0V ± 10% Word Program in Progress
I_{CCE}	V_{CC} Block Erase Current	1,6		18	25	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
				20	30	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		2	4	mA	RAS#, CAS# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby/Read	1		± 1	± 10	µA	$V_{PP} \leq V_{CC}$
	Current			30	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5	µA	RP# = GND ± 0.2V
I_{PPW}	V_{PP} Word Program Current	1,6		7	12	mA	V_{PP} = 12.0V ± 5% Word Program in Progress
				17	22	mA	V_{PP} = 5.0V ± 10% Word Program in Progress
I_{PPE}	V_{PP} Block Erase Current	1,6		5	10	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
				16	20	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Susp.Current	1		30	200	µA	Block Erase Suspended
V_{IL}	Input Low Voltage	6	–0.5		0.8	V	
V_{IH}	Input High Voltage	6	2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage	6			0.45	V	$V_{CC} = V_{CC}$ Min I_{OL} = 5.8 mA
V_{OH1}	Output High Voltage	6	0.85 V_{CC}			V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.5 mA
V_{OH2}		6	V_{CC}– 0.4			V	$V_{CC} = V_{CC}$ Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Erase/Program Lock Voltage	3,6	0.0		1.5	V	
$V_{PPH}1$	V_{PP} during Program/Erase Operations	3	4.5	5.0	5.5	V	
$V_{PPH}2$	V_{PP} during Program/Erase Operations	3	11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Program Lock Voltage		2.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V or 5.0V, T = +25°C. These currents are specified for a CMOS rise/fall time (10% to 90%) of <5 ns and a TTL rise/fall time of <10 ns.
2. I_{CCES} is specified with the device de-selected. If the device is read while in Erase Suspend mode, current draw is the sum of I_{CCES} and I_{CC1}/I_{CC4}.
3. Block erases, word programs and lock block operations are inhibited when $V_{PP} = V_{PPLK}$ and not guaranteed in the ranges between $V_{PPLK(max)}$ and $V_{PPH1(min)}$, between $V_{PPH1(max)}$ and $V_{PPH2(min)}$, and above $V_{PPH2(max)}$.
4. Automatic Power Saving (APS) reduces I_{CC1} and I_{CC4} to 1 mA typical in static operation.
5. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL inputs are either V_{IL} or V_{IH}.
6. Sampled, not 100% tested. Guaranteed by design.

5.6 AC Characteristics(11)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Read, Program, Read-Modify-Program and Refresh Cycles (Common Parameters)

Versions			28F016XD-95		Units
Sym	Parameter	Notes	Min	Max	
t_{RP}	RAS# precharge time		10		ns
t_{CP}	CAS# precharge time		15		ns
t_{ASR}	Row address set-up time	9	0		ns
t_{RAH}	Row address hold time	9	15		ns
t_{ASC}	Column address set-up time	9	0		ns
t_{CAH}	Column address hold time	9	20		ns
t_{AR}	Column address hold time referenced to RAS#	3,9	35		ns
t_{RAD}	RAS# to column address delay time	8,9	15	15	ns
t_{CRP}	CAS# to RAS# precharge time		10		ns
t_{OED}	OE# to data delay	10	30		ns
t_{DZO}	OE# delay time from data-in	10	0		ns
t_{DZC}	CAS# delay time from data-in	10	0		ns
t_T	Transition time (rise and fall)	10	2	4	ns

Read Cycle

Versions			28F016XD-95		Units
Sym	Parameter	Notes	Min	Max	
$t_{RC(R)}$	Random read cycle time		105		ns
$t_{RAS(R)}$	RAS# pulse width (reads)		95	∞	ns
$t_{CAS(R)}$	CAS# pulse width (reads)		45	∞	ns
$t_{RCD(R)}$	RAS# to CAS# delay time (reads)	1	15	50	ns
$t_{RSH(R)}$	RAS# hold time (reads)		30		ns
$t_{CSH(R)}$	CAS# hold time (reads)		95		ns
t_{RAC}	Access time from RAS#	1,8		95	ns
t_{CAC}	Access time from CAS#	1,2		40	ns
t_{AA}	Access time from column address	8		75	ns
t_{OEA}	OE# access time			40	ns

Read Cycle (Continued)

Versions			28F016XD-95		Units
Sym	**Parameter**	**Notes**	**Min**	**Max**	
t_{ROH}	RAS# hold time referenced to OE#		40		ns
t_{RCS}	Read command setup time		5		ns
t_{RCH}	Read command hold time referenced to CAS#	6,10	0		ns
t_{RRH}	Read command hold time referenced to RAS#	6,10	0		ns
t_{RAL}	Column address to RAS# lead time	9	15		ns
t_{CAL}	Column address to CAS# lead time	9	75		ns
t_{CLZ}	CAS# to output in Low-Z		0		ns
t_{OH}	Output data hold time		0		ns
t_{OHO}	Output data hold time from OE#		0		ns
t_{OFF}	Output buffer turn-off delay	4		30	ns
t_{OEZ}	Output buffer turn off delay time from OE#			30	ns
t_{CDD}	CAS# to data-in delay time		30		ns

Write Cycle

Versions			28F016XD-95		Units
Sym	**Parameter**	**Notes**	**Min**	**Max**	
$t_{RC(W)}$	Random write cycle time		90		ns
$t_{RAS(W)}$	RAS# pulse width (writes)		80	∞	ns
$t_{CAS(W)}$	CAS# pulse width (writes)		65	∞	ns
$t_{RCD(W)}$	RAS# to CAS# delay time (writes)	1	15	15	ns
$t_{RSH(W)}$	RAS# hold time (writes)		65		ns
$t_{CSH(W)}$	CAS# hold time (writes)		80		ns
t_{WCS}	Write command set-up time	5	0		ns
t_{WCH}	Write command hold time		15		ns
t_{WCR}	Write command hold time referenced to RAS#	3	30		ns
t_{WP}	Write command pulse width		15		ns
t_{RWL}	Write command to RAS# lead time		65		ns
t_{CWL}	Write command to CAS# lead time		65		ns
t_{DS}	Data-in set-up time	7,9	0		ns
t_{DH}	Data-in hold time	7,9	15		ns
t_{DHR}	Data-in hold time referenced to RAS#	3,9	30		ns

Read-Modify-Write Cycle

Versions			28F016XD-95		Units
Sym	Parameter	Notes	Min	Max	
t_{RWC}	Read-modify-write cycle time	10	200		ns
t_{RWD}	RAS# to WE# delay time	5,10	125		ns
t_{CWD}	CAS# to WE# delay time	5,10	75		ns
t_{AWD}	Column address to WE# delay time	5,9,10	105		ns
t_{OEH}	OE# command hold time	10	15		ns

Fast Page Mode Cycle

Versions			28F016XD-95		Units
Sym	Parameter	Notes	Min	Max	
$t_{PC(R)}$	Fast page mode cycle time (reads)		75		ns
$t_{PC(W)}$	Fast page mode cycle time (writes)		80		ns
$t_{RASP(R)}$	RAS# pulse width (reads)		95	∞	ns
$t_{RASP(W)}$	RAS# pulse width (writes)		80	∞	ns
t_{CPA}	Access time from CAS# precharge			85	ns
t_{CPW}	WE# delay time from CAS# precharge	10	0		ns
$t_{CPRH(R)}$	RAS# hold time from CAS# precharge (reads)		75		ns
$t_{CPRH(W)}$	RAS# hold time from CAS# precharge (writes)		80		ns

Fast Page Mode Read-Modify-Write Cycle

Versions			28F016XD-95		Units
Sym	Parameter	Notes	Min	Max	
t_{PRWC}	Fast page mode read-modify-write cycle time	10	170		ns

Refresh Cycle

Versions			28F016XD-95		Units
Sym	Parameter	Notes	Min	Max	
t_{CSR}	CAS# set-up time (CAS#-before-RAS# refresh)	10	10		ns
t_{CHR}	CAS# hold time (CAS#-before-RAS# refresh)	10	10		ns
t_{WRP}	WE# setup time (CAS#-before-RAS# refresh)	10	10		ns
t_{WRH}	WE# hold time (CAS#-before-RAS# refresh)	10	10		ns
t_{RPC}	RAS# precharge to CAS# hold time	10	10		ns
t_{RASS}	RAS# pulse width (self-refresh mode)	10	0		ns
t_{RPS}	RAS# precharge time (self-refresh mode)	10	10		ns
t_{CPN}	CAS# precharge time (self-refresh mode)	10	10		ns
t_{CHS}	CAS# hold time (self-refresh mode)	10	0		ns

Refresh

Versions			28F016XD-95		Units
Sym	Parameter	Notes	Min	Max	
t_{REF}	Refresh period	10		∞	ms

Misc. Specifications

Versions		28F016XD-95		Units
Parameter	Notes	Min	Max	
RP# high to RAS# going low	10	480		ns
RP# set-up to WE# going low	10	480		ns
V_{PP} set-up to CAS# high at end of write cycle	10	100		ns
WE# high to RY/BY# going low	10		100	ns
RP# hold from valid status register data and RY/BY# high	10	0		ns
V_{PP} hold from valid status register data and RY/BY# high	10	0		ns

NOTES:

1. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point.
2. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
3. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
4. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
5. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to the CAS# leading edge in early write cycles and to the WE# leading edge in read-write cycles.
8. Operation within the $t_{RAD(max)}$ limit ensures that $t_{RAC(max)}$ can be met, $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then the access time is controlled by t_{AA}.
9. Refer to command definition tables for valid address and data values.
10. Sampled, but not 100% tested. Guaranteed by design.
11. See AC Input/Output Reference Waveforms for timing measurements.

5.7 AC Characteristics(11)

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to +70°C

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Versions			28F016XD-85		Units
Sym	**Parameter**	**Notes**	**Min**	**Max**	
t_{RP}	RAS# precharge time		10		ns
t_{CP}	CAS# precharge time		15		ns
t_{ASR}	Row address set-up time	9	0		ns
t_{RAH}	Row address hold time	9	15		ns
t_{ASC}	Column address set-up time	9	0		ns
t_{CAH}	Column address hold time	9	20		ns
t_{AR}	Column address hold time referenced to RAS#	3,9	35		ns
t_{RAD}	RAS# to column address delay time	8,9	15	15	ns
t_{CRP}	CAS# to RAS# precharge time		10		ns
t_{OED}	OE# to data delay	10	30		ns
t_{DZO}	OE# delay time from data-in	10	0		ns
t_{DZC}	CAS# delay time from data-in	10	0		ns
t_T	Transition time (rise and fall)	10	2	4	ns

Read Cycle

Versions			28F016XD-85		Units
Sym	**Parameter**	**Notes**	**Min**	**Max**	
$t_{RC(R)}$	Random read cycle time		95		ns
$t_{RAS(R)}$	RAS# pulse width (reads)		85	∞	ns
$t_{CAS(R)}$	CAS# pulse width (reads)		35	∞	ns
$t_{RCD(R)}$	RAS# to CAS# delay time (reads)	1	15	50	ns
$t_{RSH(R)}$	RAS# hold time (reads)		30		ns
$t_{CSH(R)}$	CAS# hold time (reads)		85		ns
t_{RAC}	Access time from RAS#	1,8		85	ns
t_{CAC}	Access time from CAS#	1,2		35	ns
t_{AA}	Access time from column address	8		65	ns
t_{OEA}	OE# access time			35	ns
t_{ROH}	RAS# hold time referenced to OE#		35		ns
t_{RCS}	Read command setup time		5		ns
t_{RCH}	Read command hold time referenced to CAS#	6,10	0		ns
t_{RRH}	Read command hold time referenced to RAS#	6,10	0		ns
t_{RAL}	Column address to RAS# lead time	9	15		ns
t_{CAL}	Column address to CAS# lead time	9	65		ns
t_{CLZ}	CAS# to output in Low-Z	10	0		ns
t_{OH}	Output data hold time	10	0		ns
t_{OHO}	Output data hold time from OE#	10	0		ns
t_{OFF}	Output buffer turn-off delay	4,10		30	ns
t_{OEZ}	Output buffer turn off delay time from OE#	10		30	ns
t_{CDD}	CAS# to data-in delay time	10	30		ns

Write Cycle

Versions			28F016XD-85		Units
Sym	Parameter	Notes	Min	Max	
$t_{RC(W)}$	Random write cycle time		75		ns
$t_{RAS(W)}$	RAS# pulse width (writes)		65	∞	ns
$t_{CAS(W)}$	CAS# pulse width (writes)		50	∞	ns
$t_{RCD(W)}$	RAS# to CAS# delay time (writes)	1	15	15	ns
$t_{RSH(W)}$	RAS# hold time (writes)		50		ns
$t_{CSH(W)}$	CAS# hold time (writes)		65		ns
t_{WCS}	Write command set-up time	5	0		ns
t_{WCH}	Write command hold time		15		ns
t_{WCR}	Write command hold time referenced to RAS#	3	30		ns
t_{WP}	Write command pulse width		15		ns
t_{RWL}	Write command to RAS# lead time		50		ns
t_{CWL}	Write command to CAS# lead time		50		ns
t_{DS}	Data-in set-up time	7,9	0		ns
t_{DH}	Data-in hold time	7,9	15		ns
t_{DHR}	Data-in hold time referenced to RAS#	3,9	30		ns

Read-Modify-Write Cycle

Versions			28F016XD-85		Units
Sym	Parameter	Notes	Min	Max	
t_{RWC}	Read-modify-write cycle time	10	175		ns
t_{RWD}	RAS# to WE# delay time	5,10	115		ns
t_{CWD}	CAS# to WE# delay time	5,10	65		ns
t_{AWD}	Column address to WE# delay time	5,9,10	100		ns
t_{OEH}	OE# command hold time	10	15		ns

Fast Page Mode Cycle

Versions			28F016XD-85		Units
Sym	Parameter	Notes	Min	Max	
$t_{PC(R)}$	Fast page mode cycle time (reads)		65		ns
$t_{PC(W)}$	Fast page mode cycle time (writes)		65		ns

Fast Page Mode Cycle Continued

Versions			28F016XD-85		Units
Sym	Parameter	Notes	Min	Max	
$t_{RASP(R)}$	RAS# pulse width (reads)		85	∞	ns
$t_{RASP(W)}$	RAS# pulse width (writes)		65	∞	ns
t_{CPA}	Access time from CAS# precharge			70	ns
t_{CPW}	WE# delay time from CAS# precharge	10	0		ns
$t_{CPRH(R)}$	RAS# hold time from CAS# precharge (reads)		65		ns
$t_{CPRH(W)}$	RAS# hold time from CAS# precharge (writes)		65		ns

Fast Page Mode Read-Modify-Write Cycle

Versions			28F016XD-85		Units
Sym	Parameter	Notes	Min	Max	
t_{PRWC}	Fast page mode read-modify-write cycle time	10	145		ns

Refresh Cycle

Versions			28F016XD-85		Units
Sym	Parameter	Notes	Min	Max	
t_{CSR}	CAS# set-up time (CAS#-before-RAS# refresh)	10	10		ns
t_{CHR}	CAS# hold time (CAS#-before-RAS# refresh)	10	10		ns
t_{WRP}	WE# setup time (CAS#-before-RAS# refresh)	10	10		ns
t_{WRH}	WE# hold time (CAS#-before-RAS# refresh)	10	10		ns
t_{RPC}	RAS# precharge to CAS# hold time	10	10		ns
t_{RASS}	RAS# pulse width (self-refresh mode)	10	0		ns
t_{RPS}	RAS# precharge time (self-refresh mode)	10	10		ns
t_{CPN}	CAS# precharge time (self-refresh mode)	10	10		ns
t_{CHS}	CAS# hold time (self-refresh mode)	10	0		ns

Refresh

Versions			28F016XD-85		Units
Sym	Parameter	Notes	Min	Max	
t_{REF}	Refresh period	10		∞	ms

Misc. Specifications

Versions		28F016XD-85		Units
Parameter	**Notes**	**Min**	**Max**	
RP# high to RAS# going low	10	300		ns
RP# set-up to WE# going low	10	300		ns
V_{PP} set-up to CAS# high at end of write cycle	10	100		ns
WE# high to RY/BY# going low	10		100	ns
RP# hold from valid status register data and RY/BY# high	10	0		ns
V_{PP} hold from valid status register data and RY/BY# high	10	0		ns

NOTES:

1. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point.
2. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
3. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
4. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
5. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to the CAS# leading edge in early write cycles and to the WE# leading edge in read-write cycles.
8. Operation within the $t_{RAD(max)}$ limit ensures that $t_{RAC(max)}$ can be met, $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then the access time is controlled by t_{AA}.
9. Refer to command definition tables for valid address and data values.
10. Sampled, but not 100% tested. Guaranteed by design.
11. See AC Input/Output Reference Waveforms for timing measurements.

5.8 AC Waveforms

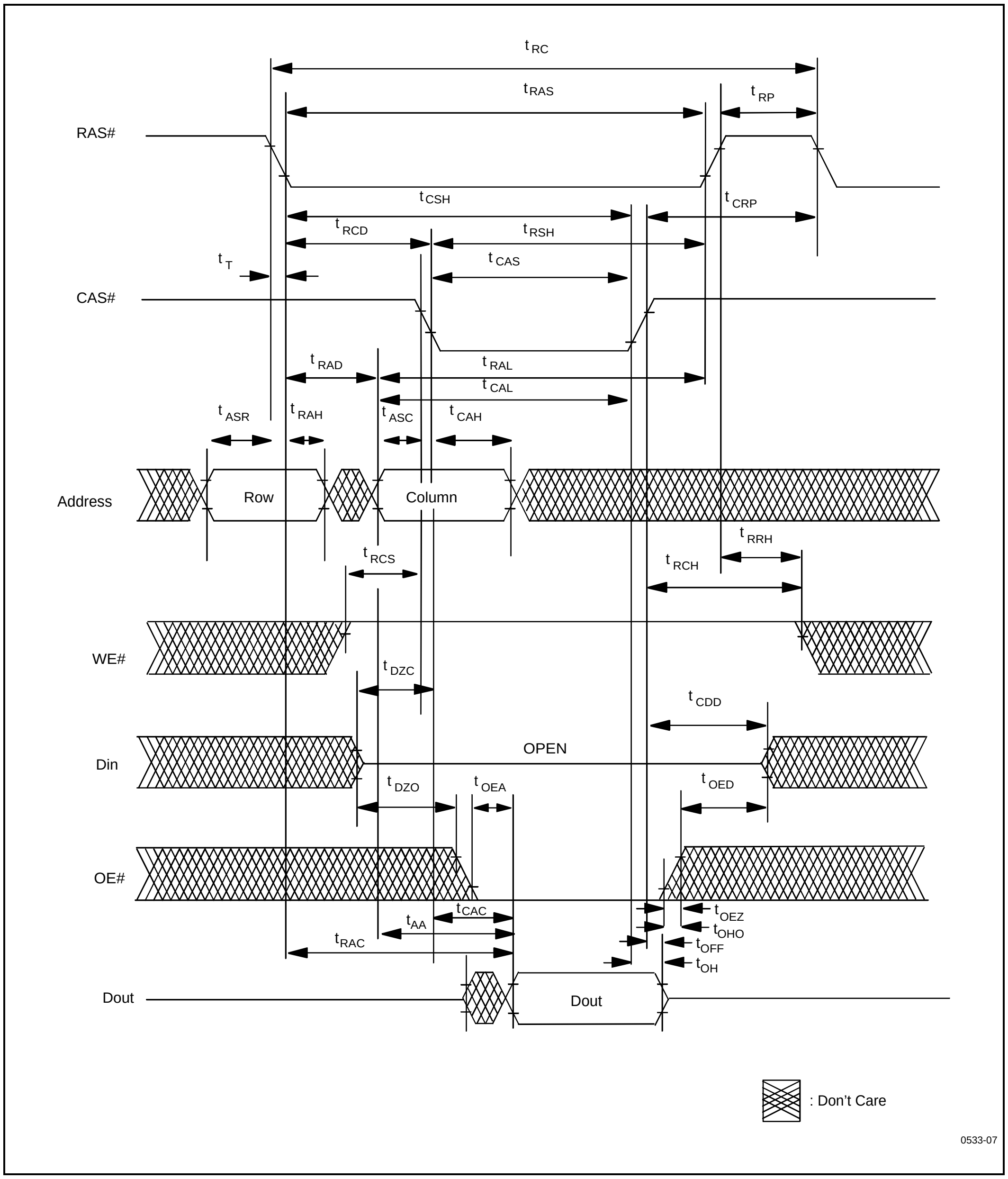


Figure 7. AC Waveforms for Read Operations

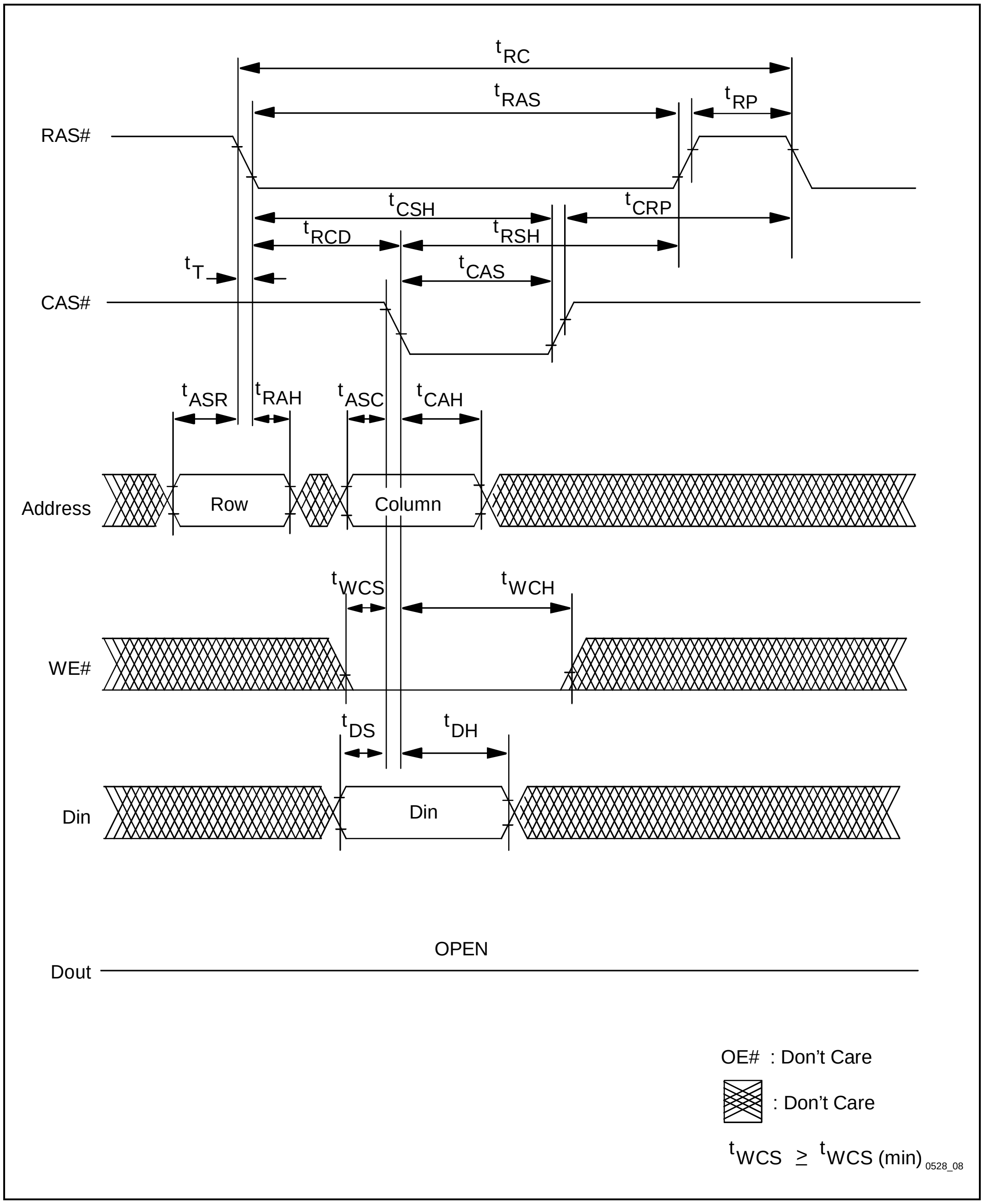


Figure 8. AC Waveforms for Early Write Operations

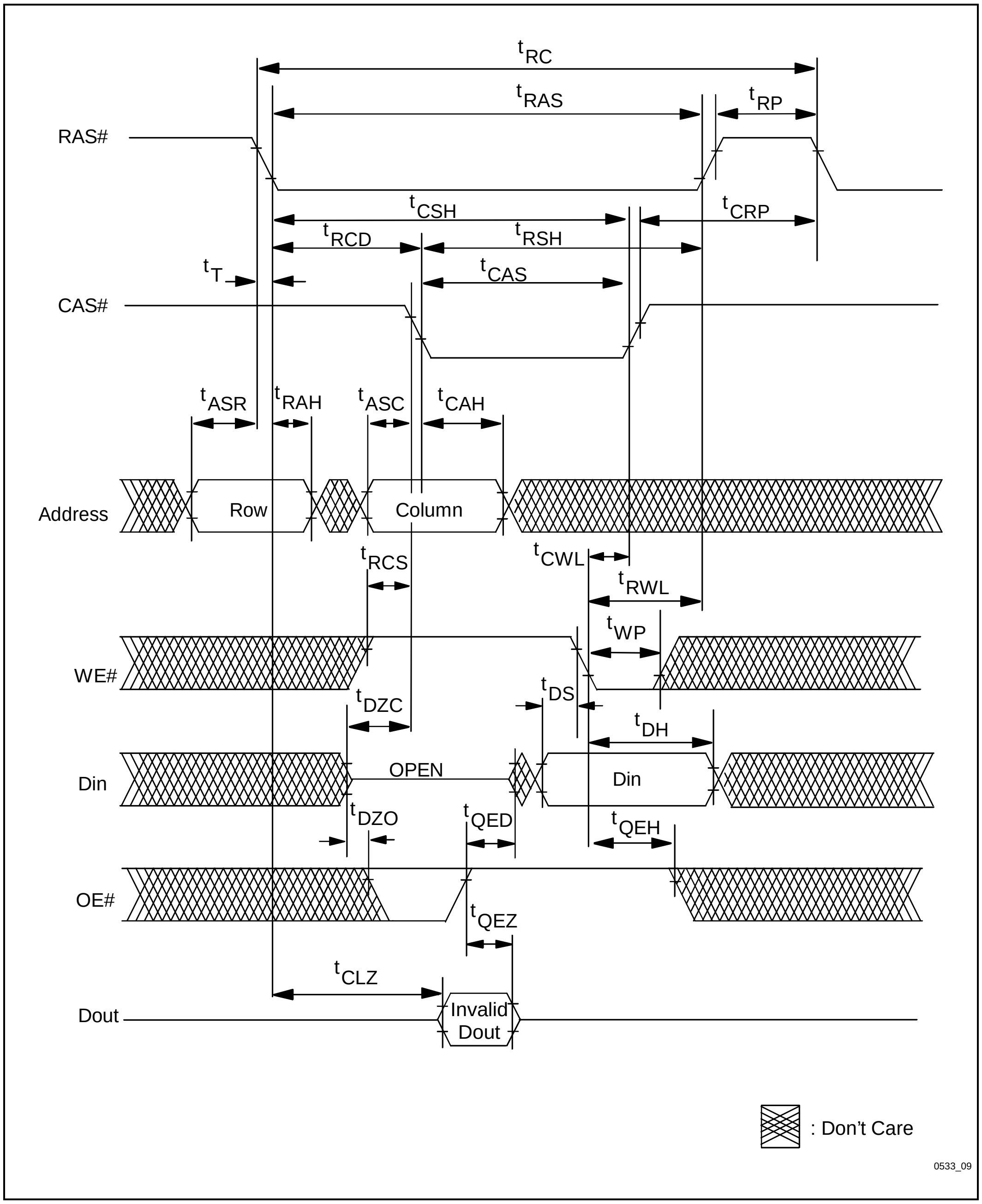


Figure 9. AC Waveforms for Delayed Write Operations

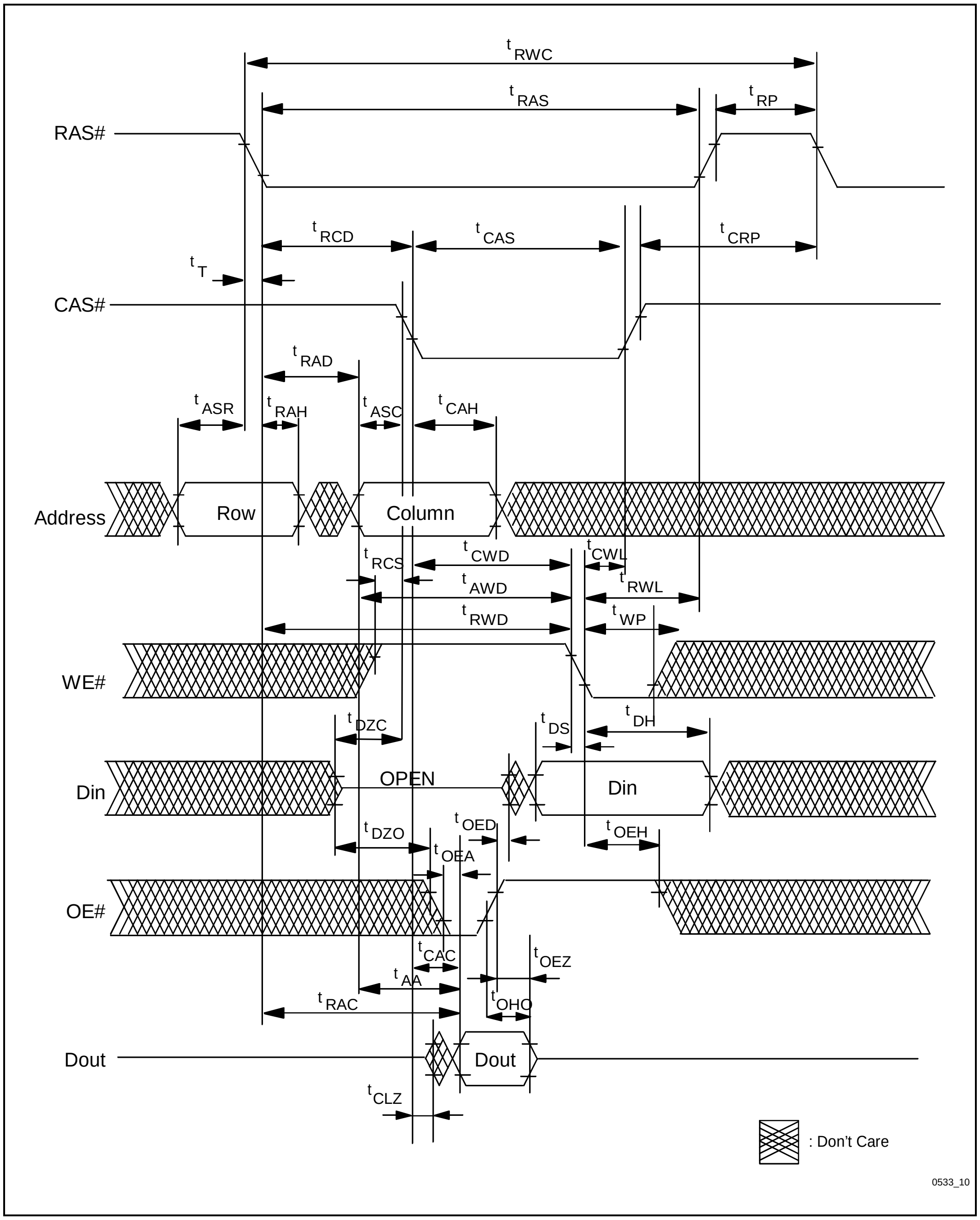


Figure 10. AC Waveforms for Read-Modify-Write Operations

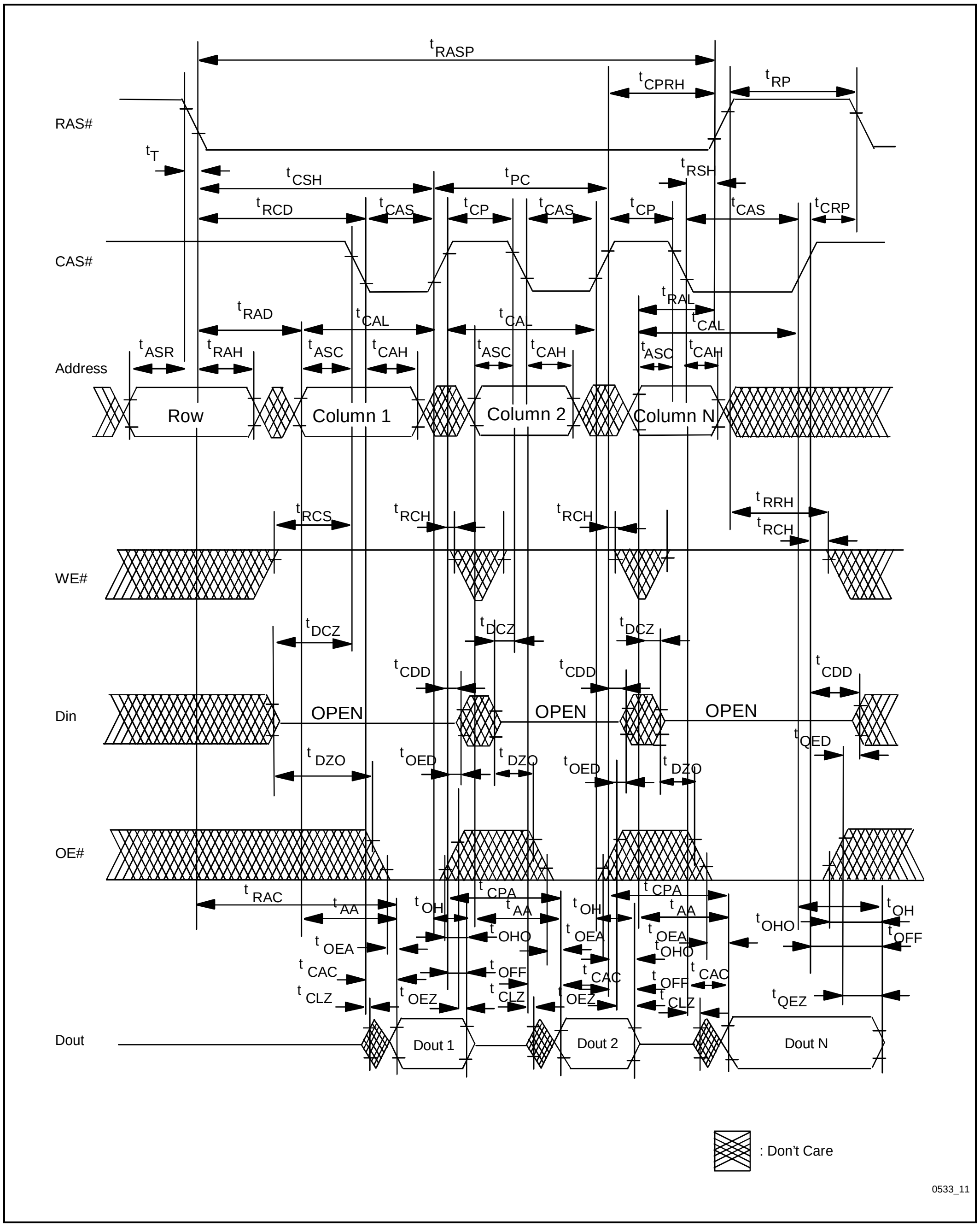


Figure 11. AC Waveforms for Fast Page Mode Read Operations

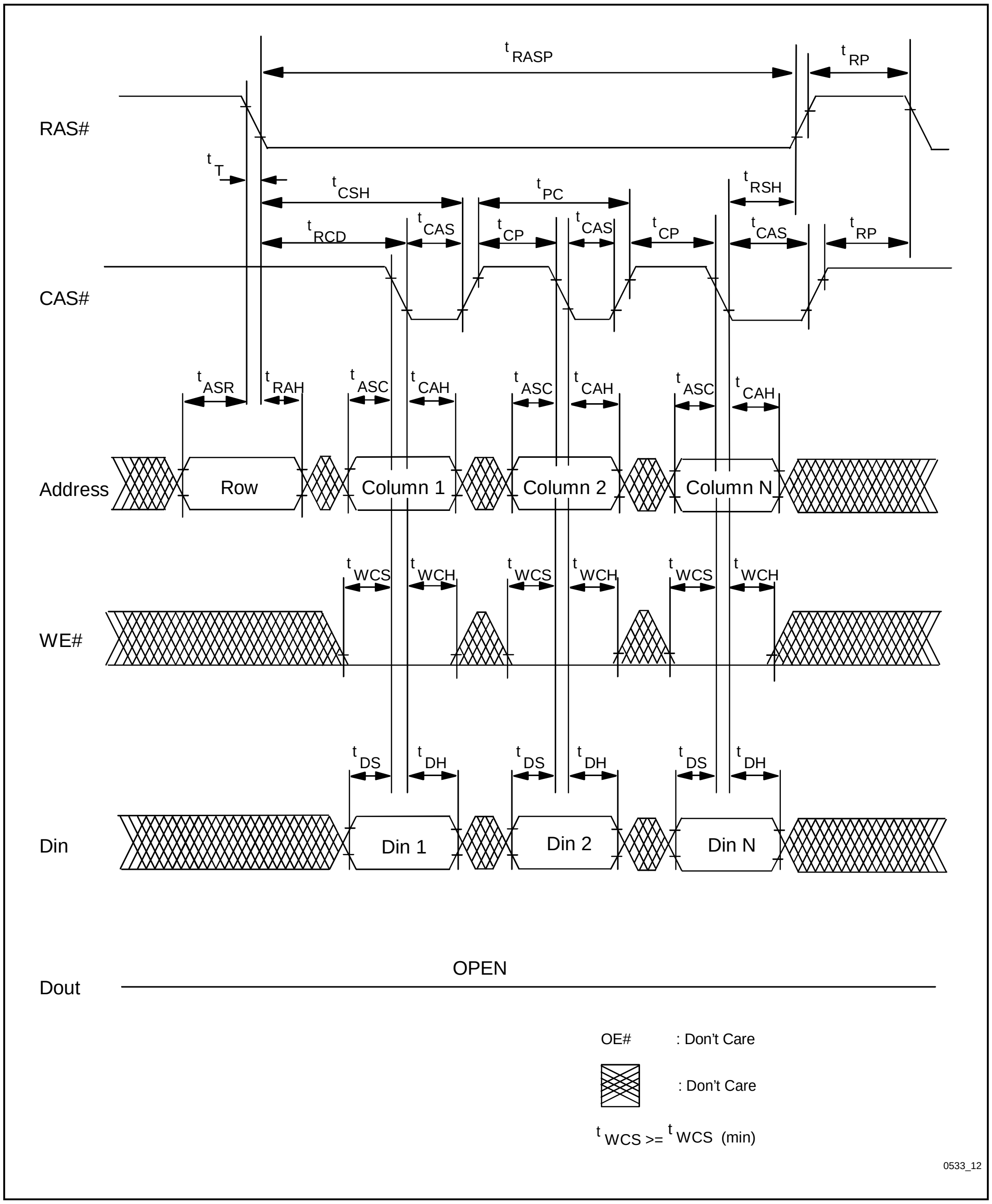


Figure 12. AC Waveforms for Fast Page Mode Early Write Operations

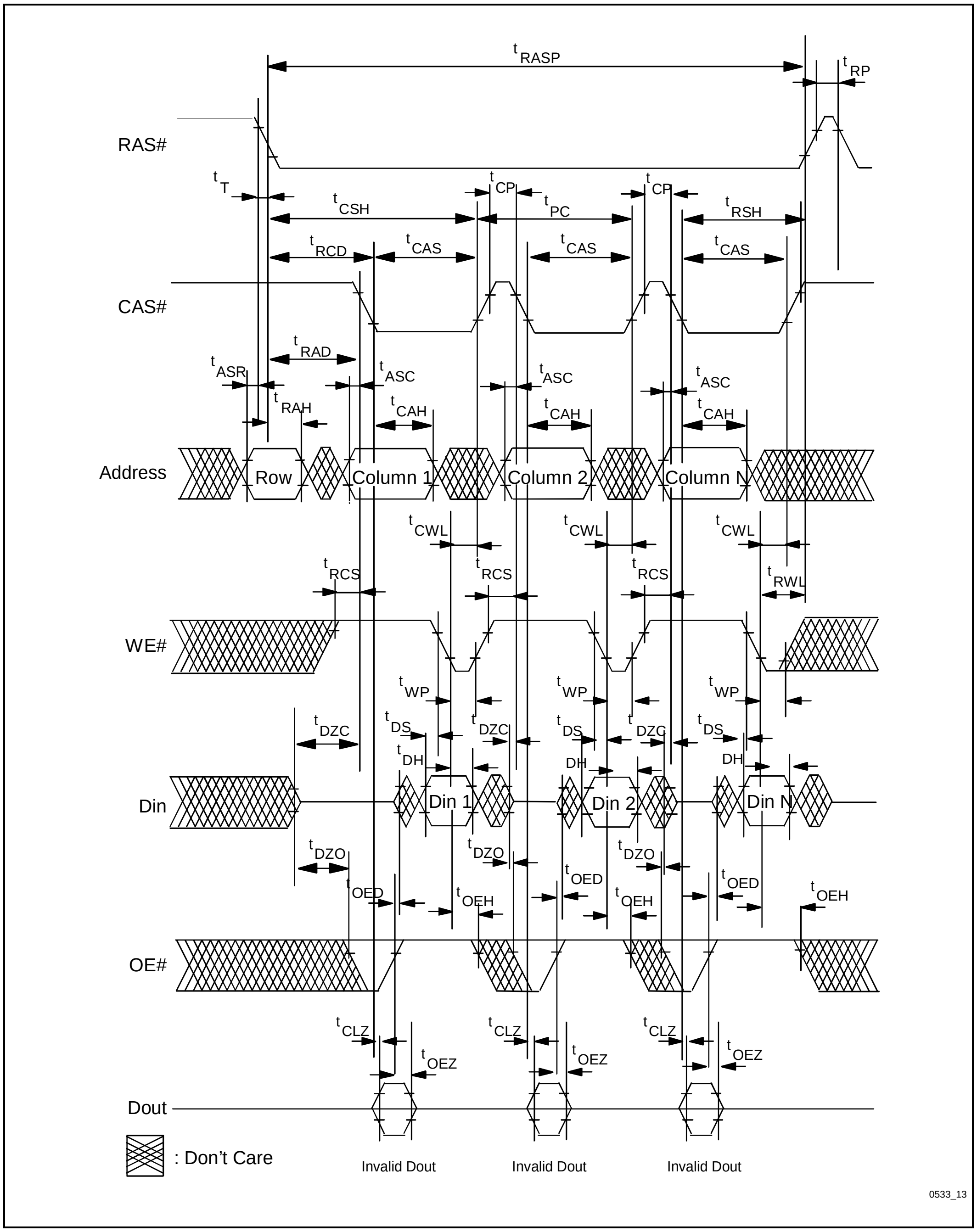


Figure 13. AC Waveforms for Fast Page Mode Delayed Write Operations

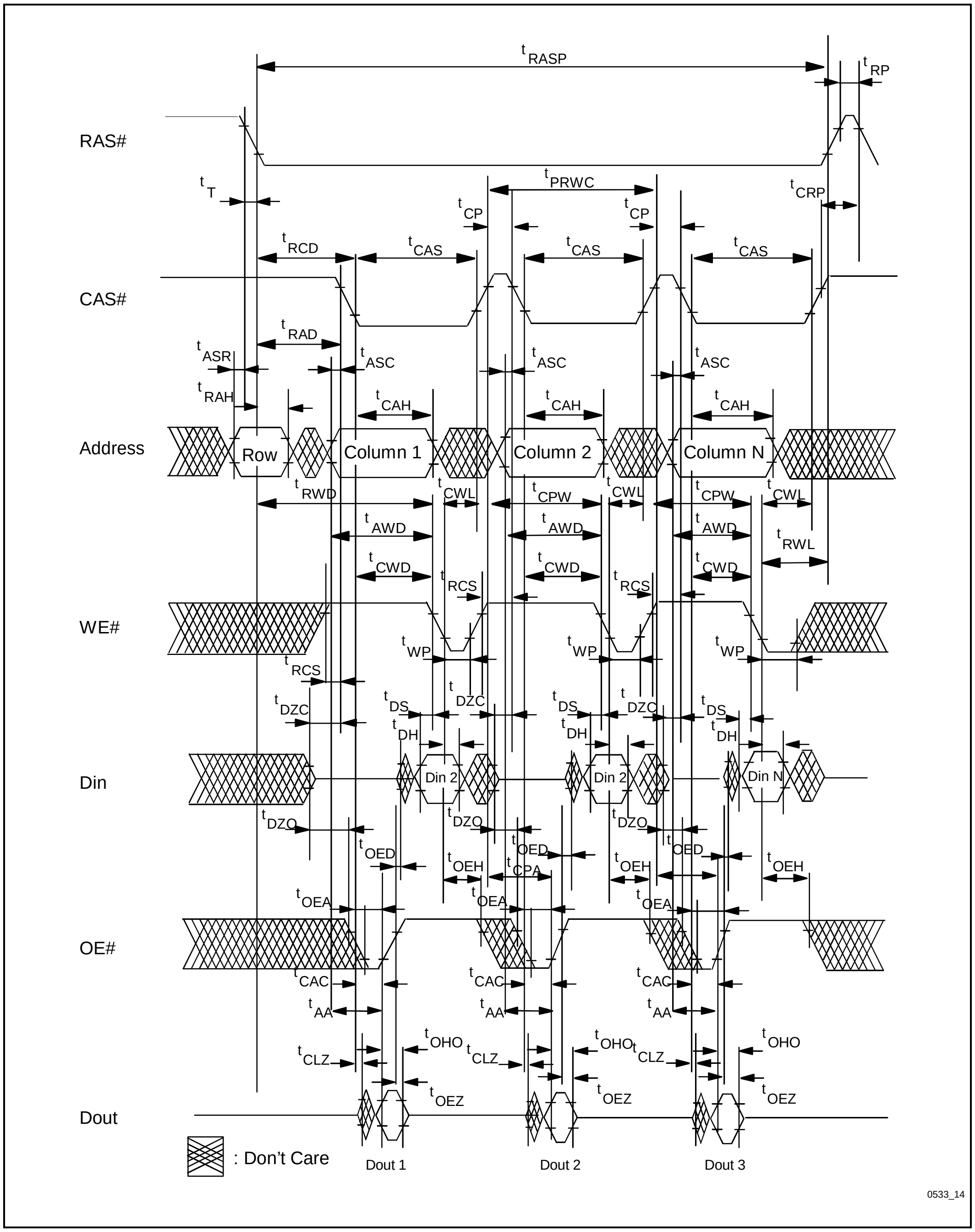


Figure 14. AC Waveforms for Fast Page Mode Read-Modify-Write Operations

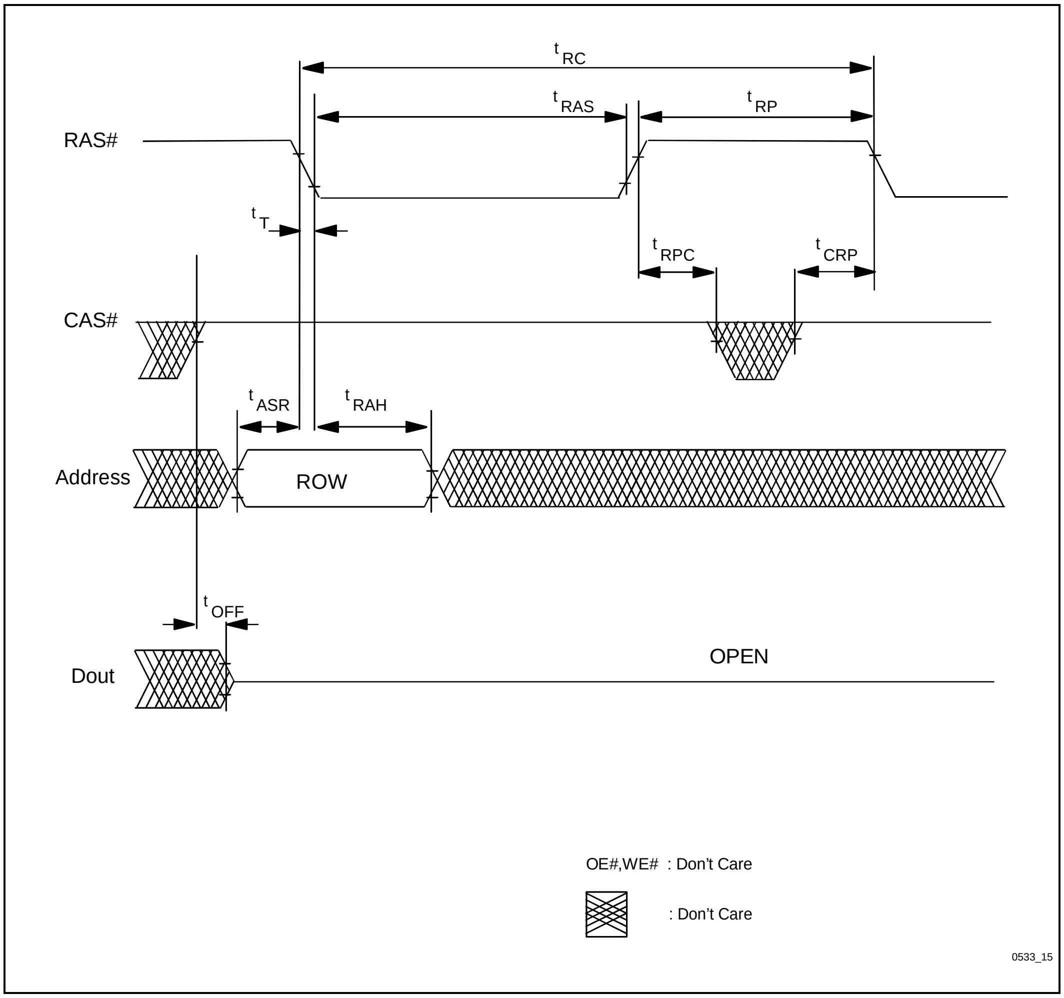


Figure 15. AC Waveforms for RAS#-Only Refresh Operations

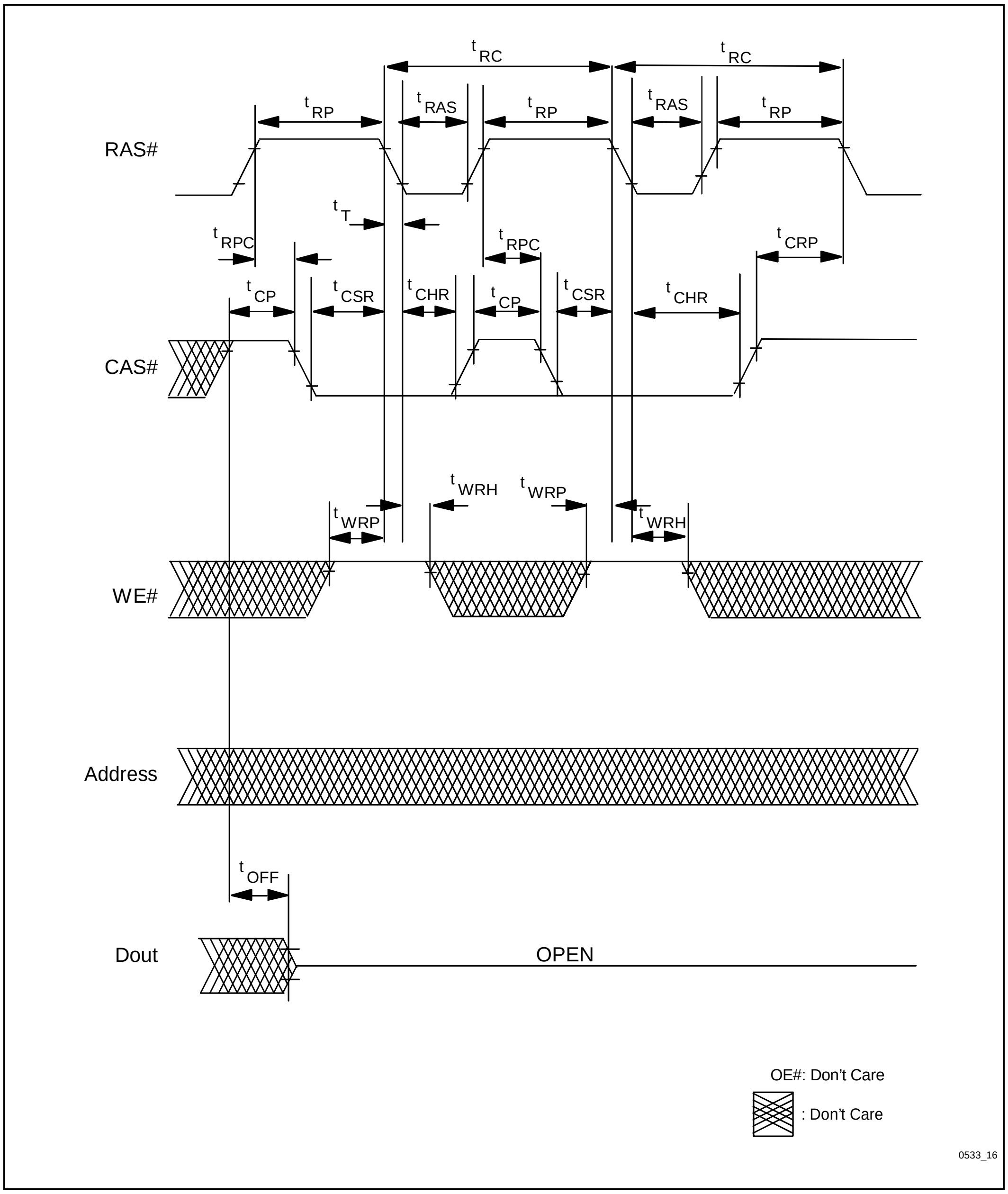


Figure 16. AC Waveforms for CAS#-before-RAS# Refresh Operations

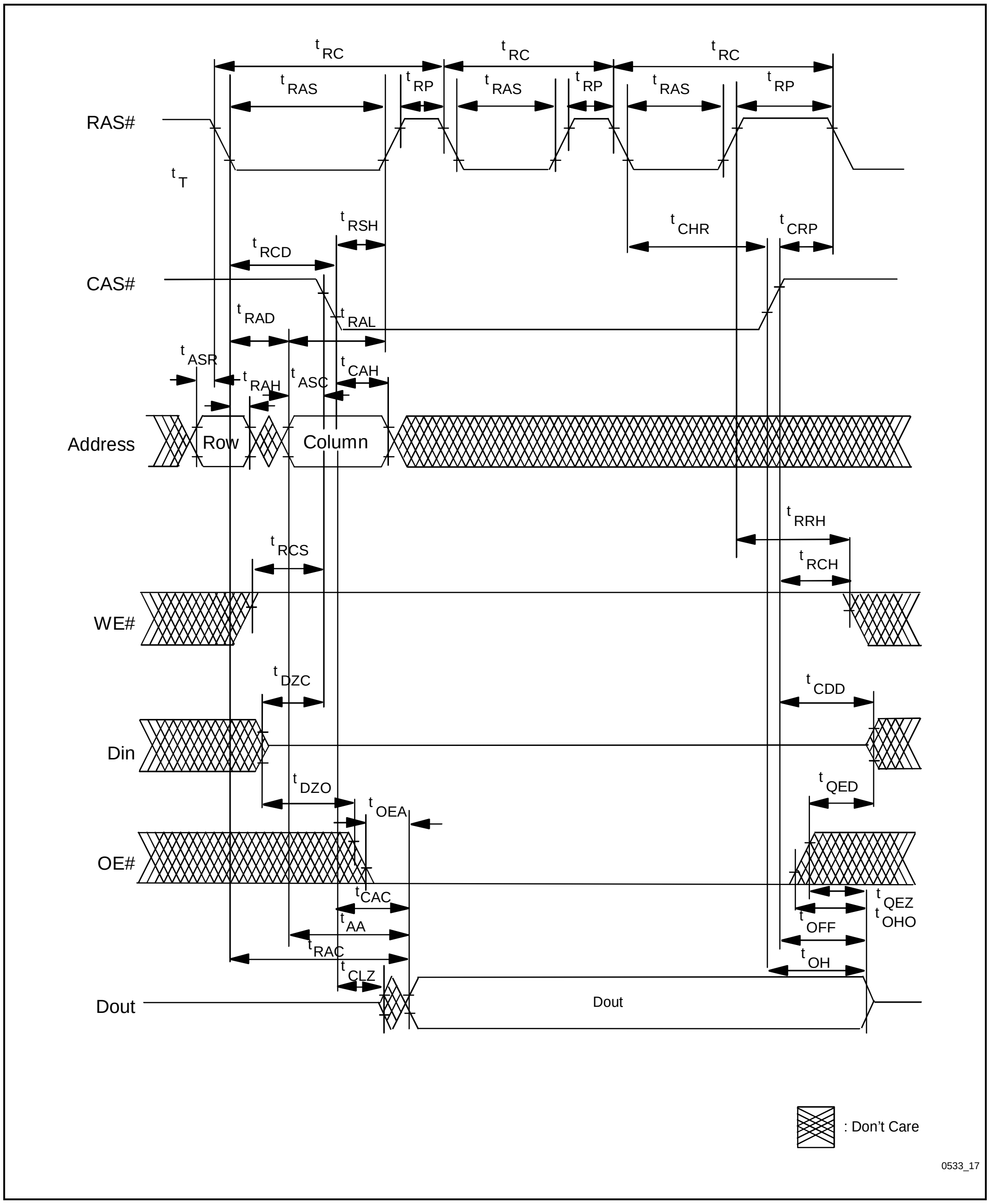


Figure 17. AC Waveforms for Hidden Refresh Operations

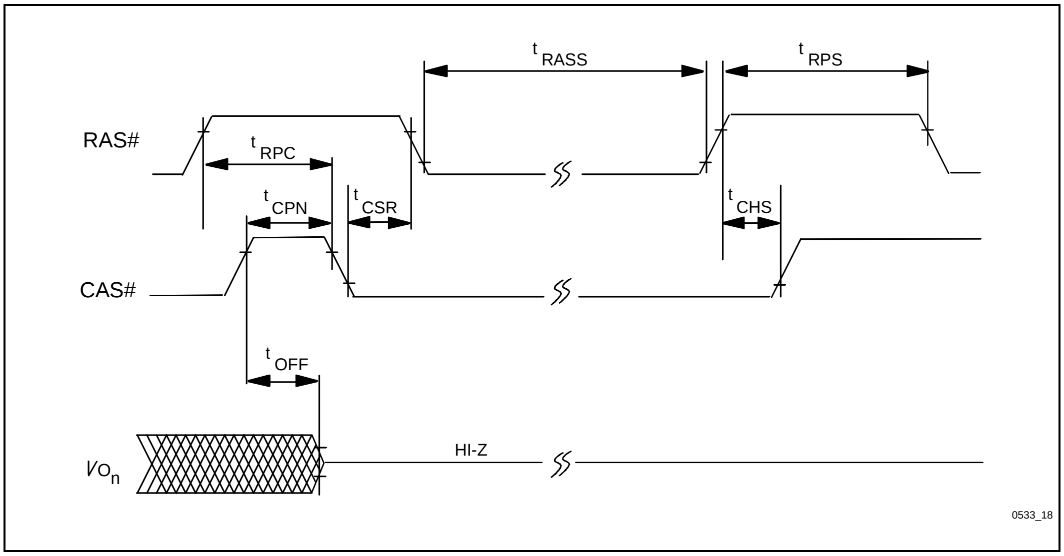


Figure 18. AC Waveforms for Self-Refresh Operations

5.9 Power-Up and Reset Timings

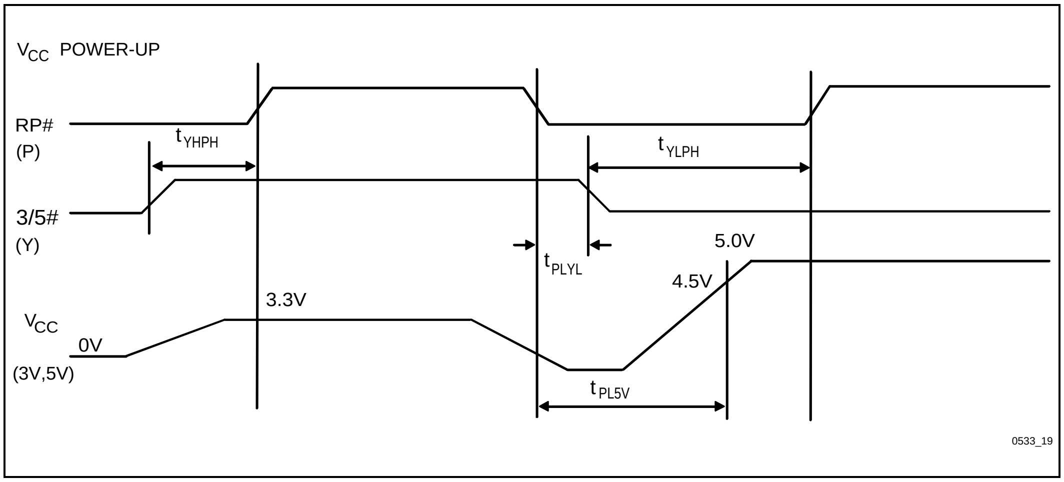


Figure 19. V_{CC} Power-Up and RP# Reset Waveforms

Symbol	Parameter	Notes	Min	Max	Units
t_{PLYL} t_{PLYH}	RP# Low to 3/5# Low (High)		0		µs
t_{YLPH} t_{YHPH}	3/5# Low (High) to RP# High		0		µs
t_{PL5V} t_{PL3V}	RP# Low to V_{CC} at 4.5V (Minimum) RP# Low to V_{CC} at 3.0V (Min) or 3.6V (Max)	2	0		µs

NOTES:

For Read Timings following Reset, see sections 5.6 and 5.7.

1. The t_{YLPH} and/or t_{YHPH} times must be strictly followed to guarantee all other read and write specifications for the 28F016XD
2. The power supply may start to switch concurrently with RP# going low.

5.10 Erase and Word Program Performance(3,4)

V_{CC} = 3.3V ± 0.3V, V_{PP} = 5.0V ± 0.5V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
$t_{WHRH}1$	Word Program Time	2,5	TBD	35.0	TBD	µs
$t_{WHRH}3$	Block Program Time	2,5	TBD	1.2	TBD	sec
	Block Erase Time	2,5	TBD	1.4	TBD	sec
	Erase Suspend Latency Time to Read		1.0	12.0	75.0	µs

V_{CC} = 3.3V ± 0.3V, V_{PP} = 12.0V ± 0.6V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
$t_{WHRH}1$	Word Program Time	2,5	5	9	TBD	µs
$t_{WHRH}3$	Block Program Time	2,5	TBD	0.3	1.0	sec
	Block Erase Time	2	0.3	0.8	10	sec
	Erase Suspend Latency Time to Read		1.0	9.0	55.0	µs

V_{CC} = 5.0V ± 0.5V, V_{PP} = 5.0V ± 0.5V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
$t_{WHRH}1$	Word Program Time	2,5	TBD	25.0	TBD	µs
$t_{WHRH}3$	Block Program Time	2,5	TBD	0.85	TBD	sec
	Block Erase Time	2,5	TBD	1.0	TBD	sec
	Erase Suspend Latency Time to Read		1.0	9.0	55.0	µs

V_{CC} = 5.0V ± 0.5V, V_{PP} = 12.0V ± 0.6V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
$t_{WHRH}1$	Word Program Time	2,5	4.5	6	TBD	µs
$t_{WHRH}3$	Block Program Time	2,5	TBD	0.2	1.0	sec
	Block Erase Time	2	0.3	0.6	10	sec
	Erase Suspend Latency Time to Read		1.0	7.0	40.0	µs

NOTES:
1. +25°C, and nominal voltages.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled, but not 100% tested. Guaranteed by design.
5. Please contact Intel's Application Hotline or your local sales office for more information for current TBD information.

6.0 MECHANICAL SPECIFICATIONS

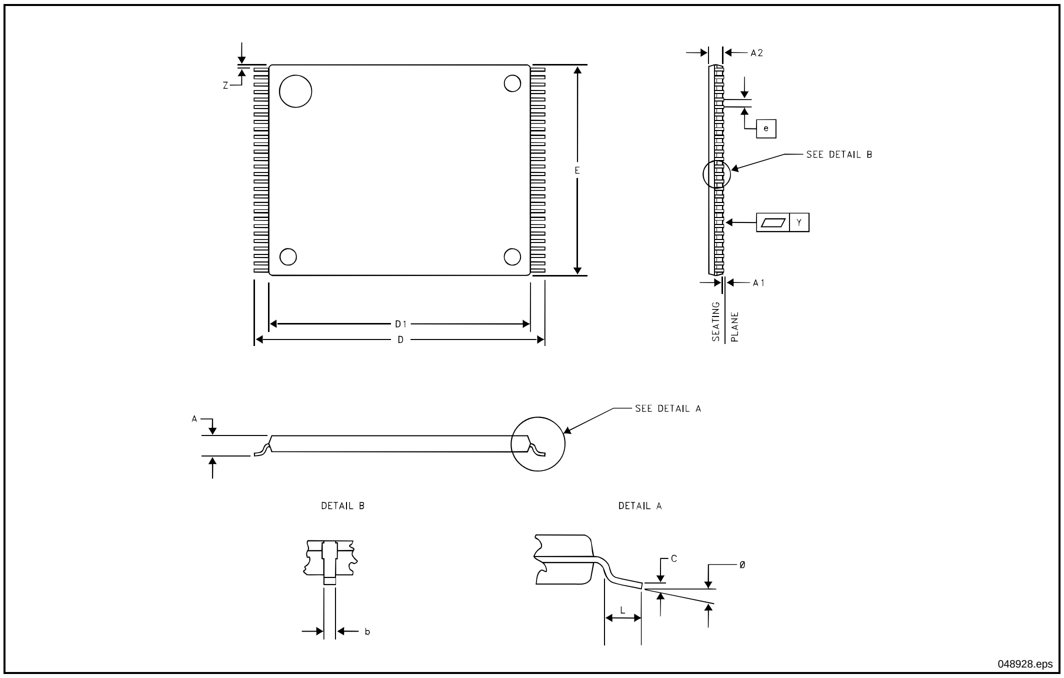
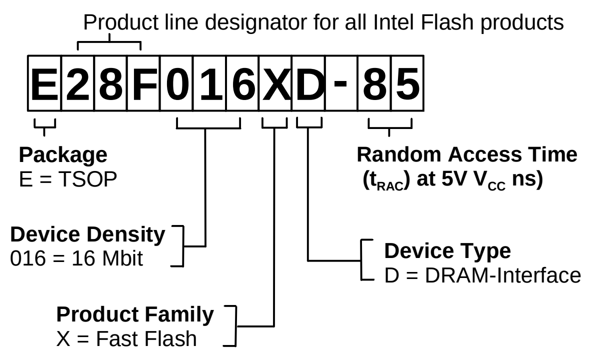


Figure 20. Mechanical Specifications of the 28F016XD 56-Lead TSOP Type I Package

Family: Thin Small Out-Line Package				
Symbol	**Millimeters**			**Notes**
	Minimum	**Nominal**	**Maximum**	
A			1.20	
A_1	0.050			
A_2	0.965	0.995	1.025	
b	0.100	0.150	0.200	
c	0.115	0.125	0.135	
D_1	18.20	18.40	18.60	
E	13.80	14.00	14.20	
e		0.50		
D	19.80	20.00	20.20	
L	0.500	0.600	0.700	
N		56		
∅	0°	3°	5°	
Y			0.100	
Z	0.150	0.250	0.350	

APPENDIX A
DEVICE NOMENCLATURE AND ORDERING INFORMATION



Order Code	Valid Combinations	
	V_{CC} = 3.3V ± 0.3V, 50 pF load, 1.5V I/O Levels(1)	V_{CC} = 5.0V ± 10%, 100 pF load, TTL I/O Levels(1)
E28F016XD 85	E28F016XD-95	E28F016XD-85

NOTE:

1. See Section 5.3 for Transient Input/Output Reference Waveforms.

APPENDIX B
ADDITIONAL INFORMATION[1,2]

Order Number	Document/Tool
297372	*16-Mbit Flash Product Family User's Manual*
292092	*AP-357 Power Supply Solutions for Flash Memory*
292123	*AP-374 Flash Memory Write Protection Techniques*
292126	*AP-377 16-Mbit Flash Product Family Software Drivers, 28F016SA/SV/XD/XS*
292131	*AP-384 Designing with the 28F016XD*
292163	*AP-610 Flash Memory In-System Code and Data Update Techniques*
292168	*AP-614 Adapting DRAM Based Designs for the 28F016XD*
292152	*AB-58 28F016XD-Based SIMM Designs*
292165	*AB-62 Compiled Code Optimizations for Flash Memories*
294016	*ER-33 ETOX™ Flash Memory Technology—Insight to Intel's Fourth Generation Process Innovation*
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	28F016XD Benchmark Utility
Contact Intel/Distribution Sales Office	Flash Cycling Utility
Contact Intel/Distribution Sales Office	28F016XD iBIS Models
Contact Intel/Distribution Sales Office	28F016XD VHDL/Verilog Models
Contact Intel/Distribution Sales Office	28F016XD TimingDesigner* Library Files
Contact Intel/Distribution Sales Office	28F016XD Orcad and ViewLogic Schematic Symbols

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.