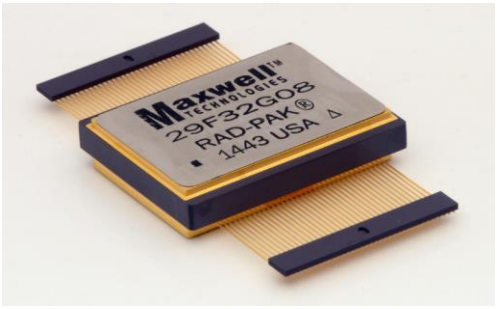
NAND Flash Module
29F32G08

Preliminary



FEATURES:

NAND Flash Interface

Single Level Cell (SLC) Technology
ONFI 2.2 Compliant

Operating Voltage

VCC 3.0 - 3.6V
VCCQ 1.7 - 1.95V or 3.0-3.6V

High density

32Gbit per FLASH NAND die
Supports higher speed designs with less capacitance/fewer I/O's to drive

Page Size

8640 bytes (8192 + 448 spare bytes)
Supports external BCH correction algorithms (16 bit correction per 540 bytes)

Features

High reliability data storage for demanding space applications
Ceramic hermetic package with built-in TID shielding
Class E, I, B or S

Speed

Can be used in asynch or synch mode
Asynch: Up to asynch timing mode 5 (50MT/sec)
Synch: Up to synchronous timing mode 5 (200MT/sec)

Temperature Range

-55°C to 125°C

Endurance

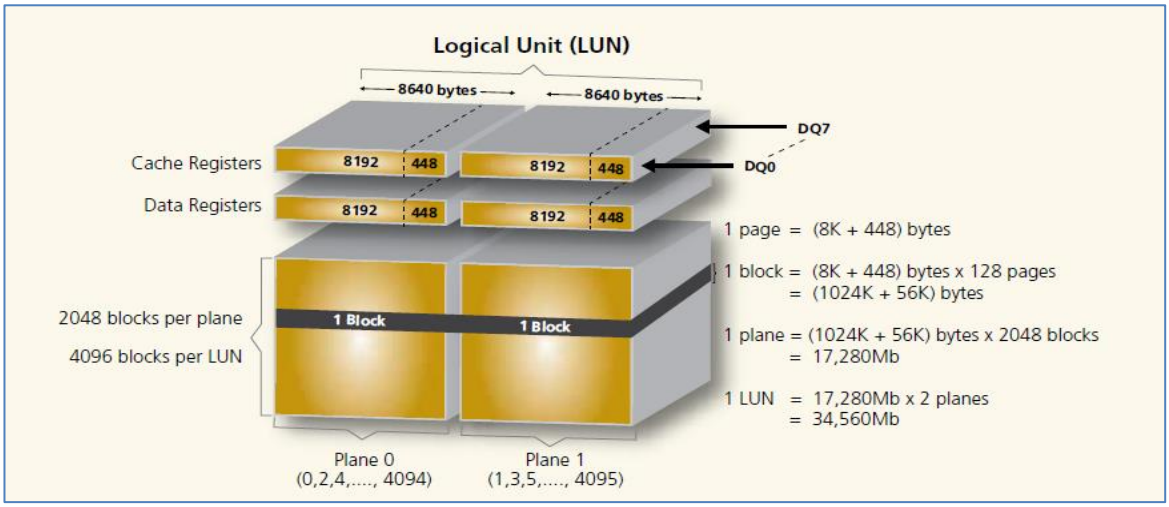
60,000 cycles

Supported Features
ONFI 1.0, 2.0, 2.1, 2.2
Interleaved (multi-plane) operations
Multiple LUN operations
Small Data Move
Interleaved Address restrictions for cache operations
No interleaved block address restrictions
Overlapped/concurrent interleaving supported
Supports timing modes: 0 thru 5
Supports driver strength settings: underdrive, overdrive 1 and 2

Supported Commands:
Reset
Synchronous Reset
Reset LUN
Get Features
Set Features
Read Status
Read Status Enchanced
Change Row Address
Read Mode
Read Page Interleaved
Read Page Cache Sequential
Read Page Cache Random
Read Page Cache Last
Program Page
Program Page Interleaved
Program Page Cache
Erase Block
Erase Block Interleaved
Copyback Read
Copyback Program
Copyback Program Interleaved
Read Unique ID
Read Parameter Page
Read ID

Not Supported
Odd to Even Page Copyback
Non-sequential page programming
16 bit data bus width per Target/LUN
Extended ECC
Synchronous Mode: clock stopped for data input

Array Organization

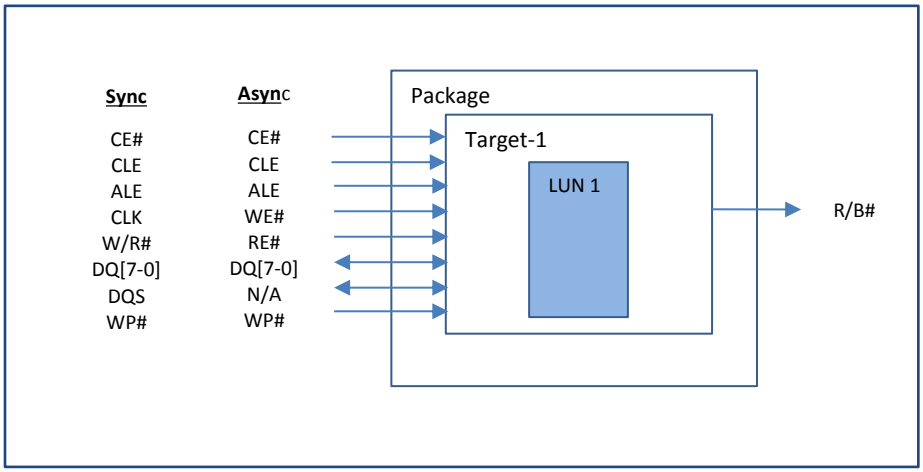


Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	L	L	CA13	CA12	CA11	CA10	CA9	CA8
Third	BA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	L	L	L	L	LUN	BA18	BA17	BA16

CA[n] = Column Address
PA[n] = Page Address
BA[n] = Bank Address
LUN = Logical Unit Address
Row Address = LUN, Bank, Page Address
BA[7] = Plane select
Column Addresses above 8639 are invalid (page size = 8192 + 448)

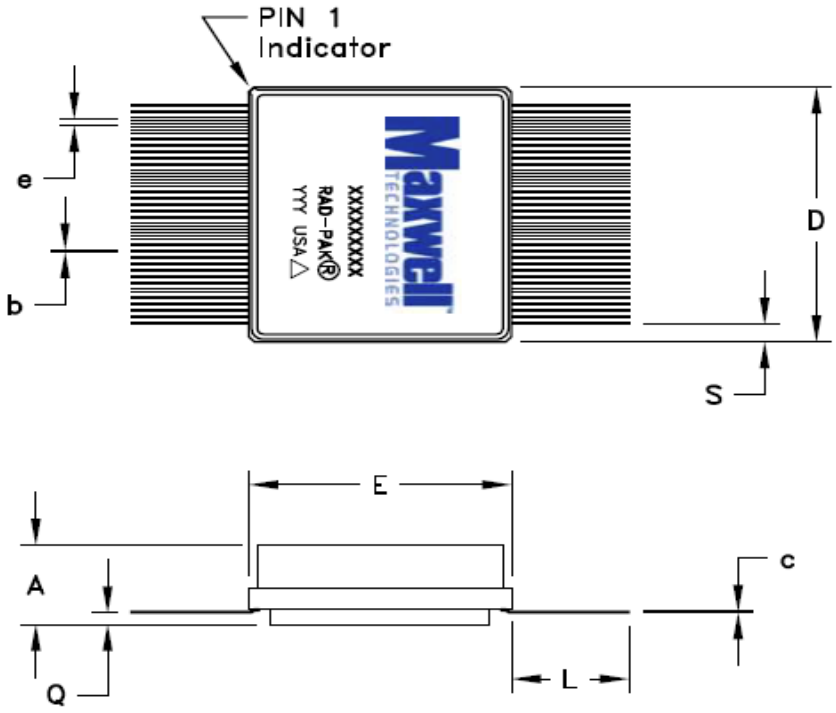
Memory Organizatoin
Bytes per page: 8192
Spare ECC bytes per page: 448
Pages per block: 128
Blocks per LUN: 4096
LUNs per chip enable: 2; 64G16 is 1 LUN per chip enable
Column address cycles: 2
Row address cycles: 3
Bits per cell: 1
Bad blocks maximum per LUN: 80
Block endurance: 60,000
Programs per page: 4
Number of bits ECC required: 8 (for 512 Bytes)
Number of interleave address bits: 1

Package Organization 29F32G08



Architecture

Independent 8 bit buses per package: 1
Targets per 8 bit bus: 1
LUNS per Target: 1
(1 die per 8 bit bus)
(1 die per package)



256G, 68 LEAD FLAT PACKAGE			
	DIMENSION		
SYMBOL	MIN	NOM	MAX
A	0.241	0.260	0.279
b	0.006	0.008	0.010
c	0.005	0.006	0.007
D	0.985	1.000	1.015
e		0.025 BSC	
E	0.810	0.82	0.830
L	0.390	0.400	0.410
Q	0.014	0.021	0.029
S	0.064	0.084	0.104
NOTE: ALL DIMENSIONS IN INCHES			

Pinout

32G08				32G08
Pin Description	Pin #		Pin #	Pin Description
VSS	1		68	VSS
VCC	2		67	NC
WP#	3		66	NC
WE#/CLK	4		65	NC
ALE	5		64	NC
CLE	6		63	NC
NC	7		62	NC
CE	8		61	NC
RE#/WR#	9		60	NC
RB#	10		59	NC
VSS	11		58	VSS
VCC	12		57	NC
VSS	13		56	VSS
VSSQ	14		55	NC
VCCQ	15		54	NC
DQ7	16		53	NC
DQ6	17		52	NC
DQ5	18		51	NC
DQ4	19		50	NC
VSSQ	20		49	NC
VCCQ	21		48	NC
VCC	22		47	NC
VSS	23		46	VSS
DQS	24		45	NC
VCCQ	25		44	NC
VSSQ	26		43	NC
DQ3	27		42	NC
DQ2	28		41	NC
DQ1	29		40	NC
DQ0	30		39	NC
VCCQ	31		38	NC
VSSQ	32		37	NC
VSS	33		36	VSS
VCC	34		35	NC

1. NC = Not internally connected

Product Ordering Options