FAIRCHILD
SEMICONDUCTOR™

April 1988
Revised August 1999

29F52•29F53
8-Bit Registered Transceiver

General Description

The 29F52 and 29F53 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-STATE output enable signals are provided for each register. The A_0–A_7 output pins are guaranteed to sink 24 mA while the B_0–B_7 output pins are designed for 64 mA.

The 29F53 is an inverting option of the 29F52. Both transceivers are AMD Am2952/2953 functional equivalents.

Features

- 8-bit registered transceivers
- Separate clock, clock enable and 3-STATE output enable provided for each register
- AMD Am2952/2953 functional equivalents
- Both inverting and non-inverting options available
- 24-Pin slimline package

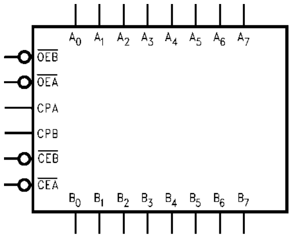
Ordering Code:

Order Number	Package Number	Package Description
29F52SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
29F52SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
29F53SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

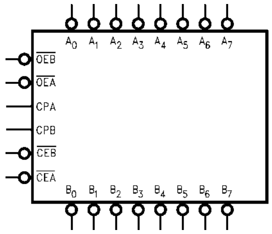
Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Logic Symbols

29F52

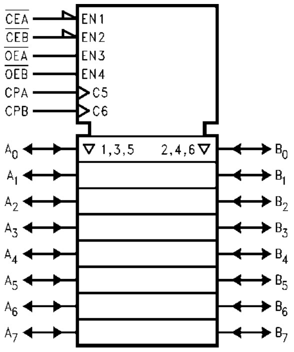


29F53



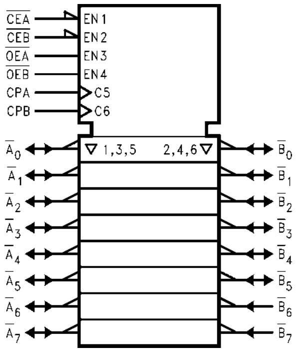
IEEE/IEC

29F52



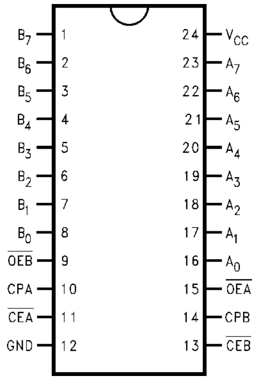
IEEE/IEC

29F53

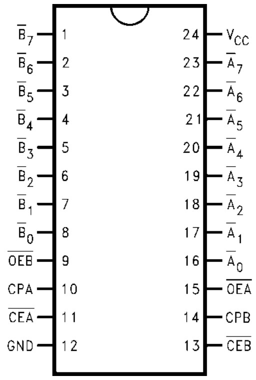


Connection Diagrams

Pin Assignment for DIP and SOIC
29F52



Pin Assignment for DIP
29F53



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$A_0–A_7$	A-Register Inputs/	3.5/1.083	70 µA/0.65 mA
	B-Register 3-STATE Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)
$B_0–B_7$	B Register Inputs/	3.5/1.083	70 µA/0.65 mA
	A-Register 3-STATE Outputs	600/106.6 (80)	–12 mA/64 mA (48 mA)
$\overline{OEA}$	Output Enable A-Register	1.0/1.0	20 µA/–0.6 mA
CPA	A-Register Clock	1.0/1.0	20 µA/–0.6 mA
$\overline{CEA}$	A-Register Clock Enable	1.0/1.0	20 µA/–0.6 mA
$\overline{OEB}$	Output Enable B-Register	1.0/1.0	20 µA/–0.6 mA
CPB	B-Register Clock	1.0/1.0	20 µA/–0.6 mA
$\overline{CEB}$	B-Register Clock Enable	1.0/1.0	20 µA/–0.6 mA

Output Control

OE	Internal Q	Y-Output		Function
		29F52	29F53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

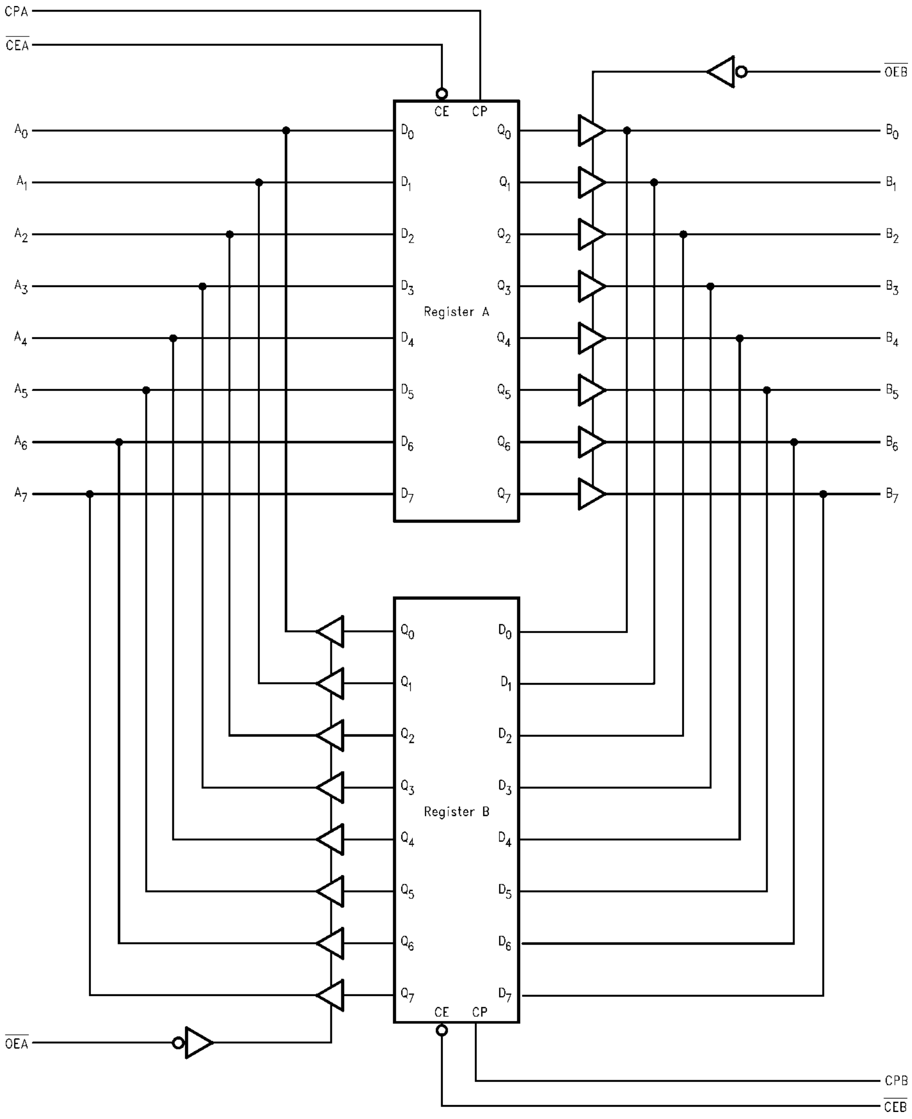
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
N = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	CE		
X	X	H	NC	Hold Data
L	N	L	L	Load Data
H	N	L	H	

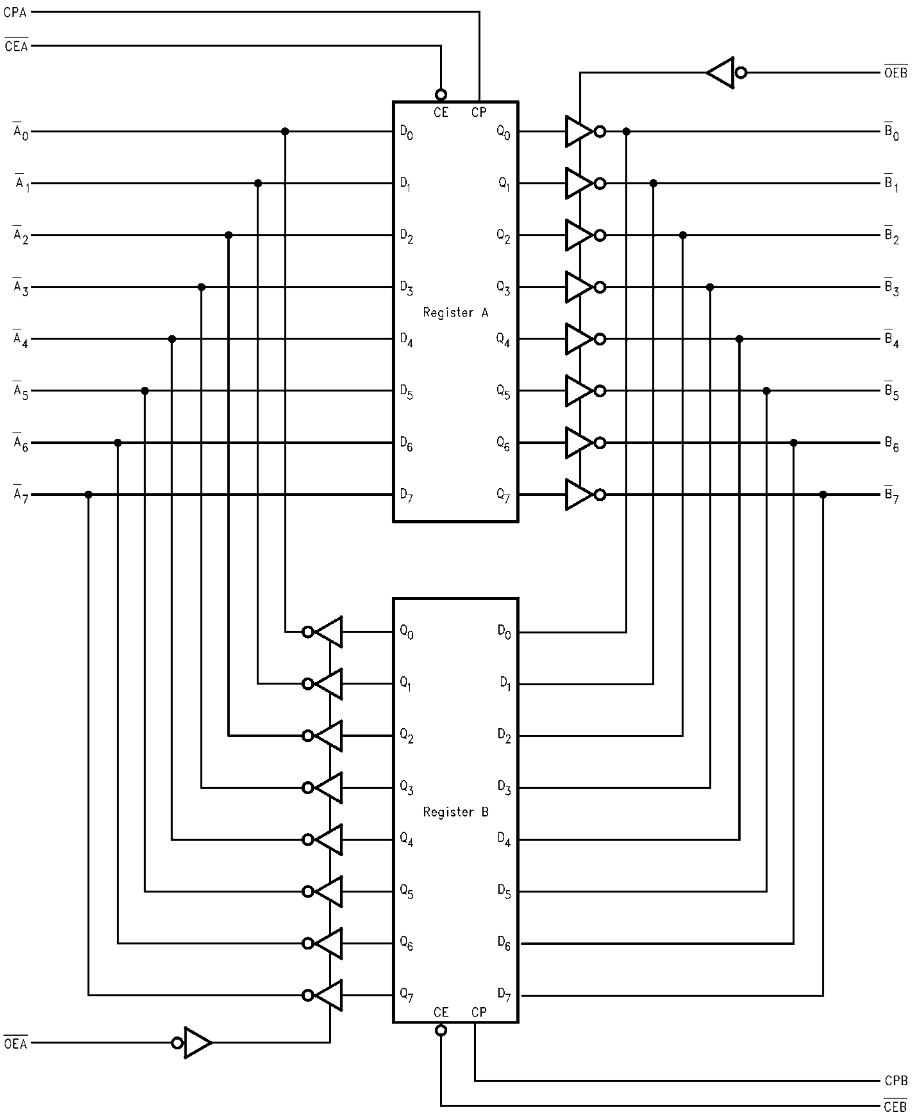
Block Diagrams

29F52



Block Diagrams (continued)

29F53



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (A_n)
	Voltage	10% V_{CC}	2.4					I_{OH} = −3 mA (A_n, B_n)
		10% V_{CC}	2.0					I_{OH} = −15 mA (B_n)
		5% V_{CC}	2.7					I_{OH} = −1 mA (A_n)
		5% V_{CC}	2.7					I_{OH} = −3 mA (A_n, B_n)
V_{OL}	Output LOW	10% V_{CC}			0.5	V	Min	I_{OL} = 24 mA (A_n)
	Voltage	10% V_{CC}			0.55			I_{OL} = 64 mA (B_n)
I_{IH}	Input HIGH Current				20	µA	Max	V_{IN} = 2.7V (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test				100	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				1.0	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				70	µA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	µA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V (A_n)
			−100		−225			V_{OUT} = 0V (B_n)
I_{CEX}	Output HIGH Leakage Current				250	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V (A_n, B_n)
I_{CCH}	Power Supply Current			130	190	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current				190	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current				190	mA	Max	V_O = HIGH Z

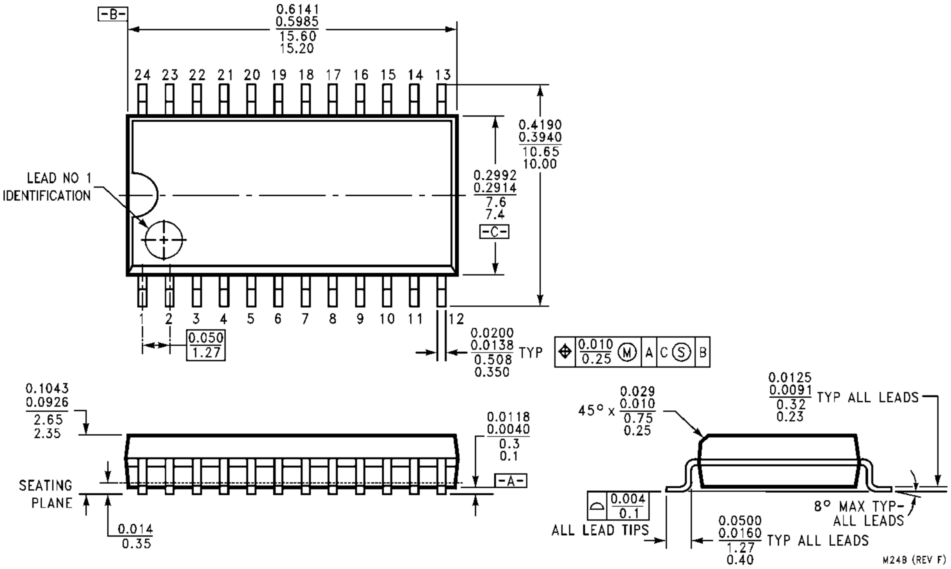
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	5.5	7.5			2.5	8.5	ns
t_{PHL}	CPA or CPB to A_n or B_n	4.0	7.0	9.0			3.5	10.0	
t_{PZH}	Output Enable Time	2.5	5.5	7.5			2.0	8.5	ns
t_{PZL}	$\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	3.5	7.0	9.5			3.0	10.5	
t_{PHZ}	Output Disable Time	2.5	6.5	9.0			2.0	10.0	ns
t_{PLZ}	$\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5	5.5	7.5			2.0	8.5	

AC Operating Requirements

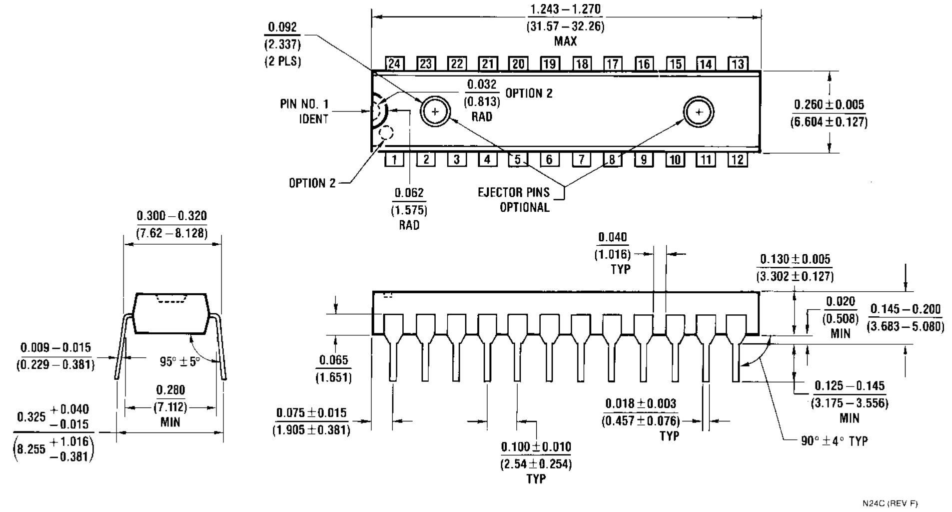
Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$ $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.0				4.5		ns
$t_S(L)$	A_n or B_n to CPA or CPB	4.0				4.5		
$t_H(H)$	Hold Time, HIGH or LOW	2.0				2.5		ns
$t_H(L)$	A_n or B_n to CPA or CPB	2.0				2.5		
$t_S(H)$	Setup Time, HIGH or LOW	1.0				1.5		ns
$t_S(L)$	$\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	4.0				4.5		
$t_H(H)$	Hold Time, HIGH or LOW	2.0				2.5		ns
$t_H(L)$	$\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	2.0				2.5		
$t_W(H)$	Pulse Width, HIGH or LOW	3.0				3.5		ns
$t_W(L)$	CPA or CPB	3.0				3.5		

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
Package Number N24C

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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