FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20901-1E

PAGE MODE FLASH MEMORY

CMOS

128M (8M × 16/4M × 32) BIT

MBM29XL12DF-70/80

■ DESCRIPTION

The MBM29XL12DF is 128M-bit, 3.0 V-only Page mode and dual operation Flash memory organized as 8M words by 16 bits or 4M words by 32 bits. The device is offered in 90-pin SSOP and 96-ball FBGA packages. This device is designed to be programmed in-system with the standard system 3.0 V Vcc supply. 12.0 V Vpp and 5.0 V Vcc are not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

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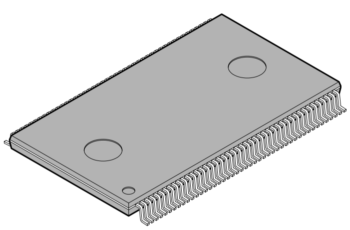
■ PRODUCT LINEUP

Part No.	MBM29XL12DF	
Ordering Part Number Suffix	70	80
V_{CC} (V)	3.0 to 3.6	2.7 to 3.1
Max Random Address Access Time (ns)	70	80
Max Page Address Access Time (ns)	25	30
Max $\overline{CE}$ Access Time (ns)	70	80
Max $\overline{OE}$ Access Time (ns)	25	30

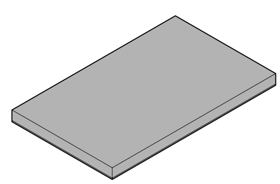
■ PACKAGES

90-pin plastic SSOP



(FPT-90P-M01)

96-ball plastic FBGA



(BGA-96P-M02)

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The device provides truly high performance non-volatile Flash memory solution. The device offers fast page access times of 25 ns and 30 ns with random access times of 70 ns and 80 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls. The page size is 8 words or 4 double words.

The dual operation function provides simultaneous operation by dividing the memory space into four banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the program and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The device is programmed by executing the program command sequence. This will invoke the Embedded Program™ Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margins. Typically, each 32K words sector can be programmed and verified in about 0.3 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase™ Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margins.

Any individual sector is typically erased and verified in 0.5 seconds. (If already preprogrammed.)

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The device is erased when shipped from the factory.

The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits program and erase operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, output pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device memory electrically erases all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The words are programmed one word at a time using the EPROM programming mechanism of hot electron injection.

■ FEATURES

- **0.17 µm Process Technology**
- **Single 3.0 V Read, Program and Erase**
  Minimized system level power requirements
- **Simultaneous Read/Write (Program and Erase) Operations (Dual Bank)**
- **FlexBank™ *1**
  Bank A: 16 Mbit (4K words ×8 and 32K words ×31)
  Bank B: 48 Mbit (32K words ×96)
  Bank C: 48 Mbit (32K words ×96)
  Bank D: 16 Mbit (4K words ×8 and 32K words ×31)
- **High Performance Page Mode**
  25 ns maximum page access time at V_{CC} = 3.0 V to 3.6 V(70 ns random access time)
  30 ns maximum page access time at V_{CC} = 2.7 V to 3.1 V(80 ns random access time)
- **8 Words Page (×16) / 4 Double Words Page (×32) Size**
- **Compatible with JEDEC-Standard Commands**
  Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard World-wide Pinouts**
  90-pin SSOP (Package Suffix : PFV)
  96-ball FBGA (Package Suffix : PBT)
- **Minimum 100,000 Program/Erase Cycles**
- **Sector Erase Architecture**
  Eight 4K words, two hundred fifty -four 32K words, and eight 4K words sectors
  Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Dual Boot Block**
  16 by 4K words bootblock sectors, 8 at the top of the address range and 8 at the bottom of the address range
- **HiddenROM Region**
  128 words of HiddenROM region by using device address of word mode 000000h to 00007Fh (double word mode: 000000h to 00003Fh) accessible through a "HiddenROM Enable" command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **Write Protect Pin ($\overline{WP}$)**
  Write Protect ($\overline{WP}$) function allows protection of "outermost" 2× 4K words on both ends of boot sectors, regardless of sector protection/unprotection status
- **Accelerate Pin (ACC)**
  At V_{ACC}, increases program performance
- **Embedded Erase™ *2 Algorithms**
  Automatically preprograms and erases the chip or any sector
- **Embedded Program™ *2 Algorithms**
  Automatically programs and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit Feature for detection of program or erase cycle completion**
- **Ready/Busy Output** (**RY/$\overline{BY}$**)
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, the device automatically switches itself to low power mode.
- **Low V_{CC} Write Inhibit ≤ V_{LKO}**

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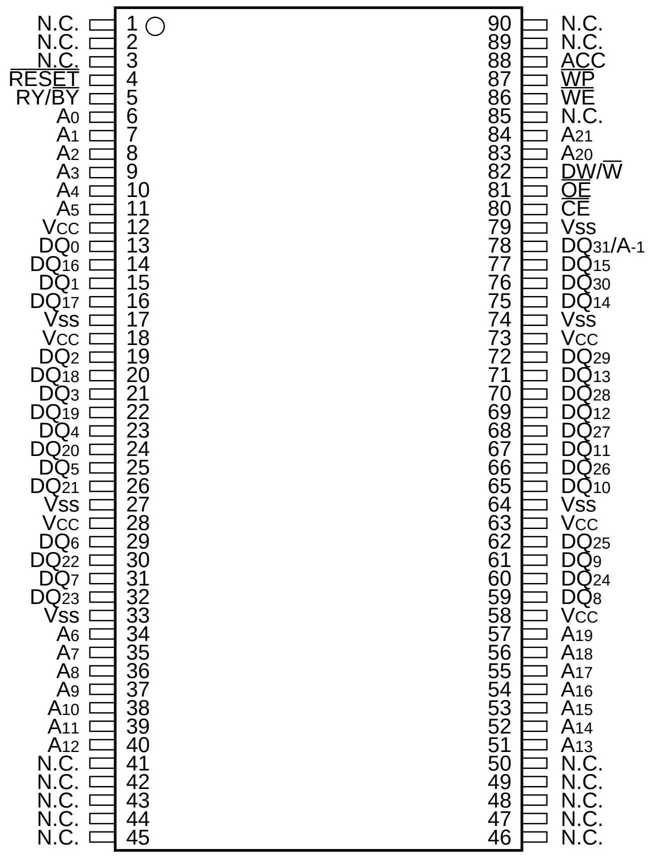
- **Program Suspend/Resume**
  Suspends the program operation to allow a read in another word
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **In accordance with CFI** (**Common Flash Memory Interface**)
- **Hardware Reset Pin (RESET)**
  Hardware method to reset the device for reading array data
- **New Sector Protection**
  Persistent Sector Protection
  Password Sector Protection
- **Hardware Sector Group Protection**
  Hardware method disables any combination of sectors from program or erase operation

*1: FlexBank™ is a trademark of Fujitsu Limited, Japan.

*2: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENTS

SSOP
(TOP VIEW)



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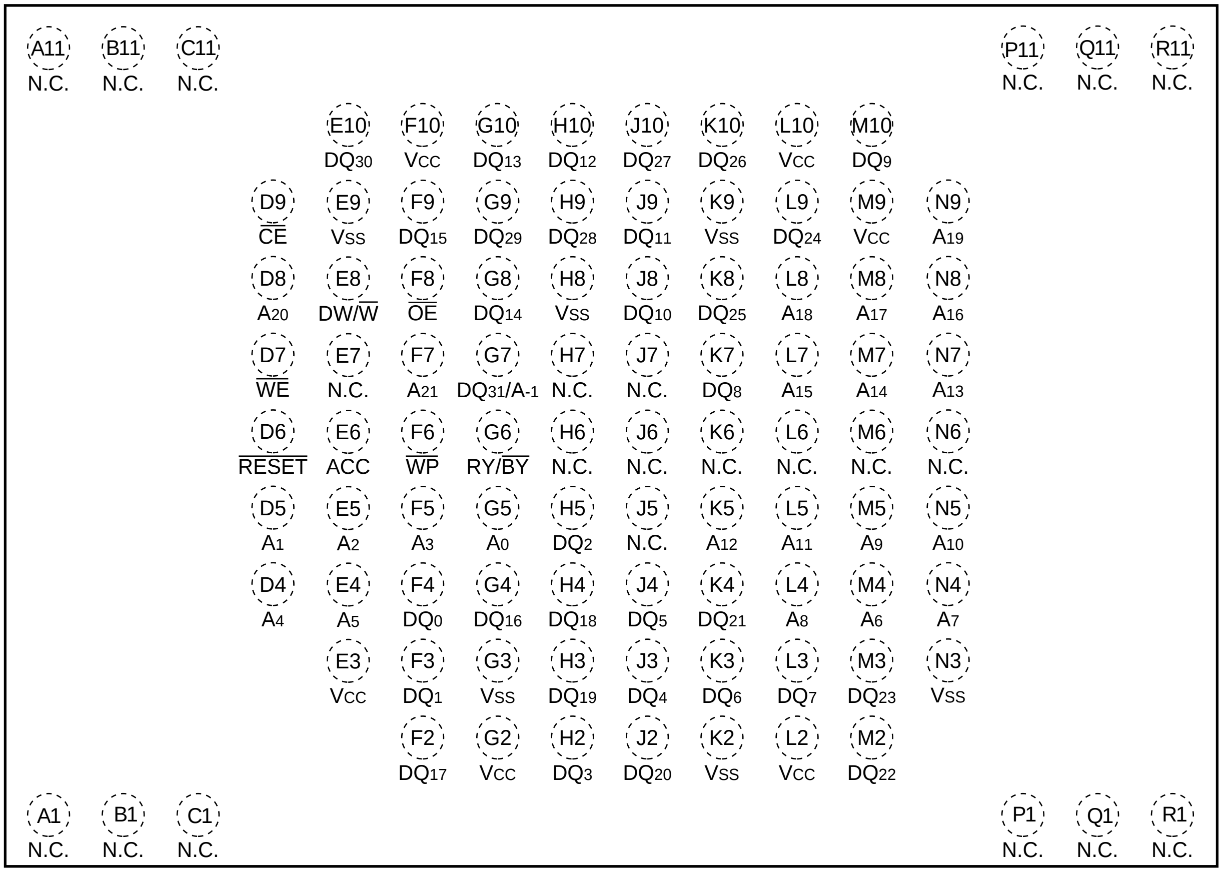
FBGA
(TOP VIEW)
Marking Side



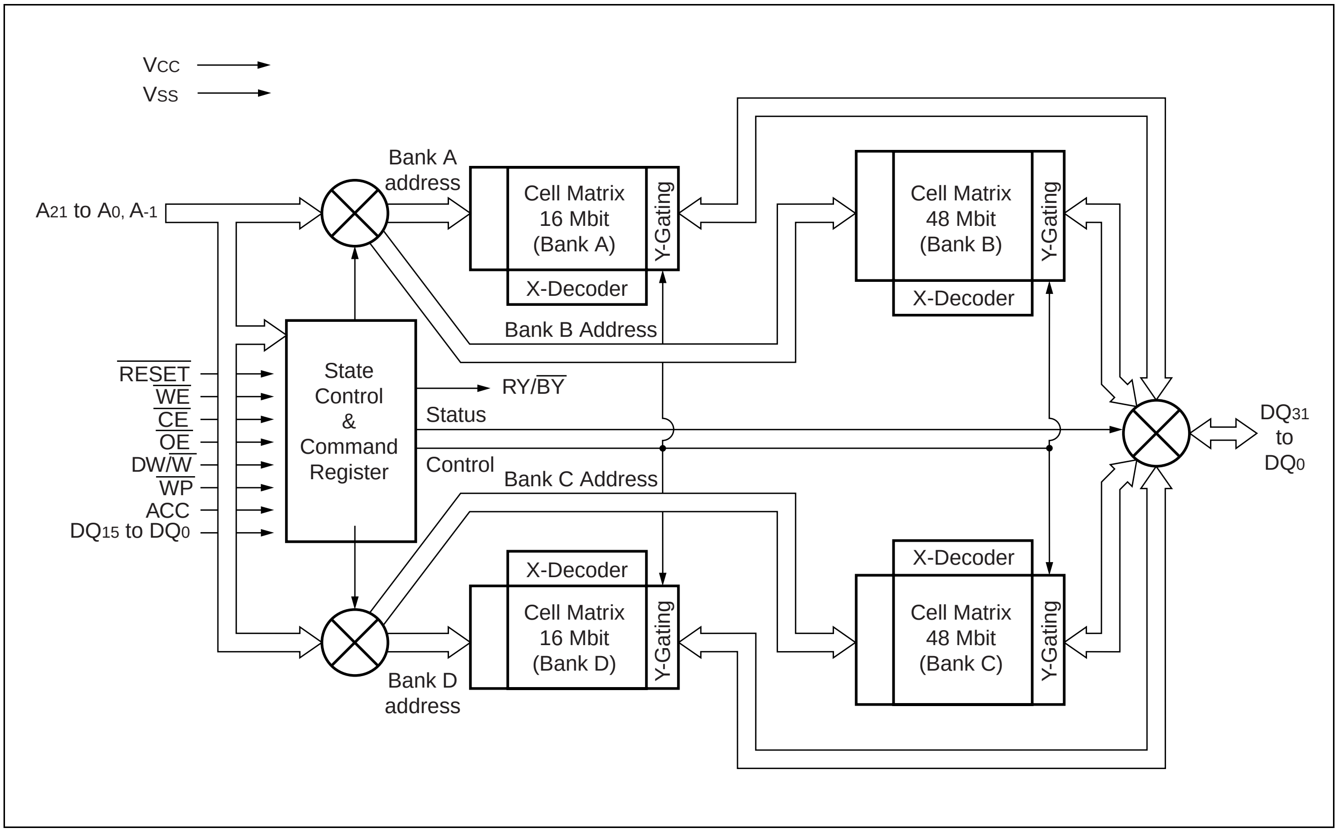
(BGA-96P-M02)

■ PIN DESCRIPTIONS

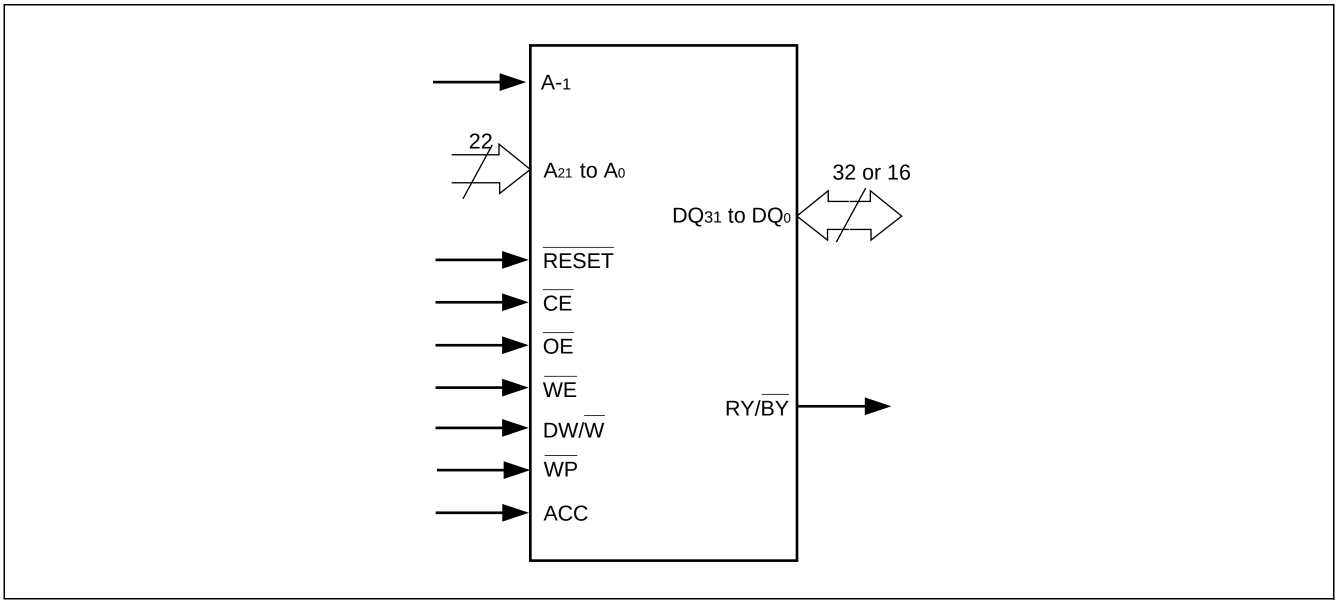
MBM29XL12DF Pin Configuration

Pin	Function
A_{21} to A_0, A_{-1}	Address Inputs
DQ_{31} to DQ_0	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	Hardware Reset / Temporary Sector Group Unprotection
RY/$\overline{BY}$	Ready/Busy Output
DW / $\overline{W}$	Selects 32-bit or 16-bit mode
$\overline{WP}$	Hardware Write Protection
ACC	Program Acceleration
N.C.	Pin Not Connected Internally
V_{SS}	Device Ground
V_{CC}	Device Power Supply

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

MBM29XL12DF User Bus Operations Table (DW/$\overline{W}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{WP}$	DQ_{31} /A_{-1}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_9	DQ_{15} to DQ_0*7	$\overline{RESET}$
Autoselect Manufacturer Code *1	L	L	H	X	L	L	L	L	L	X	X	L	V_{ID}	Code	H
Autoselect Device Code *1	L	L	H	X	L	H	L	L	L	X	X	L	V_{ID}	Code	H
Extended Autoselect Device Code *1	L	L	H	X	L	L	H	H	H	X	X	L	V_{ID}	Code	H
	L	L	H	X	L	H	H	H	H	X	X	L	V_{ID}	Code	H
Read *3	L	L	H	X	A_{-1}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	X	X	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	X	A_{-1}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_9	D_{IN}	H
Enable Sector Group Protection *2,*4	L	V_{ID}	‾__‾	X	L	L	H	L	H	H	H	L	V_{ID}	X	H
Verify Sector Group Protection *2, *4	L	L	H	H	L	L	H	L	H	H	H	L	V_{ID}	Code	H
Boot Block Sector Write Protection *5	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
Temporary Sector Group Unprotection *6	X	X	X	H	X	X	X	X	X	X	X	X	X	X	V_{ID}
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	High-Z	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ‾__‾ = Pulse input. See "■DC CHARACTERISTICS" for voltage levels.

*1 : Manufacturer and device codes may also be accessed via a command register write sequence.
See "MBM29XL12DF Command Definitions Table".

*2 : Refer to section on "Sector Group Protection".

*3 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the program and erase operations.

*4 : V_{CC} = 3.0 V to 3.6 V for 70 ns random access time
V_{CC} = 2.7 V to 3.1 V for 80 ns random access time

*5 : Protects “outermost” 2 × 4K words on both end of the boot block sectors. (SA0, SA1, SA268, and SA269)

*6 : Also used for "Extended Sector Group Protection".

*7 : DQ_{30} to DQ_{16} = X (V_{IL} or V_{IH})

MBM29XL12DF User Bus Operations Table (DW/$\overline{W}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{WP}$	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_9	DQ_{31} to DQ_0	$\overline{RESET}$
Autoselect Manufacturer Code *1	L	L	H	X	L	L	L	L	X	X	L	V_{ID}	Code	H
Autoselect Device Code *1	L	L	H	X	H	L	L	L	X	X	L	V_{ID}	Code	H
Extended Autoselect Device Code *1	L	L	H	X	L	H	H	H	X	X	L	V_{ID}	Code	H
	L	L	H	X	H	H	H	H	X	X	L	V_{ID}	Code	H
Read *3	L	L	H	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	X	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_9	D_{IN}	H
Enable Sector Group Protection *2,*4	L	V_{ID}	⊔	X	L	H	L	H	H	H	L	V_{ID}	X	H
Verify Sector Group Protection *2, *4	L	L	H	H	L	H	L	H	H	H	L	V_{ID}	Code	H
Boot Block Sector Write Protection *5	X	X	X	L	X	X	X	X	X	X	X	X	X	H
Temporary Sector Group Unprotection *6	X	X	X	H	X	X	X	X	X	X	X	X	X	V_{ID}
Reset	X	X	X	X	X	X	X	X	X	X	X	X	High-Z	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ⊔ = Pulse input. See "■DC CHARACTERISTICS" for voltage levels.

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*6 : Also used for "Extended Sector Group Protection".

MBM29XL12DF Command Definitions Table

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle		Seventh Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset *1		2	XXXh	F0h	RA	RD	—	—	—	—	—	—	—	—	—	—
Read/Reset *1	DW	4	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
Autoselect	DW	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
Program	DW	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
Chip Erase	DW	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h	—	—
	W		AAAh		555h		AAAh		AAAh		555h		AAAh			
Sector Erase	DW	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h	—	—
	W		AAAh		555h		AAAh		AAAh		555h					
Program/Erase Suspend		1	BA	B0h	—	—	—	—	—	—	—	—	—	—	—	—
Program/Erase Resume		1	BA	30h	—	—	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	DW	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
Fast Program *2	DW	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—	—	—
	W		XXXh													
Reset from Fast Mode *2	DW	2	BA	90h	XXXh	F0h *6	—	—	—	—	—	—	—	—	—	—
	W		BA		XXXh											
Extended Sector Group Protection*3	DW	4	XXXh	60h	SGA	60h	SGA	40h	SGA	SD	—	—	—	—	—	—
	W															
Query *4	DW	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—	—	—
	W		(BA) 55h													
HiddenROM Entry	DW	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
HiddenROM Program *5	DW	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
HiddenROM Exit *5	DW	4	555h	AAh	2AAh	55h	555h	90h	XXXh	00h	—	—	—	—	—	—
	W		AAAh		555h		AAAh									

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Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle Addr.	First Bus Write Cycle Data	Second Bus Write Cycle Addr.	Second Bus Write Cycle Data	Third Bus Write Cycle Addr.	Third Bus Write Cycle Data	Fourth Bus Read/Write Cycle Addr.	Fourth Bus Read/Write Cycle Data	Fifth Bus Write Cycle Addr.	Fifth Bus Write Cycle Data	Sixth Bus Write Cycle Addr.	Sixth Bus Write Cycle Data	Seventh Bus Write Cycle Addr.	Seventh Bus Write Cycle Data
HiddenROM Protect *5	DW	6	555h	AAh	2AAh	55h	555h	60h	OPBP	68h	OPBP	48h	XXXh	RD (0)	—	—
	W		AAAh		555h		AAAh									
Password Program *7	DW	4	555h	AAh	2AAh	55h	555h	38h	XX0h	PD0	—	—	—	—	—	—
									XX1h	PD1						
	W		AAAh		555h		AAAh		XX0h	PD0						
									XX1h	PD1						
									XX2h	PD2						
									XX3h	PD3						
Password Unlock	DW	5	555h	AAh	2AAh	55h	555h	28h	XX0h	PD0	XX1h	PD1	—	—	—	—
	W	7	AAAh		555h		AAAh						XX2h	PD2	XX3h	PD3
Password Verify	DW	3	555h	AAh	2AAh	55h	555h	C8h	PWA	PWD	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
Password Mode Locking Bit Program	DW	6	555h	AAh	2AAh	55h	555h	60h	PL	68h	PL	48h	XXh	RD (0)	—	—
	W		AAAh		555h		AAAh									
Persistent Sector Protection Mode Locking Bit Program	DW	6	555h	AAh	2AAh	55h	555h	60h	SPML	68h	SPML	48h	XXh	RD (0)	—	—
	W		AAAh		555h		AAAh									
PPB Program	DW	6	555h	AAh	2AAh	55h	555h	60h	(SGA) WP	68h	(SGA) WP	48h	XX	RD (0)	—	—
	W		AAAh		555h		AAAh									
PPB Verify	DW	4	555h	AAh	2AAh	55h	555h	58h	SA	RD (0)	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
All PPB Erase *8	DW	6	555h	AAh	2AAh	55h	555h	60h	EP	60h	EP	40h	XX	RD (0)	—	—
	W		AAAh		555h		AAAh									
PPB Lock Bit Set	DW	3	555h	AAh	2AAh	55h	555h	78h	—	—	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
PPB Lock Bit Verify	DW	4	555h	AAh	2AAh	55h	(BA) 555h	58h	SA	RD (1)	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
DPB Write	DW	4	555h	AAh	2AAh	55h	555h	48h	SA	X1h	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
DPB Erase	DW	4	555h	AAh	2AAh	55h	555h	48h	SA	X0h	—	—	—	—	—	—
	W		AAAh		555h		AAAh									
DPB/PPB Verify	DW	4	555h	AAh	2AAh	55h	(BA) 555h	58h	SA	RD (0)	—	—	—	—	—	—
	W		AAAh		555h		AAAh									

Legend :

RA = Address of the memory location to be read
PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector
BA = Bank Address
RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
SGA = Sector group address to be protected. Set sector group address and (A_6, A_5, A_4, A_3, A_2, A_1, A_0) = (0, 1, 1, 1, 0, 1, 0)
SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
HRA = Address of the HiddenROM area (Double Word Mode: 000000h to 00003Fh)
(Word Mode : 000000h to 00007Fh)
RD(0) = DQ_0 data, RD(1) = DQ_1 data. PPB Lock bit is read on DQ_1 and PPB or DPB are read on DQ_0.
If set, DQ_0/DQ_1=1. If cleared, DQ_0/DQ_1=0.
OPBP = (A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (X, 0, 1, 1, 0, 1, 0)
64 bit Password Data
PD0 to PD1 : Double Word Mode
PD0 to PD3 : Word Mode
PWA/PWD = Password Address/Password Data
PL = Password Locking Address (A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (X, 0, 0, 1, 0, 1, 0)
SPML = Persistent Protection Mode Locking (A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (X, 0, 1, 0, 0, 1, 0)
WP = PPB Program (A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 1, 1, 1, 0, 1, 0)
EP = PPB Erase (A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (1, 1, 1, 1, 0, 1, 0)

*1 : Both of these reset commands are equivalent.

*2 : This command is valid during Fast Mode.

*3 : This command is valid while $\overline{RESET}$ = V_{ID}.

*4 : The valid addresses are A_6 to A_0.

*5 : This command is valid during HiddenROM mode.

*6 : The data “00h” is also acceptable.

*7 : Data before fourth cycle also need to be programmed repearting from first cycle to third cycle.

*8 : RD(0) of the sixth cycle shows PPB erase status. When RD(0) is "1", programming must be repeated from the beginning of first cycle to the fourth cycle; both fifth and the sixth validate full completion of erase.

Notes :
- Address bits A_{21} to A_{11} = X = “H” or “L” for all address commands except for PA, SA, BA, SGA, OPBP, PWA, PL, SPML, WP.
- Bus operations are defined in "MBM29XL12DF User Bus Operations Table (DW/$\overline{W}$ = V_{IL})" and "MBM29XL12DF User Bus Operations Table (DW/$\overline{W}$ = V_{IH})".
- The system should generate the following address patterns:
  DW (Double Word) Mode : 555h or 2AAh to addresses A_{10} to A_0
  W (Word) Mode : AAAh or 555h to addresses A_{10} to A_0, A_{-1}
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
- Command combinations not described in “Command Definitions Table” are illegal.

MBM29XL12DF Autoselect Codes Table

Type		A_{21} to A_{11}	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture's Code		BA*3	V_{IL}	x	x	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	Double Word	BA*3	V_{IL}	x	x	V_{IL}	V_{IL}	V_{IL}	V_{IH}	x	2222227Eh
	Word									V_{IL}	227Eh
Extended Device Code*4	Double Word	BA*3	V_{IL}	x	x	V_{IH}	V_{IH}	V_{IH}	V_{IL}	x	2222220Dh
	Word									V_{IL}	220Dh
	Double Word	BA*3	V_{IL}	x	x	V_{IH}	V_{IH}	V_{IH}	V_{IH}	x	22222200h
	Word									V_{IL}	2200h
PPB Protection		Sector Group Addresses	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h*2

*1 : A_{-1} is for word mode.

*2 : Sector Group can be protected by "Sector Group Protection", "Extended Sector Group Protection" and "New Sector Protection(PPB Protection)". Outputs 01h at protected PPB addresses and outputs 00h at unprotected PPB addresses.

*3 : When V_{ID} is applied to A_9, both Bank 1 and Bank 2 are put into Autoselect mode, which makes simutaneous operation unable to be executed. Consequently, specifying the bank address is not required. However, the bank address needs to be indicated when Autoselect mode is read out at command mode, because then it enables to activate simultaneous operation.

*4 : At double word mode, a read cycle at address (BA) 01h (at word mode,02h) outputs device code.
When 222227Eh (at word mode,227Eh) is output, it indicates that two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh (at word mode,1Ch), as well as at (BA) 0Fh (at word mode, 1Eh).

Exteneded Auteselect Code Table

Type		Code	DQ_{31}	DQ_{30}	DQ_{29}	DQ_{28}	DQ_{27}	DQ_{26}	DQ_{25}	DQ_{24}	DQ_{23}	DQ_{22}	DQ_{21}	DQ_{20}	DQ_{19}	DQ_{18}	DQ_{17}	DQ_{16}
Manufacturer’s Code		04h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Device Code	(DW)	2222 227Eh	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
	(W)	227Eh	A_{-1}	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ
Extended Device Code	(DW)	2222 220Dh	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
	(W)	220Dh	A_{-1}	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ
	(DW)	2222 2200h	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
	(W)	2200h	A_{-1}	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ
PPB Protection		01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PPB Unprotection		00h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Type		Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_{9}	DQ_{8}	DQ_{7}	DQ_{6}	DQ_{5}	DQ_{4}	DQ_{3}	DQ_{2}	DQ_{1}	DQ_{0}
Manufacturer’s Code		04h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	(DW)	2222 227Eh	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	0
	(W)	227Eh	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	0
Extended Device Code	(DW)	2222 220Dh	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	1
	(W)	220Dh	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	1
	(DW)	2222 2200h	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
	(W)	2200h	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
PPB Protection *		01h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PPB Unprotection *		00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HZ : High-Z
(DW) : Double Word mode
(W) : Word mode

* : In word mode, DQ_{30} to DQ_{16} become "High-Z" and DQ_{31} becomes Lowest address "A_{-1}".

Sector Address Tables (Bank A)

Bank	Sector	Sector Address											Sector Size (KW / KDW)	(× 16) Address Range	(× 32) Address Range
		Bank Address													
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}			
Bank A	SA0	0	0	0	0	0	0	0	0	0	0	0	4/2	000000h to 000FFFh	000000h to 0007FFh
	SA1	0	0	0	0	0	0	0	0	0	0	1	4/2	001000h to 001FFFh	000800h to 000FFFh
	SA2	0	0	0	0	0	0	0	0	0	1	0	4/2	002000h to 002FFFh	001000h to 0017FFh
	SA3	0	0	0	0	0	0	0	0	0	1	1	4/2	003000h to 003FFFh	001800h to 001FFFh
	SA4	0	0	0	0	0	0	0	0	1	0	0	4/2	004000h to 004FFFh	002000h to 0027FFh
	SA5	0	0	0	0	0	0	0	0	1	0	1	4/2	005000h to 005FFFh	002800h to 002FFFh
	SA6	0	0	0	0	0	0	0	0	1	1	0	4/2	006000h to 006FFFh	003000h to 0037FFh
	SA7	0	0	0	0	0	0	0	0	1	1	1	4/2	007000h to 007FFFh	003800h to 003FFFh
	SA8	0	0	0	0	0	0	0	1	X	X	X	32/16	008000h to 00FFFFh	004000h to 007FFFh
	SA9	0	0	0	0	0	0	1	0	X	X	X	32/16	010000h to 017FFFh	008000h to 00BFFFh
	SA10	0	0	0	0	0	0	1	1	X	X	X	32/16	018000h to 01FFFFh	00C000h to 00FFFFh
	SA11	0	0	0	0	0	1	0	0	X	X	X	32/16	020000h to 027FFFh	010000h to 013FFFh
	SA12	0	0	0	0	0	1	0	1	X	X	X	32/16	028000h to 02FFFFh	014000h to 017FFFh
	SA13	0	0	0	0	0	1	1	0	X	X	X	32/16	030000h to 037FFFh	018000h to 01BFFFh
	SA14	0	0	0	0	0	1	1	1	X	X	X	32/16	038000h to 03FFFFh	01C000h to 01FFFFh
	SA15	0	0	0	0	1	0	0	0	X	X	X	32/16	040000h to 047FFFh	020000h to 023FFFh
	SA16	0	0	0	0	1	0	0	1	X	X	X	32/16	048000h to 04FFFFh	024000h to 027FFFh
	SA17	0	0	0	0	1	0	1	0	X	X	X	32/16	050000h to 057FFFh	028000h to 02BFFFh
	SA18	0	0	0	0	1	0	1	1	X	X	X	32/16	058000h to 05FFFFh	02C000h to 02FFFFh
	SA19	0	0	0	0	1	1	0	0	X	X	X	32/16	060000h to 067FFFh	030000h to 033FFFh
	SA20	0	0	0	0	1	1	0	1	X	X	X	32/16	068000h to 06FFFFh	034000h to 037FFFh
	SA21	0	0	0	0	1	1	1	0	X	X	X	32/16	070000h to 077FFFh	038000h to 03BFFFh
	SA22	0	0	0	0	1	1	1	1	X	X	X	32/16	078000h to 07FFFFh	03C000h to 03FFFFh
	SA23	0	0	0	1	0	0	0	0	X	X	X	32/16	080000h to 087FFFh	040000h to 043FFFh
	SA24	0	0	0	1	0	0	0	1	X	X	X	32/16	088000h to 08FFFFh	044000h to 047FFFh
	SA25	0	0	0	1	0	0	1	0	X	X	X	32/16	090000h to 097FFFh	048000h to 04BFFFh
	SA26	0	0	0	1	0	0	1	1	X	X	X	32/16	098000h to 09FFFFh	04C000h to 04FFFFh
	SA27	0	0	0	1	0	1	0	0	X	X	X	32/16	0A0000h to 0A7FFFh	050000h to 053FFFh
	SA28	0	0	0	1	0	1	0	1	X	X	X	32/16	0A8000h to 0AFFFFh	054000h to 057FFFh
	SA29	0	0	0	1	0	1	1	0	X	X	X	32/16	0B0000h to 0B7FFFh	058000h to 05BFFFh
	SA30	0	0	0	1	0	1	1	1	X	X	X	32/16	0B8000h to 0BFFFFh	05C000h to 05FFFFh
	SA31	0	0	0	1	1	0	0	0	X	X	X	32/16	0C0000h to 0C7FFFh	060000h to 063FFFh
	SA32	0	0	0	1	1	0	0	1	X	X	X	32/16	0C8000h to 0CFFFFh	064000h to 067FFFh
	SA33	0	0	0	1	1	0	1	0	X	X	X	32/16	0D0000h to 0D7FFFh	068000h to 06BFFFh
	SA34	0	0	0	1	1	0	1	1	X	X	X	32/16	0D8000h to 0DFFFFh	06C000h to 06FFFFh
	SA35	0	0	0	1	1	1	0	0	X	X	X	32/16	0E0000h to 0E7FFFh	070000h to 073FFFh
	SA36	0	0	0	1	1	1	0	1	X	X	X	32/16	0E8000h to 0EFFFFh	074000h to 077FFFh
	SA37	0	0	0	1	1	1	1	0	X	X	X	32/16	0F0000h to 0F7FFFh	078000h to 07BFFFh
	SA38	0	0	0	1	1	1	1	1	X	X	X	32/16	0F8000h to 0FFFFFh	07C000h to 07FFFFh

Sector Address Tables (Bank B)

Bank	Sector	Sector Address											Sector Size (KW / KDW)	(× 16) Address Range	(× 32) Address Range
		Bank Address													
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}			
Bank B	SA39	0	0	1	0	0	0	0	0	X	X	X	32/16	100000h to 107FFFh	080000h to 083FFFh
	SA40	0	0	1	0	0	0	0	1	X	X	X	32/16	108000h to 10FFFFh	084000h to 087FFFh
	SA41	0	0	1	0	0	0	1	0	X	X	X	32/16	110000h to 117FFFh	088000h to 08BFFFh
	SA42	0	0	1	0	0	0	1	1	X	X	X	32/16	118000h to 11FFFFh	08C000h to 08FFFFh
	SA43	0	0	1	0	0	1	0	0	X	X	X	32/16	120000h to 127FFFh	090000h to 093FFFh
	SA44	0	0	1	0	0	1	0	1	X	X	X	32/16	128000h to 12FFFFh	094000h to 097FFFh
	SA45	0	0	1	0	0	1	1	0	X	X	X	32/16	130000h to 137FFFh	098000h to 09BFFFh
	SA46	0	0	1	0	0	1	1	1	X	X	X	32/16	138000h to 13FFFFh	09C000h to 09FFFFh
	SA47	0	0	1	0	1	0	0	0	X	X	X	32/16	140000h to 147FFFh	0A0000h to 0A3FFFh
	SA48	0	0	1	0	1	0	0	1	X	X	X	32/16	148000h to 14FFFFh	0A4000h to 0A7FFFh
	SA49	0	0	1	0	1	0	1	0	X	X	X	32/16	150000h to 157FFFh	0A8000h to 0ABFFFh
	SA50	0	0	1	0	1	0	1	1	X	X	X	32/16	158000h to 15FFFFh	0AC000h to 0AFFFFh
	SA51	0	0	1	0	1	1	0	0	X	X	X	32/16	160000h to 167FFFh	0B0000h to 0B3FFFh
	SA52	0	0	1	0	1	1	0	1	X	X	X	32/16	168000h to 16FFFFh	0B4000h to 0B7FFFh
	SA53	0	0	1	0	1	1	1	0	X	X	X	32/16	170000h to 177FFFh	0B8000h to 0BBFFFh
	SA54	0	0	1	0	1	1	1	1	X	X	X	32/16	178000h to 17FFFFh	0BC000h to 0BFFFFh
	SA55	0	0	1	1	0	0	0	0	X	X	X	32/16	180000h to 187FFFh	0C0000h to 0C3FFFh
	SA56	0	0	1	1	0	0	0	1	X	X	X	32/16	188000h to 18FFFFh	0C4000h to 0C7FFFh
	SA57	0	0	1	1	0	0	1	0	X	X	X	32/16	190000h to 197FFFh	0C8000h to 0CBFFFh
	SA58	0	0	1	1	0	0	1	1	X	X	X	32/16	198000h to 19FFFFh	0CC000h to 0CFFFFh
	SA59	0	0	1	1	0	1	0	0	X	X	X	32/16	1A0000h to 1A7FFFh	0D0000h to 0D3FFFh
	SA60	0	0	1	1	0	1	0	1	X	X	X	32/16	1A8000h to 1AFFFFh	0D4000h to 0D7FFFh
	SA61	0	0	1	1	0	1	1	0	X	X	X	32/16	1B0000h to 1B7FFFh	0D8000h to 0DBFFFh
	SA62	0	0	1	1	0	1	1	1	X	X	X	32/16	1B8000h to 1BFFFFh	0DC000h to 0DFFFFh
	SA63	0	0	1	1	1	0	0	0	X	X	X	32/16	1C0000h to 1C7FFFh	0E0000h to 0E3FFFh
	SA64	0	0	1	1	1	0	0	1	X	X	X	32/16	1C8000h to 1CFFFFh	0E4000h to 0E7FFFh
	SA65	0	0	1	1	1	0	1	0	X	X	X	32/16	1D0000h to 1D7FFFh	0E8000h to 0EBFFFh
	SA66	0	0	1	1	1	0	1	1	X	X	X	32/16	1D8000h to 1DFFFFh	0EC000h to 0EFFFFh
	SA67	0	0	1	1	1	1	0	0	X	X	X	32/16	1E0000h to 1E7FFFh	0F0000h to 0F3FFFh
	SA68	0	0	1	1	1	1	0	1	X	X	X	32/16	1E8000h to 1EFFFFh	0F4000h to 0F7FFFh
	SA69	0	0	1	1	1	1	1	0	X	X	X	32/16	1F0000h to 1F7FFFh	0F8000h to 0FBFFFh
	SA70	0	0	1	1	1	1	1	1	X	X	X	32/16	1F8000h to 1FFFFFh	0FC000h to 0FFFFFh
	SA71	0	1	0	0	0	0	0	0	X	X	X	32/16	200000h to 207FFFh	100000h to 103FFFh
	SA72	0	1	0	0	0	0	0	1	X	X	X	32/16	208000h to 20FFFFh	104000h to 107FFFh
	SA73	0	1	0	0	0	0	1	0	X	X	X	32/16	210000h to 217FFFh	108000h to 10BFFFh
	SA74	0	1	0	0	0	0	1	1	X	X	X	32/16	218000h to 21FFFFh	10C000h to 10FFFFh
	SA75	0	1	0	0	0	1	0	0	X	X	X	32/16	220000h to 227FFFh	110000h to 113FFFh
	SA76	0	1	0	0	0	1	0	1	X	X	X	32/16	228000h to 22FFFFh	114000h to 117FFFh
	SA77	0	1	0	0	0	1	1	0	X	X	X	32/16	230000h to 237FFFh	118000h to 11BFFFh

(Continued)

Bank	Sector	Sector Address											Sector Size (KW / KDW)	(× 16) Address Range	(× 32) Address Range
		Bank Address													
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11			
Bank B	SA78	0	1	0	0	0	1	1	1	X	X	X	32/16	238000h to 23FFFFh	11C000h to 11FFFFh
	SA79	0	1	0	0	1	0	0	0	X	X	X	32/16	240000h to 247FFFh	120000h to 123FFFh
	SA80	0	1	0	0	1	0	0	1	X	X	X	32/16	248000h to 24FFFFh	124000h to 127FFFh
	SA81	0	1	0	0	1	0	1	0	X	X	X	32/16	250000h to 257FFFh	128000h to 12BFFFh
	SA82	0	1	0	0	1	0	1	1	X	X	X	32/16	258000h to 25FFFFh	12C000h to 12FFFFh
	SA83	0	1	0	0	1	1	0	0	X	X	X	32/16	260000h to 267FFFh	130000h to 133FFFh
	SA84	0	1	0	0	1	1	0	1	X	X	X	32/16	268000h to 26FFFFh	134000h to 137FFFh
	SA85	0	1	0	0	1	1	1	0	X	X	X	32/16	270000h to 277FFFh	138000h to 13BFFFh
	SA86	0	1	0	0	1	1	1	1	X	X	X	32/16	278000h to 27FFFFh	13C000h to 13FFFFh
	SA87	0	1	0	1	0	0	0	0	X	X	X	32/16	280000h to 287FFFh	140000h to 143FFFh
	SA88	0	1	0	1	0	0	0	1	X	X	X	32/16	288000h to 28FFFFh	144000h to 147FFFh
	SA89	0	1	0	1	0	0	1	0	X	X	X	32/16	290000h to 297FFFh	148000h to 14BFFFh
	SA90	0	1	0	1	0	0	1	1	X	X	X	32/16	298000h to 29FFFFh	14C000h to 14FFFFh
	SA91	0	1	0	1	0	1	0	0	X	X	X	32/16	2A0000h to 2A7FFFh	150000h to 153FFFh
	SA92	0	1	0	1	0	1	0	1	X	X	X	32/16	2A8000h to 2AFFFFh	154000h to 157FFFh
	SA93	0	1	0	1	0	1	1	0	X	X	X	32/16	2B0000h to 2B7FFFh	158000h to 15BFFFh
	SA94	0	1	0	1	0	1	1	1	X	X	X	32/16	2B8000h to 2BFFFFh	15C000h to 15FFFFh
	SA95	0	1	0	1	1	0	0	0	X	X	X	32/16	2C0000h to 2C7FFFh	160000h to 163FFFh
	SA96	0	1	0	1	1	0	0	1	X	X	X	32/16	2C8000h to 2CFFFFh	164000h to 167FFFh
	SA97	0	1	0	1	1	0	1	0	X	X	X	32/16	2D0000h to 2D7FFFh	168000h to 16BFFFh
	SA98	0	1	0	1	1	0	1	1	X	X	X	32/16	2D8000h to 2DFFFFh	16C000h to 16FFFFh
	SA99	0	1	0	1	1	1	0	0	X	X	X	32/16	2E0000h to 2E7FFFh	170000h to 173FFFh
	SA100	0	1	0	1	1	1	0	1	X	X	X	32/16	2E8000h to 2EFFFFh	174000h to 177FFFh
	SA101	0	1	0	1	1	1	1	0	X	X	X	32/16	2F0000h to 2F7FFFh	178000h to 17BFFFh
	SA102	0	1	0	1	1	1	1	1	X	X	X	32/16	2F8000h to 2FFFFFh	17C000h to 17FFFFh
	SA103	0	1	1	0	0	0	0	0	X	X	X	32/16	300000h to 307FFFh	180000h to 183FFFh
	SA104	0	1	1	0	0	0	0	1	X	X	X	32/16	308000h to 30FFFFh	184000h to 187FFFh
	SA105	0	1	1	0	0	0	1	0	X	X	X	32/16	310000h to 317FFFh	188000h to 18BFFFh
	SA106	0	1	1	0	0	0	1	1	X	X	X	32/16	318000h to 31FFFFh	18C000h to 18FFFFh
	SA107	0	1	1	0	0	1	0	0	X	X	X	32/16	320000h to 327FFFh	190000h to 193FFFh
	SA108	0	1	1	0	0	1	0	1	X	X	X	32/16	328000h to 32FFFFh	194000h to 197FFFh
	SA109	0	1	1	0	0	1	1	0	X	X	X	32/16	330000h to 337FFFh	198000h to 19BFFFh
	SA110	0	1	1	0	0	1	1	1	X	X	X	32/16	338000h to 33FFFFh	19C000h to 19FFFFh
	SA111	0	1	1	0	1	0	0	0	X	X	X	32/16	340000h to 347FFFh	1A0000h to 1A3FFFh
	SA112	0	1	1	0	1	0	0	1	X	X	X	32/16	348000h to 34FFFFh	1A4000h to 1A7FFFh
	SA113	0	1	1	0	1	0	1	0	X	X	X	32/16	350000h to 357FFFh	1A8000h to 1ABFFFh
	SA114	0	1	1	0	1	0	1	1	X	X	X	32/16	358000h to 35FFFFh	1AC000h to 1AFFFFh
	SA115	0	1	1	0	1	1	0	0	X	X	X	32/16	360000h to 367FFFh	1B0000h to 1B3FFFh
	SA116	0	1	1	0	1	1	0	1	X	X	X	32/16	368000h to 36FFFFh	1B4000h to 1B7FFFh

(Continued)

(Continued)

Bank	Sector	Sector Address											Sector Size (KW / KDW)	(× 16) Address Range	(× 32) Address Range
		Bank Address													
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}			
Bank B	SA117	0	1	1	0	1	1	1	0	X	X	X	32/16	370000h to 377FFFh	1B8000h to 1BBFFFh
	SA118	0	1	1	0	1	1	1	1	X	X	X	32/16	378000h to 37FFFFh	1BC000h to 1BFFFFh
	SA119	0	1	1	1	0	0	0	0	X	X	X	32/16	380000h to 387FFFh	1C0000h to 1C3FFFh
	SA120	0	1	1	1	0	0	0	1	X	X	X	32/16	388000h to 38FFFFh	1C4000h to 1C7FFFh
	SA121	0	1	1	1	0	0	1	0	X	X	X	32/16	390000h to 397FFFh	1C8000h to 1CBFFFh
	SA122	0	1	1	1	0	0	1	1	X	X	X	32/16	398000h to 39FFFFh	1CC000h to 1CFFFFh
	SA123	0	1	1	1	0	1	0	0	X	X	X	32/16	3A0000h to 3A7FFFh	1D0000h to 1D3FFFh
	SA124	0	1	1	1	0	1	0	1	X	X	X	32/16	3A8000h to 3AFFFFh	1D4000h to 1D7FFFh
	SA125	0	1	1	1	0	1	1	0	X	X	X	32/16	3B0000h to 3B7FFFh	1D8000h to 1DBFFFh
	SA126	0	1	1	1	0	1	1	1	X	X	X	32/16	3B8000h to 3BFFFFh	1DC000h to 1DFFFFh
	SA127	0	1	1	1	1	0	0	0	X	X	X	32/16	3C0000h to 3C7FFFh	1E0000h to 1E3FFFh
	SA128	0	1	1	1	1	0	0	1	X	X	X	32/16	3C8000h to 3CFFFFh	1E4000h to 1E7FFFh
	SA129	0	1	1	1	1	0	1	0	X	X	X	32/16	3D0000h to 3D7FFFh	1E8000h to 1EBFFFh
	SA130	0	1	1	1	1	0	1	1	X	X	X	32/16	3D8000h to 3DFFFFh	1EC000h to 1EFFFFh
	SA131	0	1	1	1	1	1	0	0	X	X	X	32/16	3E0000h to 3E7FFFh	1F0000h to 1F3FFFh
	SA132	0	1	1	1	1	1	0	1	X	X	X	32/16	3E8000h to 3EFFFFh	1F4000h to 1F7FFFh
	SA133	0	1	1	1	1	1	1	0	X	X	X	32/16	3F0000h to 3F7FFFh	1F8000h to 1FBFFFh
	SA134	0	1	1	1	1	1	1	1	X	X	X	32/16	3F8000h to 3FFFFFh	1FC000h to 1FFFFFh

Sector Address Tables (Bank C)

Bank	Sector	Sector Address											Sector Size (KW / KDW)	(× 16) Address Range	(× 32) Address Range
		Bank Address													
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}			
	SA135	1	0	0	0	0	0	0	0	X	X	X	32/16	400000h to 407FFFh	200000h to 203FFFh
	SA136	1	0	0	0	0	0	0	1	X	X	X	32/16	408000h to 40FFFFh	204000h to 207FFFh
	SA137	1	0	0	0	0	0	1	0	X	X	X	32/16	410000h to 417FFFh	208000h to 20BFFFh
	SA138	1	0	0	0	0	0	1	1	X	X	X	32/16	418000h to 41FFFFh	20C000h to 20FFFFh
	SA139	1	0	0	0	0	1	0	0	X	X	X	32/16	420000h to 427FFFh	210000h to 213FFFh
	SA140	1	0	0	0	0	1	0	1	X	X	X	32/16	428000h to 42FFFFh	214000h to 217FFFh
	SA141	1	0	0	0	0	1	1	0	X	X	X	32/16	430000h to 437FFFh	218000h to 21BFFFh
	SA142	1	0	0	0	0	1	1	1	X	X	X	32/16	438000h to 43FFFFh	21C000h to 21FFFFh
	SA143	1	0	0	0	1	0	0	0	X	X	X	32/16	440000h to 447FFFh	220000h to 223FFFh
	SA144	1	0	0	0	1	0	0	1	X	X	X	32/16	448000h to 44FFFFh	224000h to 227FFFh
	SA145	1	0	0	0	1	0	1	0	X	X	X	32/16	450000h to 457FFFh	228000h to 22BFFFh
	SA146	1	0	0	0	1	0	1	1	X	X	X	32/16	458000h to 45FFFFh	22C000h to 22FFFFh
	SA147	1	0	0	0	1	1	0	0	X	X	X	32/16	460000h to 467FFFh	230000h to 233FFFh
	SA148	1	0	0	0	1	1	0	1	X	X	X	32/16	468000h to 46FFFFh	234000h to 237FFFh
	SA149	1	0	0	0	1	1	1	0	X	X	X	32/16	470000h to 477FFFh	238000h to 23BFFFh
	SA150	1	0	0	0	1	1	1	1	X	X	X	32/16	478000h to 47FFFFh	23C000h to 23FFFFh
	SA151	1	0	0	1	0	0	0	0	X	X	X	32/16	480000h to 487FFFh	240000h to 243FFFh
	SA152	1	0	0	1	0	0	0	1	X	X	X	32/16	488000h to 48FFFFh	244000h to 247FFFh
	SA153	1	0	0	1	0	0	1	0	X	X	X	32/16	490000h to 497FFFh	248000h to 24BFFFh
Bank C	SA154	1	0	0	1	0	0	1	1	X	X	X	32/16	498000h to 49FFFFh	24C000h to 24FFFFh
	SA155	1	0	0	1	0	1	0	0	X	X	X	32/16	4A0000h to 4A7FFFh	250000h to 253FFFh
	SA156	1	0	0	1	0	1	0	1	X	X	X	32/16	4A8000h to 4AFFFFh	254000h to 257FFFh
	SA157	1	0	0	1	0	1	1	0	X	X	X	32/16	4B0000h to 4B7FFFh	258000h to 25BFFFh
	SA158	1	0	0	1	0	1	1	1	X	X	X	32/16	4B8000h to 4BFFFFh	25C000h to 25FFFFh
	SA159	1	0	0	1	1	0	0	0	X	X	X	32/16	4C0000h to 4C7FFFh	260000h to 263FFFh
	SA160	1	0	0	1	1	0	0	1	X	X	X	32/16	4C8000h to 4CFFFFh	264000h to 267FFFh
	SA161	1	0	0	1	1	0	1	0	X	X	X	32/16	4D0000h to 4D7FFFh	268000h to 26BFFFh
	SA162	1	0	0	1	1	0	1	1	X	X	X	32/16	4D8000h to 4DFFFFh	26C000h to 26FFFFh
	SA163	1	0	0	1	1	1	0	0	X	X	X	32/16	4E0000h to 4E7FFFh	270000h to 273FFFh
	SA164	1	0	0	1	1	1	0	1	X	X	X	32/16	4E8000h to 4EFFFFh	274000h to 277FFFh
	SA165	1	0	0	1	1	1	1	0	X	X	X	32/16	4F0000h to 4F7FFFh	278000h to 27BFFFh
	SA166	1	0	0	1	1	1	1	1	X	X	X	32/16	4F8000h to 4FFFFFh	27C000h to 27FFFFh
	SA167	1	0	1	0	0	0	0	0	X	X	X	32/16	500000h to 507FFFh	280000h to 283FFFh
	SA168	1	0	1	0	0	0	0	1	X	X	X	32/16	508000h to 50FFFFh	284000h to 287FFFh
	SA169	1	0	1	0	0	0	1	0	X	X	X	32/16	510000h to 517FFFh	288000h to 28BFFFh
	SA170	1	0	1	0	0	0	1	1	X	X	X	32/16	518000h to 51FFFFh	28C000h to 28FFFFh
	SA171	1	0	1	0	0	1	0	0	X	X	X	32/16	520000h to 527FFFh	290000h to 293FFFh
	SA172	1	0	1	0	0	1	0	1	X	X	X	32/16	528000h to 52FFFFh	294000h to 297FFFh
	SA173	1	0	1	0	0	1	1	0	X	X	X	32/16	530000h to 537FFFh	298000h to 29BFFFh

(Continued)

Bank	Sector	Sector Address											Sector Size (KW / KDW)	(× 16) Address Range	(× 32) Address Range
		Bank Address													
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}			
Bank C	SA174	1	0	1	0	0	1	1	1	X	X	X	32/16	538000h to 53FFFFh	29C000h to 29FFFFh
	SA175	1	0	1	0	1	0	0	0	X	X	X	32/16	540000h to 547FFFh	2A0000h to 2A3FFFh
	SA176	1	0	1	0	1	0	0	1	X	X	X	32/16	548000h to 54FFFFh	2A4000h to 2A7FFFh
	SA177	1	0	1	0	1	0	1	0	X	X	X	32/16	550000h to 557FFFh	2A8000h to 2ABFFFh
	SA178	1	0	1	0	1	0	1	1	X	X	X	32/16	558000h to 55FFFFh	2AC000h to 2AFFFFh
	SA179	1	0	1	0	1	1	0	0	X	X	X	32/16	560000h to 567FFFh	2B0000h to 2B3FFFh
	SA180	1	0	1	0	1	1	0	1	X	X	X	32/16	568000h to 56FFFFh	2B4000h to 2B7FFFh
	SA181	1	0	1	0	1	1	1	0	X	X	X	32/16	570000h to 577FFFh	2B8000h to 2BBFFFh
	SA182	1	0	1	0	1	1	1	1	X	X	X	32/16	578000h to 57FFFFh	2BC000h to 2BFFFFh
	SA183	1	0	1	1	0	0	0	0	X	X	X	32/16	580000h to 587FFFh	2C0000h to 2C3FFFh
	SA184	1	0	1	1	0	0	0	1	X	X	X	32/16	588000h to 58FFFFh	2C4000h to 2C7FFFh
	SA185	1	0	1	1	0	0	1	0	X	X	X	32/16	590000h to 597FFFh	2C8000h to 2CBFFFh
	SA186	1	0	1	1	0	0	1	1	X	X	X	32/16	598000h to 59FFFFh	2CC000h to 2CFFFFh
	SA187	1	0	1	1	0	1	0	0	X	X	X	32/16	5A0000h to 5A7FFFh	2D0000h to 2D3FFFh
	SA188	1	0	1	1	0	1	0	1	X	X	X	32/16	5A8000h to 5AFFFFh	2D4000h to 2D7FFFh
	SA189	1	0	1	1	0	1	1	0	X	X	X	32/16	5B0000h to 5B7FFFh	2D8000h to 2DBFFFh
	SA190	1	0	1	1	0	1	1	1	X	X	X	32/16	5B8000h to 5BFFFFh	2DC000h to 2DFFFFh
	SA191	1	0	1	1	1	0	0	0	X	X	X	32/16	5C0000h to 5C7FFFh	2E0000h to 2E3FFFh
	SA192	1	0	1	1	1	0	0	1	X	X	X	32/16	5C8000h to 5CFFFFh	2E4000h to 2E7FFFh
	SA193	1	0	1	1	1	0	1	0	X	X	X	32/16	6D0000h to 5D7FFFh	2E8000h to 2EBFFFh
	SA194	1	0	1	1	1	0	1	1	X	X	X	32/16	6D8000h to 5DFFFFh	2EC000h to 2EFFFFh
	SA195	1	0	1	1	1	1	0	0	X	X	X	32/16	5E0000h to 5E7FFFh	2F0000h to 2F3FFFh
	SA196	1	0	1	1	1	1	0	1	X	X	X	32/16	5E8000h to 5EFFFFh	2F4000h to 2F7FFFh
	SA197	1	0	1	1	1	1	1	0	X	X	X	32/16	5F0000h to 5F7FFFh	2F8000h to 2FBFFFh
	SA198	1	0	1	1	1	1	1	1	X	X	X	32/16	5F8000h to 5FFFFFh	2FC000h to 2FFFFFh
	SA199	1	1	0	0	0	0	0	0	X	X	X	32/16	600000h to 607FFFh	300000h to 303FFFh
	SA200	1	1	0	0	0	0	0	1	X	X	X	32/16	608000h to 60FFFFh	304000h to 307FFFh
	SA201	1	1	0	0	0	0	1	0	X	X	X	32/16	610000h to 617FFFh	308000h to 30BFFFh
	SA202	1	1	0	0	0	0	1	1	X	X	X	32/16	618000h to 61FFFFh	30C000h to 30FFFFh
	SA203	1	1	0	0	0	1	0	0	X	X	X	32/16	620000h to 627FFFh	310000h to 313FFFh
	SA204	1	1	0	0	0	1	0	1	X	X	X	32/16	628000h to 62FFFFh	314000h to 317FFFh
	SA205	1	1	0	0	0	1	1	0	X	X	X	32/16	630000h to 637FFFh	318000h to 31BFFFh
	SA206	1	1	0	0	0	1	1	1	X	X	X	32/16	638000h to 63FFFFh	31C000h to 31FFFFh
	SA207	1	1	0	0	1	0	0	0	X	X	X	32/16	640000h to 647FFFh	320000h to 323FFFh
	SA208	1	1	0	0	1	0	0	1	X	X	X	32/16	648000h to 64FFFFh	324000h to 327FFFh
	SA209	1	1	0	0	1	0	1	0	X	X	X	32/16	650000h to 657FFFh	328000h to 32BFFFh
	SA210	1	1	0	0	1	0	1	1	X	X	X	32/16	658000h to 65FFFFh	32C000h to 32FFFFh
	SA211	1	1	0	0	1	1	0	0	X	X	X	32/16	660000h to 667FFFh	330000h to 333FFFh
	SA212	1	1	0	0	1	1	0	1	X	X	X	32/16	668000h to 66FFFFh	334000h to 337FFFh

(Continued)

(Continued)

Bank	Sector	Sector Address											Sector Size (KW / KDW)	(× 16) Address Range	(× 32) Address Range
		Bank Address													
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}			
Bank C	SA213	1	1	0	0	1	1	1	0	X	X	X	32/16	670000h to 677FFFh	338000h to 33BFFFh
	SA214	1	1	0	0	1	1	1	1	X	X	X	32/16	678000h to 67FFFFh	33C000h to 33FFFFh
	SA215	1	1	0	1	0	0	0	0	X	X	X	32/16	680000h to 687FFFh	340000h to 343FFFh
	SA216	1	1	0	1	0	0	0	1	X	X	X	32/16	688000h to 68FFFFh	344000h to 347FFFh
	SA217	1	1	0	1	0	0	1	0	X	X	X	32/16	690000h to 697FFFh	348000h to 34BFFFh
	SA218	1	1	0	1	0	0	1	1	X	X	X	32/16	698000h to 69FFFFh	34C000h to 34FFFFh
	SA219	1	1	0	1	0	1	0	0	X	X	X	32/16	6A0000h to 6A7FFFh	350000h to 353FFFh
	SA220	1	1	0	1	0	1	0	1	X	X	X	32/16	6A8000h to 6AFFFFh	354000h to 357FFFh
	SA221	1	1	0	1	0	1	1	0	X	X	X	32/16	6B0000h to 6B7FFFh	358000h to 35BFFFh
	SA222	1	1	0	1	0	1	1	1	X	X	X	32/16	8B8000h to 6BFFFFh	35C000h to 35FFFFh
	SA223	1	1	0	1	1	0	0	0	X	X	X	32/16	6C0000h to 6C7FFFh	360000h to 363FFFh
	SA224	1	1	0	1	1	0	0	1	X	X	X	32/16	6C8000h to 6CFFFFh	364000h to 367FFFh
	SA225	1	1	0	1	1	0	1	0	X	X	X	32/16	6D0000h to 6D7FFFh	368000h to 36BFFFh
	SA226	1	1	0	1	1	0	1	1	X	X	X	32/16	6D8000h to 6DFFFFh	36C000h to 36FFFFh
	SA227	1	1	0	1	1	1	0	0	X	X	X	32/16	6E0000h to 6E7FFFh	370000h to 373FFFh
	SA228	1	1	0	1	1	1	0	1	X	X	X	32/16	6E8000h to 6EFFFFh	374000h to 377FFFh
	SA229	1	1	0	1	1	1	1	0	X	X	X	32/16	6F0000h to 6F7FFFh	378000h to 37BFFFh
	SA230	1	1	0	1	1	1	1	1	X	X	X	32/16	6F8000h to 6FFFFFh	37C000h to 37FFFFh

Sector Address Tables (Bank D)

Bank	Sector	Sector Address											Sector Size (KW / KDW)	(× 16) Address Range	(× 32) Address Range
		Bank Address													
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}			
Bank D	SA231	1	1	1	0	0	0	0	0	X	X	X	32/16	700000h to 707FFFh	380000h to 383FFFh
	SA232	1	1	1	0	0	0	0	1	X	X	X	32/16	708000h to 70FFFFh	384000h to 387FFFh
	SA233	1	1	1	0	0	0	1	0	X	X	X	32/16	710000h to 717FFFh	388000h to 38BFFFh
	SA234	1	1	1	0	0	0	1	1	X	X	X	32/16	718000h to 71FFFFh	38C000h to 38FFFFh
	SA235	1	1	1	0	0	1	0	0	X	X	X	32/16	720000h to 727FFFh	390000h to 393FFFh
	SA236	1	1	1	0	0	1	0	1	X	X	X	32/16	728000h to 72FFFFh	394000h to 397FFFh
	SA237	1	1	1	0	0	1	1	0	X	X	X	32/16	730000h to 737FFFh	398000h to 39BFFFh
	SA238	1	1	1	0	0	1	1	1	X	X	X	32/16	738000h to 73FFFFh	39C000h to 39FFFFh
	SA239	1	1	1	0	1	0	0	0	X	X	X	32/16	740000h to 747FFFh	3A0000h to 3A3FFFh
	SA240	1	1	1	0	1	0	0	1	X	X	X	32/16	748000h to 74FFFFh	3A4000h to 3A7FFFh
	SA241	1	1	1	0	1	0	1	0	X	X	X	32/16	750000h to 757FFFh	3A8000h to 3ABFFFh
	SA242	1	1	1	0	1	0	1	1	X	X	X	32/16	758000h to 75FFFFh	3AC000h to 3AFFFFh
	SA243	1	1	1	0	1	1	0	0	X	X	X	32/16	760000h to 767FFFh	3B0000h to 3B3FFFh
	SA244	1	1	1	0	1	1	0	1	X	X	X	32/16	768000h to 76FFFFh	3B4000h to 3B7FFFh
	SA245	1	1	1	0	1	1	1	0	X	X	X	32/16	770000h to 777FFFh	3B8000h to 3BBFFFh
	SA246	1	1	1	0	1	1	1	1	X	X	X	32/16	778000h to 77FFFFh	3BC000h to 3BFFFFh
	SA247	1	1	1	1	0	0	0	0	X	X	X	32/16	780000h to 787FFFh	3C0000h to 3C3FFFh
	SA248	1	1	1	1	0	0	0	1	X	X	X	32/16	788000h to 78FFFFh	3C4000h to 3C7FFFh
	SA249	1	1	1	1	0	0	1	0	X	X	X	32/16	790000h to 797FFFh	3C8000h to 3CBFFFh
	SA250	1	1	1	1	0	0	1	1	X	X	X	32/16	798000h to 79FFFFh	3CC000h to 3CFFFFh
	SA251	1	1	1	1	0	1	0	0	X	X	X	32/16	7A0000h to 7A7FFFh	3D0000h to 3D3FFFh
	SA252	1	1	1	1	0	1	0	1	X	X	X	32/16	7A8000h to 7AFFFFh	3D4000h to 3D7FFFh
	SA253	1	1	1	1	0	1	1	0	X	X	X	32/16	7B0000h to 7B7FFFh	3D8000h to 3DBFFFh
	SA254	1	1	1	1	0	1	1	1	X	X	X	32/16	7B8000h to 7BFFFFh	3DC000h to 3DFFFFh
	SA255	1	1	1	1	1	0	0	0	X	X	X	32/16	7C0000h to 7C7FFFh	3E0000h to 3E3FFFh
	SA256	1	1	1	1	1	0	0	1	X	X	X	32/16	7C8000h to 7CFFFFh	3E4000h to 3E7FFFh
	SA257	1	1	1	1	1	0	1	0	X	X	X	32/16	7D0000h to 7D7FFFh	3E8000h to 3EBFFFh
	SA258	1	1	1	1	1	0	1	1	X	X	X	32/16	7D8000h to 7DFFFFh	3EC000h to 3EFFFFh
	SA259	1	1	1	1	1	1	0	0	X	X	X	32/16	7E0000h to 7E7FFFh	3F0000h to 3F3FFFh
	SA260	1	1	1	1	1	1	0	1	X	X	X	32/16	7E8000h to 7EFFFFh	3F4000h to 3F7FFFh
	SA261	1	1	1	1	1	1	1	0	X	X	X	32/16	7F0000h to 7F7FFFh	3F8000h to 3FBFFFh
	SA262	1	1	1	1	1	1	1	1	0	0	0	4/2	7F8000h to 7F8FFFh	3FC000h to 3FC7FFh
	SA263	1	1	1	1	1	1	1	1	0	0	1	4/2	7F9000h to 7F9FFFh	3FC800h to 3FCFFFh
	SA264	1	1	1	1	1	1	1	1	0	1	0	4/2	7FA000h to 7FAFFFh	3FD000h to 3FD7FFh
	SA265	1	1	1	1	1	1	1	1	0	1	1	4/2	7FB000h to 7FBFFFh	3FD800h to 3FDFFFh
	SA266	1	1	1	1	1	1	1	1	1	0	0	4/2	7FC000h to 7FCFFFh	3FE000h to 3FE7FFh
	SA267	1	1	1	1	1	1	1	1	1	0	1	4/2	7FD000h to 7FDFFFh	3FE800h to 3FEFFFh
	SA268	1	1	1	1	1	1	1	1	1	1	0	4/2	7FE000h to 7FEFFFh	3FF000h to 3FF7FFh
	SA269	1	1	1	1	1	1	1	1	1	1	1	4/2	7FF000h to 7FFFFFh	3FF800h to 3FFFFFh

Sector Group Address Table

Sector Group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0	0 1 1	1 0 1	X	X	X	SA8 to SA10
SGA9	0	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	0	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	0	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	0	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	0	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	0	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	0	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	0	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	0	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA24	0	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA25	0	1	0	0	0	1	X	X	X	X	X	SA75 to SA78
SGA26	0	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA27	0	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA28	0	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA29	0	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	0	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	0	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA32	0	1	1	0	0	0	X	X	X	X	X	SA103 to SA106

(Continued)

Sector Group	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	Sectors
SGA33	0	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	0	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	0	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA36	0	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA37	0	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA38	0	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA39	0	1	1	1	1	1	X	X	X	X	X	SA131 to SA134
SGA40	1	0	0	0	0	0	X	X	X	X	X	SA135 to SA138
SGA41	1	0	0	0	0	1	X	X	X	X	X	SA139 to SA142
SGA42	1	0	0	0	1	0	X	X	X	X	X	SA143 to SA146
SGA43	1	0	0	0	1	1	X	X	X	X	X	SA147 to SA150
SGA44	1	0	0	1	0	0	X	X	X	X	X	SA151 to SA154
SGA45	1	0	0	1	0	1	X	X	X	X	X	SA155 to SA158
SGA46	1	0	0	1	1	0	X	X	X	X	X	SA159 to SA162
SGA47	1	0	0	1	1	1	X	X	X	X	X	SA163 to SA166
SGA48	1	0	1	0	0	0	X	X	X	X	X	SA167 to SA170
SGA49	1	0	1	0	0	1	X	X	X	X	X	SA171 to SA174
SGA50	1	0	1	0	1	0	X	X	X	X	X	SA175 to SA178
SGA51	1	0	1	0	1	1	X	X	X	X	X	SA179 to SA182
SGA52	1	0	1	1	0	0	X	X	X	X	X	SA183 to SA186
SGA53	1	0	1	1	0	1	X	X	X	X	X	SA187 to SA190
SGA54	1	0	1	1	1	0	X	X	X	X	X	SA191 to SA194
SGA55	1	0	1	1	1	1	X	X	X	X	X	SA195 to SA198
SGA56	1	1	0	0	0	0	X	X	X	X	X	SA199 to SA202
SGA57	1	1	0	0	0	1	X	X	X	X	X	SA203 to SA206
SGA58	1	1	0	0	1	0	X	X	X	X	X	SA207 to SA210
SGA59	1	1	0	0	1	1	X	X	X	X	X	SA211 to SA214
SGA60	1	1	0	1	0	0	X	X	X	X	X	SA215 to SA218
SGA61	1	1	0	1	0	1	X	X	X	X	X	SA219 to SA222
SGA62	1	1	0	1	1	0	X	X	X	X	X	SA223 to SA226
SGA63	1	1	0	1	1	1	X	X	X	X	X	SA227 to SA230
SGA64	1	1	1	0	0	0	X	X	X	X	X	SA231 to SA234
SGA65	1	1	1	0	0	1	X	X	X	X	X	SA235 to SA238
SGA66	1	1	1	0	1	0	X	X	X	X	X	SA239 to SA242
SGA67	1	1	1	0	1	1	X	X	X	X	X	SA243 to SA246

(Continued)

(Continued)

Sector Group	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	Sectors
SGA68	1	1	1	1	0	0	X	X	X	X	X	SA247 to SA250
SGA69	1	1	1	1	0	1	X	X	X	X	X	SA251 to SA254
SGA70	1	1	1	1	1	0	X	X	X	X	X	SA255 to SA258
SGA71	1	1	1	1	1	1	0	0	X	X	X	SA259 to SA261
							0	1				
							1	0				
SGA72	1	1	1	1	1	1	1	1	0	0	0	SA262
SGA73	1	1	1	1	1	1	1	1	0	0	1	SA263
SGA74	1	1	1	1	1	1	1	1	0	1	0	SA264
SGA75	1	1	1	1	1	1	1	1	0	1	1	SA265
SGA76	1	1	1	1	1	1	1	1	1	0	0	SA266
SGA77	1	1	1	1	1	1	1	1	1	0	1	SA267
SGA78	1	1	1	1	1	1	1	1	1	1	0	SA268
SGA79	1	1	1	1	1	1	1	1	1	1	1	SA269

Common Flash Memory Interface Code

Description	A_6 to A_0	DQ_{15} to DQ_0
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h
Primary OEM Command Set 02h: AMD/FJ standard type	13h 14h	0002h 0000h
Address for Primary Extended Table	15h 16h	0040h 0000h
Alternate OEM Command Set (00h = not applicable)	17h 18h	0000h 0000h
Address for Alternate OEM Extended Table	19h 1Ah	0000h 0000h
V_{CC} Min (write/erase)DQ_7 to DQ_4=1V, DQ_3 to DQ_0=100 mV	1Bh	0027h
V_{CC} Max (write/erase)DQ_7 to DQ_4=1V, DQ_3 to DQ_0=100 mV	1Ch	0036h
V_{PP} Min voltage	1Dh	0000h
V_{PP} Max voltage	1Eh	0000h
Typical timeout per single byte/word write 2^N µs	1Fh	0004h
Typical timeout for Min size buffer write 2^N µs	20h	0000h
Typical timeout per individual sector erase 2^N ms	21h	000Ah
Typical timeout for full chip erase 2^N ms	22h	0000h
Max timeout for byte/word write 2^N times typical µs	23h	0005h
Max timeout for buffer write 2^N times typical µs	24h	0000h
Max timeout per individual sector erase 2^N times typical ms	25h	0004h
Max timeout for full chip erase 2^N times typical ms	26h	0000h
Device Size = 2^N byte	27h	0018h
Flash Device Interface description 05h: ×16 / ×32	28h 29h	0005h 0000h
Max number of byte in multi-byte write = 2^N	2Ah 2Bh	0000h 0000h
Number of Erase Block Regions within device	2Ch	0003h
Erase Block Region 1 Information bit 15 to 0: y = number of sectors bit 31 to 16: z = size (z × 256 bytes)	2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h
Erase Block Region 2 Information bit 15 to 0: y = number of sectors bit 31 to 16: z = size (z × 256 bytes)	31h 32h 33h 34h	00FDh 0000h 0000h 0001h
Erase Block Region 3 Information bit 15 to 0: y = number of sectors bit 31 to 16: z = size (z × 256 bytes)	35h 36h 37h 38h	0007h 0000h 0020h 0000h

(Continued)

(Continued)

Description	A_6 to A_0	DQ_{15} to DQ_0
Erase Block Region 4 Information bit 15 to 0: y = number of sectors bit 31 to 16: z = size (z × 256 bytes)	39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h
Query-unique ASCII string “PRI”	40h 41h 42h	0050h 0052h 0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0033h
Address Sensitive Unlock 04h = Required and 0.17µm technology	45h	0004h
Erase Suspend 02h = To Read & Write	46h	0002h
Sector Protection 00h = Not Supported X = Number of sectors in per group	47h	0001h
Sector Temporary Unprotection 01h = Supported	48h	0001h
Sector Protection Algorithm	49h	0007h
Dual Operation 00h = Not Supported, X = Total number of sectors in all Banks except Bank A	4Ah	00E7h
Burst Mode Type 00h = Not Supported	4Bh	0000h
Page Mode Type 02h = 8 Word Page	4Ch	0002h
V_{ACC} (Acceleration) Supply Minimum DQ_7 to DQ_4=1V, DQ_3 to DQ_0=100 mV	4Dh	00B5h
V_{ACC} (Acceleration) Supply Maximum DQ_7 to DQ_4=1V, DQ_3 to DQ_0=100 mV	4Eh	00C5h
Boot Type	4Fh	0001h
Program Suspend, 01h = Supported	50h	0001h
Bank Organization X = Number of Banks	57h	0004h
Bank A Region Information X = Number of sectors in Bank A	58h	0027h
Bank B Region Information X = Number of sectors in Bank B	59h	0060h
Bank C Region Information X = Number of sectors in Bank C	5Ah	0060h
Bank D Region Information X = Number of sectors in Bank D	5Bh	0027h

■ FUNCTIONAL DESCRIPTION

Simultaneous Operation

The device features functions that enable data reading from one memory bank while a program or erase operation is in progress in the other memory bank (simultaneous operation) , in addition to conventional features (read, program, erase, erase-suspend read, and erase-suspend program) . The bank is selected by bank address (A_{21}, A_{20}, A_{19}) with zero latency. The device consists of the following four banks :
Bank A : 8 × 4KW and 31× 32KW; Bank B : 96 × 32 KW; Bank C : 96 ×32KW; Bank D : 8 × 4KW and 31 × 32KW.
The device can execute simultaneous operations between Bank 1, a bank chosen from among the four banks, and Bank 2, a bank consisting of the three remaining banks. See "FlexBank™ Architecture" below. This is what we call "FlexBank", for example the rest of banks B, C and D to let the system read while Bank A is in the process of program (or erase) operation. However the different types of operations for the three banks are not allowed, e.g. Bank A programming, Bank B erasing, and Bank C reading out. With this "FlexBank", as described in "Example of Virtual Banks Combination", the system gets to select from four combinations of data volume for Bank 1 and Bank 2, which works well to meet the system requirement. The simultaneous operation cannot execute multi-function mode in the same bank. Refer to "Bank-to-Bank Read/Write(Program and Erase) Timing Diagram".

FlexBank™ Architecture

Bank Splits	Bank 1		Bank 2	
	Bank Size	Combination	Bank Size	Combination
1	16 Mbit	Bank A	112 Mbit	Bank B, C, D
2	48 Mbit	Bank B	80 Mbit	Bank A, C, D
3	48 Mbit	Bank C	80 Mbit	Bank A, B, D
4	16 Mbit	Bank D	112 Mbit	Bank A, B, C

Example of Virtual Banks Combination

Bank Splits	Bank 1			Bank 2		
	Bank Size	Combination of Memory Bank	Sector Sizes	Bank Size	Combination of Memory Bank	Sector Sizes
1	16 Mbit	Bank A	8 × 4K words, 31 × 32K words	112 Mbit	Bank B + Bank C + Bank D	8 × 4K words, 223 × 32K words
2	32 Mbit	Bank A + Bank D	16 × 4K words, 62 × 32K words	96 Mbit	Bank B + Bank C	192 × 32K words
3	48 Mbit	Bank B	96 × 32K words	80 Mbit	Bank A + Bank C + Bank D	16 × 4K words, 158 × 32K words
4	64 Mbit	Bank A + Bank B	8 × 4K words, 127 × 32Kwords	64 Mbit	Bank C + Bank D	8 × 4K words, 127 × 32Kwords

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out they output the sequence flag once they are selected. Meanwhile the system would get to read from either Bank C or Bank D.

Simultaneous Operation

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode	Read mode

Note : Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. The Bank consists of 4 banks, Bank A, Bank B, BankC and Bank D. Bank Address (BA) means to specify each of the Banks.

Read Mode

The device has two control functions required to obtain data at the outputs. $\overline{CE}$ is the power control and used for a device selection. $\overline{OE}$ is the output control and used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. Assuming the addresses have been stable for at least t_{ACC} - t_{OE} time. When reading out a data without changing addresses after power-up, input hardware reset or to change $\overline{CE}$ pin from “H” or “L”.

Page Mode Read

The device is capable of fast Page mode read and are compatible with the Page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The Page size of the device is 8 words or 4 double words, within the appropriate Page being selected by the higher address bits A_{21} to A_2 and the LSB bits A_1 to A_0 (in the double word mode) and A_1 to A_{-1}(in the word mode) determining the specific double word or word within that page. This is an asynchronous operation with the microprocessor supplying the specific double word or word location.

The random or initial page access is equal to t_{ACC} and subsequent Page read access (as long as the locations specified by the microprocessor fall within that Page) is equivalent to t_{PACC}. Here again, $\overline{CE}$ selects the device and $\overline{OE}$ is the output control and used to gate data to the output pins if the device is selected. Fast Page mode accesses are obtained by keeping A_{21} to A_2 constant and changing A_1 to A_0 to select the specific double word or changing A_1 to A_{-1} to select the specific word, within that page.

Standby Mode

There are two ways to implement the standby mode on the device, one using both the $\overline{CE}$ and $\overline{RESET}$ pins, and the other via the $\overline{RESET}$ pin only.

When using both pins, CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ input held at V_{CC}±0.3 V. Under this condition the current consumed is less than 5 µA Max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even when $\overline{CE}$=“H”. The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, CMOS standby mode is achieved with $\overline{RESET}$ input held at V_{SS}±0.3 V ($\overline{CE}$=“H” or “L”) . Under this condition the current consumed is less than 5 µA Max. Once the $\overline{RESET}$ pin is set high, the device requires t_{RH} as a wake-up time for output to be valid for read access.

During standby mode, the output is in the high impedance state regardless of $\overline{OE}$ input.

Automatic Sleep Mode

Automatic sleep mode works to restrain power consumption during read-out of the device data. This is useful in the application such as a handy terminal which requires low power consumption.

To activate this mode, the device automatically switches itself to low power mode when addresses remain stable during access time of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on this mode. The current consumed is typically 1 µA (CMOS Level).

During simultaneous operation, V_{CC} active current (I_{CC2}) is required.

Since the data are latched during this mode, the data are continuously read out. When the addresses are changed, the mode is automatically canceled and the device reads the data for changed addresses.

Output Disable

With the $\overline{OE}$ input is at logic high level (V_{IH}), output from the device is disabled. This causes the output pins to be in a high impedance state.

Autoselect

Autoselect mode allows reading out of a binary code and identifies its manufacturer and type.It is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9. Three identifier bytes may then be sequenced from the device outputs by toggling addresses. All addresses are DON'T CARES except A_6 to A_0.

The manufacturer and device codes may also be read via the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in “Command Definitions Table” of ■DEVICE BUS OPERATIONS.

In the command Autoselect mode, the bank addresses BA (A_{21}, A_{20}, A_{19}) must point to a specific bank during the third write bus cycle of the Autoselect command. Then the Autoselect data are read from that bank while array data can be read from the other bank.

A read cycle from address 00h returns the manufacturer's code (Fujitsu=04h) . A read cycle from address 01h (at word mode, 02h) outputs device code. When 2222227Eh (at word mode, 227Eh) is output, it indicates that two additional codes, called Extended Device Codes is required. Therefore the system may continue reading out these Extended Device Codes at addresses of 0Eh (at word mode, 1Ch) and 0Fh (at word mode, 1Eh). Refer to “Autoselect Codes Table” and “Extended Autoselect Code Table” in ■DEVICE BUS OPERATION.

In the case of applying V_{ID} on A_9, because both Bank 1 and Bank 2 enter Autoselect mode, simultanous operation cannot be executed.

Write

Device erase and programming are accomplished via the command register. The contents of the register serve as input to the internal state machine. The state machine output dictates the device function.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever starts later, while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever starts first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Double Word/Word Configuration

DW/$\overline{W}$ pin selects double word (32-bit) mode or word (16-bit) mode for the device. When this pin is driven high, device operates in the double word (32-bit) mode. Data is read and programmed at DQ_{31} to DQ_0. When this pin is driven low, device operates in word (16-bit) mode. Under this mode, DQ_{31}/A_{-1} pin becomes the lowest address bit, and DQ_{30} to DQ_{16} bits are tri-stated. However, the command bus cycle is always an 16-bit operation and hence commands are written at DQ_{15} to DQ_0 and DQ_{31} to DQ_{16} bits are ignored. Refer to "Double Word Mode Configuration Timing Diagram","Word Mode Configuration Timing Diagram" and "DW/$\overline{W}$ Diagram for Write Operations" in "■TIMING DIAGRAM".

Accelerated Program Operation

The device offers accelerated program operation which enables the programming in high speed. If the system asserts V_{ACC} to the ACC pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 60%. This function is primarily intended to allow high speed program, so caution is needed as the sector group becomes temporarily unprotected.

The system uses fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device automatically set to fast mode. Therefore the present sequence is used for programming and detection of completion during acceleration mode.

Removing V_{ACC} from the ACC pin and applying V_{IL} or V_{IH} returns the device to normal operation. Do not remove V_{ACC} from ACC pin while programming. See "Accelerated Program Timing Diagram".

RESET

Hardware Reset

The device may be reset by driving the $\overline{RESET}$ pin to V_{IL}. The $\overline{RESET}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least "t_{RP}" in order to properly reset the internal state machine. Any operation in the process of being executed is terminated and the internal state machine is reset to the read mode "t_{READY}" after the $\overline{RESET}$ pin is driven low. Furthermore once the $\overline{RESET}$ pin goes high the device requires an additional "t_{RH}" before it allows read access. When the $\overline{RESET}$ pin is low, the device is in the standby mode for the duration of the pulse and all the data output pins are tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location are corrupted. Please note that the RY/$\overline{BY}$ output signal should be ignored during the $\overline{RESET}$ pulse. See "$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram".

HiddenROM Region

Unlike previous flash memory devices, the MBM29XL12DF allows simultaneous operation while the HiddenROM is enabled. However, there are a number of restrictions associated with simultaneous operation and device operation when the HiddenROM is enabled:

(1) The HiddenROM is not available for reading while the Password Unlock, any PPB program/erase operation, or Password programming are in progress. Reading to any location in the Bank A will return the status of these operations until these operations have completed execution.

(2) Writing the corresponding Sector Protect latch associated with the overlaid bootblock sector results in the Sector Protect latch NOT being updated. This is only accomplished when the HiddenROM is not enabled.

(3) Reading the corresponding DPB associated with the overlaid bootblock sector results in reading invalid data when the PPB Lock/DPB Verify command is issued. This function is only accomplished when the HiddenROM is not enabled.

(4) All commands are available for execution when the HiddenROM is enabled except the following list. Issuing the following commands while the HiddenROM is enabled results in the command being ignored.

— CFI
— Set to Fast Mode
— Fast Program
— Reset from Fast Mode
— Program and Sector Erase Suspend
— Program and Sector Erase Resume

(5) Executing the Sector Erase command is permitted when the HiddenROM is enabled, however, there is no provision for erasing the HiddenROM with the Sector Erase command, regardless of the protection status. The Sector Erase command will erase all other sectors when the HiddenROM is enabled. Erasing the HiddenROM with the Embedded Algorithm is accomplished by issuing the Chip Erase command. If the HiddenROM is the only sector requiring erasure, set the Sector Protect latches for the remaining sectors prior to issuing the Chip Erase command.

(6) Executing the HiddenROM Entry command during program or erase suspend mode is allowed. Since the Sector Erase/Program Resume command is disabled while the HiddenROM is enabled, the user cannot resume programming or erase of the HiddenROM in place of the overlaid boot block sector.

HiddenROM Protection Bit

The HiddenROM Protection Bit prevents programming of the HiddenROM memory area. Once set, the Hidden-ROM memory area contents are non-modifiable.

<Protection>

The MBM29XL12DF features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

(1) Write Protect ($\overline{WP}$)[Hardware Protection]

The device features a hardware protection option using a write protect pin that prevents programming or erasing, regardless of the state of the sector's Persistent or Dynamic Protection Bits. The $\overline{WP}$ pin is associated with the "outermost" 2 × 4K words on both ends of boot sectors. The $\overline{WP}$ pin has no effect on any other sector. When $\overline{WP}$ is taken to V_{IL}, program and erase operations of the "outermost" 2 × 4K words sectors on both end are disabled. By taking $\overline{WP}$ back to V_{IH}, the "outermost" 2 × 4K words sectors are enabled for program and erase operations, depending upon the status of the individual sector Persistent or Dynamic Protection Bits. If either of the two outermost sectors Persistent or Dynamic Protection Bits are programmed, program or erase operations are inhibited. If the sector Persistent or Dynamic Protection Bits are both erased, the two sectors are available for programming or erasing as long as $\overline{WP}$ remains at V_{IH}. The user must hold the $\overline{WP}$ pin at either V_{IH} or V_{IL} during the entire program or erase operation of the "outermost" two sectors on both end of boot sectors.

(2)Sector Group Protection [Software Protection]

The device features hardware sector group protection. This feature disables both program and erase operations in any number of sector groups. The sector group protection feature is enabled using programming equipment at the user's site. The device is shipped with all sector groups unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, $\overline{CE}$ = V_{IL}, (A_6, A_5, A_4, A_3, A_2, A_1,A_0) = (0, 1, 1, 1, 0, 1, 0). The sector addresses pins (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, A_{12}, and A_{11}) should be set to the sector group to be protected. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See Sector Group Protection waveforms and algorithms.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, A_{12}, and A_{11}) while (A_6, A_5, A_4, A_3, A_2, A_1,A_0) = (0, 1, 1, 1, 0, 1, 0) produces logic "1" at device output DQ_0 for a protected sector. Otherwise the device produces logic "0" for an unprotected sector group. A_{-1} = V_{IL} is required in word mode.

It is also possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses pins (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, A_{12}, and A_{11}) represents the sector group address will produce a logical "1" at DQ_0 for a protected sector. See "User Bus Operations" for Autoselect codes.

(3) Extended Sector Group Protection [Software Protection]

In addition to normal sector group protection, the device has Extended Sector Group Protection as extended function. This function enables protection of the sector group by forcing V_{ID} on $\overline{RESET}$ pin and writes a command sequence. Unlike conventional procedures, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector group protection in this mode. The extended sector group protection requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) in the command register. Then the sector group addresses pins (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, A_{12}, and A_{11}) and (A_6, A_5, A_4, A_3, A_2, A_1, A_0) = (0, 1, 1, 1, 0, 1, 0) should be set to the sector group to be protected (setting V_{IL} for the other addresses pins is recommended) , and an extended sector group protection command (60h) should be written. A sector group is typically protected in 250 µs. To verify programming of the protection circuitry, the sector group addresses pins (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, A_{12}, and A_{11}) and (A_6, A_5, A_4, A_3, A_2, A_1, A_0) = (0, 1, 1, 1, 0, 1, 0) should be set a command (40h) should be written. Following the command write, logic "1" at device output DQ_0 produces a protected sector in the read operation. If the output is logic "0", write the extended sector group protection command (60h) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to V_{IH}. Refer to. Extended Sector Group Protection waveforms and algorithm.

(4) New Sector Protection [Software Protection]

A command sector protection method that replaces the old V_{ID} controlled protection method in future. However MBM29XL12DF supports both V_{ID} protection and Persistent Sector Protection. Both Protect supported as a shift period.

The Persistent Sector Protection and the old V_{ID} controlled protection can go back each other until Persistent Protection Lock Bit is settled.

a) Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 4 K words boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the PPB Write Command.

Note: If a PPB requires erasure, all of the sector PPBs must first be preprogrammed prior to PPB erasing. All PPBs erase in parallel, unlike programming where individual PPBs are programmable. It is the responsibility of the user to perform the preprogramming operation. Otherwise, an already erased sector PPBs has the potential of being over-erased. There is no hardware mechanism to prevent sector PPBs over-erasure.

b) Dynamic Protection Bit (DPB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DPBs is “0”. Each DPB is individually modifiable through the DPB Write Command.

When the parts are first shipped, the PPBs are cleared, the DPBs are cleared, and PPB Lock is defaulted to power up in the cleared state - meaning the PPBs are changeable.

When the device is first powered on the DPBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DPB related to that sector. For the sectors that have the PPBs cleared, the DPBs control whether or not the sector is protected or unprotected. By issuing the DPB Write/Erase command sequences, the DPBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DPBs maybe set or cleared as often as needed.

PPB vs DPB

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are Non-Volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PBB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to “1”. Setting the PPB Lock disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PBB Lock to disable any further changes to the PBBs during system operation.

The $\overline{WP}$ write protect pin adds a final level of hardware protection to the two outermost 4K words on both ends of boot sectors. When this pin is low it is not possible to change the contents of these two sectors. These sectors generally hold system boot code. So, the $\overline{WP}$ pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DPB Write command sequence is all that is necessary. The DPB write/erase command for the dynamic sectors switch the DPBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

Note: to achieve the best protection, it's recommended to execute the PPB lock bit set command early in the boot code, and protect the boot code by holding $\overline{WP}$ = V_{IL}.

DPB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DPB are changeable
1	0	0	Protected—PPB and DPB and DPB are changeable
0	1	0	Protected—PPB and DPB and DPB are changeable
1	1	0	Protected—PPB and DPB and DPB are changeable
0	0	1	Unprotected—PPB not changeable, DPB is changeable
1	0	1	Protected—PPB not changeable, DPB is changeable
0	1	1	Protected—PPB not changeable, DPB is changeable
1	1	1	Protected—PPB not changeable, DPB is changeable

The above table contains all possible combinations of the DPB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PBB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DPB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DPB, PPB, and PPB lock for a given sector can be verified by writing a DPB/PPB/PPB lock verify command to the device.

–DPB/PPB Status

The programming of the DPB/PPB for a given sector can be verified by writing a DPB/PPB status verify command to the device.

–PPB Lock Bit Status

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device.

c) Persistent Protection Bit Lock (PPB Lock)

- **PPB Locked**
- **PPB Locked with Password**

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted.

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue using the Persistent Sector Protection method, they must set the Persistent Sector Protection Mode Locking Bit. This will permanently set the part to operate only using Persistent Sector Protection. If the customer decides to use the password protection method, they must set the Password Mode Locking Bit. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the Persistent Sector Protection Mode Locking Bit or the Password Mode Locking Bit permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone. This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The $\overline{\text{WP}}$ Hardware Protection feature is always available, independent of the software managed protection method chosen.

A global volatile bit. When set to “1”, the PPBs cannot be changed. When cleared (“0”), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Locking Bit is set, which indicates the device is in Password Protection Mode, the PPB Lock Bit is also set after a hardware reset ($\overline{\text{RESET}}$ asserted) or a power-up reset. The ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting $\overline{\text{RESET}}$, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit back to a “1”.

If the Password Mode Locking Bit is not set, indicating Persistent Sector Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Sector Protection Mode.

-Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. Fujitsu recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

(1) It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.

(2) It also disables all further commands to the password region. All program, and read operations are ignored. Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see “Password Verify Command”). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

-Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

(5) Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the device in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{\text{RESET}}$ pin to high voltage (V_{ID}). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the V_{ID} is taken away from the $\overline{\text{RESET}}$ pin, all the previously protected sector groups will be protected again. While PPB Lock is set, this device cannot enter the Temporary Sector Group Unprotection mode.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Some commands require Bank Address (BA) input. When command sequences are input into bank reading, the commands have priority over the reading. "MBM29XL12DF Command Definitions Table" in ■DEVICE BUS OPERATION shows the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Also the Program Suspend (B0h) and Program Resume (30h) commands are valid only while the Program operation is in progress. Moreover, Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_{15} to DQ_0 and DQ_{31} to DQ_{16} bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to Read/Reset mode, verify mode of secter protect commands, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device automatically powers-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. Therefore manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a higher voltage. However multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated first by writing two unlock cycles. This is followed by a third write cycle that contains the bank address (BA) and the Autoselect command. Then the manufacture and device codes can be read from the bank, and actual data from the memory cell can be read from another bank. The higher order address (A_{21}, A_{20}, A_{19}) required for reading out the manufacture and device codes demands the bank address (BA) set at the third write cycle.

Following the command write, a read cycle from address (BA) 00h returns the manufacturer’s code (Fujitsu=04h). And, at double word mode, a read cycle at address (BA) 01h (at word mode, 02h) outputs device code. When 2222227Eh (at word mode, 227Eh) is output, this indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh (at word mode, 1Ch), as well as at (BA) 0Fh (at word mode, 1Eh). Refer to "MBM29XL12DF Autoselect Codes Table" and "Exteneded Auteselect Code Table" in ■DEVICE BUS OPERATION.

The sector state (PPB protection or PPB unprotection) is informed by address (SA) XX02h . Scanning the sector group addresses (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, A_{12} and A_{11}) while(A_6, A_5, A_4, A_3, A_2, A_1,A_0) = (0, 1, 1, 1, 0, 1, 0) produces logic “1” at device output DQ_0 for a protected sector group. The programming verification should be performed by verifying sector group protection on the protected sector. See "MBM29XL12DF User Bus Operations Table (DW/$\overline{W}$ = V_{IL})" and "MBM29XL12DF User Bus Operations Table (DW/$\overline{W}$ = V_{IH})" in ■DEVICE BUS OPERATION.

The manufacture and device codes can be read from the selected bank. To read the manufacture and device codes and sector protection status from a non-selected bank, it is necessary to write the Read/Reset command sequence into the register. Autoselect command should then be written into the bank to be read.

If the software (program code) for Autoselect command is stored in the Flash memory, the device and manufacture codes should be read from the other bank, which does not contain the software.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register. To execute the Autoselect command during the operation, Read/Reset command sequence must be written before the Autoselect command.

Word/Double Word Programming Command

The device is programmed on word-by-word basis (or double word-by-double word). Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later, and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) starts programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device automatically provides adequate internally generated program pulses and verify programmed cell margin.

The system can determine the status of the program operation by using DQ_7 ($\overline{Data}$ Polling), DQ_6 (Toggle Bit) or RY/$\overline{BY}$. The $\overline{Data}$ Polling and Toggle Bit must be performed at the memory location being programmed.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which device returns to the read mode and addresses are no longer latched. See "Hardware Sequence Flags". Therefore the device requires that a valid address to the device be supplied by the system in this particular instance. Hence $\overline{Data}$ Polling must be performed at the memory location being programmed.

Any commands written to the chip during this period are ignored. If hardware reset occurs during the programming operation, the data being written is not guaranteed.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still "0". Only erase operations can convert from "0"s to "1"s.

Refer to "Embedded Program™ Algorithm" using typical command strings and bus operations.

Program Suspend/Resume Command

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any address. Writing the Program Suspend command (B0h) during the Embedded Program operation immediately suspends the programming. The Program Suspend command may also be issued during a programming operation while an erase is suspended. The bank addresses of sector being programmed should be set when writing the Program Suspend command.

When the Program Suspend command is written during a programming process, the device halts the program operation within 1 µs and updates the status bits.

After the program operation has been suspended, the system can read data from any address. The data at program-suspended address is not valid. Normal read timing and command definitions apply.

After the Program Resume command (30h) is written, the device reverts to programming. The bank addresses of sectors being suspended should be set when writing the Program Resume command. The system can determine the program operation status using the DQ_7 or DQ_6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the Autoselect command sequence in the Program Suspend mode. The device allows reading Autoselect codes at the addresses within programming sectors, since the codes are not stored in the memory. When the device exits from the Autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Program Resume command (address bits are "Bank Address") to exit from the Program Suspend mode and continue programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming.

Chip Erase Command

Chip erase is a six-bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. (Preprogram Function) The system is not required to provide any controls or timings during these operations.

The system can determine the erase operation status by using DQ_7 ($\overline{Data}$ Polling), or DQ_6 (Toggle Bit). The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on DQ_7 is “1” (See "Write Operation Status" section.) at which the device returns to read the mode.

Chip Erase Time: Sector Erase Time $\times$ All sectors + Chip Program Time (Preprogramming)

Refer to "Embedded Erase™ Algorithm" for typical command strings and bus operations.

Sector Erase Command

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever starts later, while the command (Data = 30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever states first. After time-out of “t_{TOW}” from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors are erased concurrently by writing the six bus cycle operations on "MBM29XL12DF Command Definitions Table" in ■DEVICE BUS OPERATION. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “t_{TOW}” otherwise that command is not accepted and erasure does not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of “t_{TOW}” from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever starts first initiates the execution of the Sector Erase command(s). If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever starts first occurs within the “t_{TOW}” time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, "Sector Erase Timer".) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun may corrupt the data in the sector. In that case restart the erase on those sectors and allow them to complete. Refer to "Write Operation Status" section for Sector Erase Timer operation. Loading the sector erase buffer may be done in any sequence and with any number of sectors.

Sector erase does not require the user to program prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling), or DQ_6 (Toggle Bit).

The sector erase begins after the “t_{TOW}” time out from the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever starts first for the last sector erase command pulse and terminates when the data on DQ_7 is “1” at which time the device returns to the read mode. See "Write Operation Status" section. $\overline{Data}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] $\times$ Number of Sector Erase.

In case of multiple sector erase across bank boundaries, a read from the bank (read-while-erase) to which sectors being erased belong cannot be performed.

Refer to "Embedded Erase™ Algorithm" for typical command strings and bus operations.

Erase Suspend/Resume Command

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command is ignored during the Chip Erase operation. Writting the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The addresses are “DON’T CARES” when writting the Erase Suspend or Erase Resume command.When the Erase Suspend command is written during the Sector Erase operation, the device takes a maximum of “t_{SPD}” to suspend the erase operation. When the device has entered the erase-suspended mode, the DQ_7 bit is at logic “1”, and DQ_6 stops toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation is suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation is suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode causes DQ_2 to toggle. See the section on DQ_2.

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode causes DQ_2 to toggle. The end of the erase-suspended program operation is detected by the $\overline{\text{Data}}$ polling of DQ_7 or by the Toggle Bit I (DQ_6) which is the same as the regular program operation. Note that DQ_7 must be read from the program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point is ignored. Another Erase Suspend command is written after the chip resumes erasing.

Fast Mode

Fast Mode function dispenses with the initial two unlock cycles required in the standard program command sequence writing Fast Mode command into the command register. In this mode the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. The read operation is also executed after exiting this mode. During the Fast mode, do not write any commands other than the Fast program/ Fast mode reset command. To exit this mode, write Fast Mode Reset command into the command register. Refer to "Embedded Program Algorithm for Fast Mode". The V_{CC} active current is required even $\overline{CE}$ = V_{IH} during Fast Mode.

Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). Refer to "Embedded Program Algorithm for Fast Mode".

Query (CFI:Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of device. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. Refer to "Common Flash Memory Interface Code" in ■FLEXIBLE SECTOR-ERASE ARCHITECTURE in detail.

The operation is initiated by writing the query command (98h) into the command register. Following the command write, a read cycle from specific address retrives device information. Please note that output data of upper byte (DQ_{31} to DQ_{16}) is “0” in word mode (16 bit) read. To terminate operation, write the Read/Reset command sequence into the register.

HiddenROM Entry Command

The device has a HiddenROM area with One Time Protect function. This area is to enter the security code and to unable the change of the code once set. Program/erase is possible in this area until it is protected. However once it is protected, it is impossible to unprotect. Therefore extreme caution is required.

HiddenROM area is 128 words in Bank A. This area is normally the “outermost” 8K words boot block area. Therefore, write the HiddenROM entry command sequence to enter the HiddenROM area. It is called HiddenROM mode when the HiddenROM area appears.

The following commands are permitted after issuing the HiddenROM Entry command:

1. Autoselect
2. Password Program
3. Password Verify
4. Password Unlock
5. Read/Reset
6. Program
7. Chip and Sector Erase
8. HiddenROM Protection Bit Program
9. PPB Program
10. All PPB Erase
11. PPB Lock Bit Set
12. DPB Write
13. DPB/PPB/PPB Lock Bit Verify
14. HiddenROM Exit

The following commands are unavailable when the HiddenROM is enabled. Issuing the following commands while the HiddenROM is enabled results in the command being ignored.

1. CFI
2. Set to Fast Mode
3. Fast Program
4. Reset from Fast Mode
5. Program and Sector Erase Suspend
6. Program and Sector Erase Resume

The HiddenROM Entry command is allowed when the device is in either program or erase suspend modes. If the HiddenROM is enabled, the program or erase suspend command is ignored. This prevents resuming either programming or erase on the HiddenROM if the overlayed sector is undergoing programming or erase. It is the responsibility of the software to resume the program or erase of a suspended program or erase after exiting the HiddenROM.

Executing any of the PPB program/erase commands, or Password Unlock command results in the Bank A returning the status of these operations while they are in progress, thus making the HiddenROM unavailable for reading. If the HiddenROM is enabled while the DPB command is issued, the DPB for the overlayed sector is not updated. Reading the DPB status using the PPB Lock Bit/DPB verify command when the HiddenROM is enabled returns invalid data.

HiddenROM Program Command

To program the data to the HiddenROM area, write the HiddenROM program command sequence during HiddenROM mode. This command is the same as the program command in usual except to write the command during HiddenROM mode. Therefore the detection of completion method is the same as using the DQ_7 data polling, and DQ_6 toggle bit. Need to pay attention to the address to be programmed. If the address other than the HiddenROM area is selected to program, data of the address are changed.

HiddenROM Protect Command

The method to protect the HiddenROM is to apply high voltage (V_{ID}) to A_9 and $\overline{OE}$, set the sector address in the HiddenROM area and (A_6, A_5, A_4, A_3, A_2, A_1, A_0) = (0, 1, 1, 1, 0, 1, 0), and apply the write pulse during the HiddenROM mode. To verify the protect circuit, apply high voltage (V_{ID}) to A_9, specify (A_6, A_5, A_4, A_3, A_2, A_1, A_0) = (0, 0, 1, 1, 0, 1, 0) and the sector address in the HiddenROM area, and read. When “1” appears on DQ_0, the protect setting is completed. “0” appears on DQ_0 if it is not protected. Please apply write pulse agian. The same command sequence could be used for the above method because other than the HiddenROM mode, it is the same as the sector protect in the past.

And the device has also HiddenROM protect command without V_{ID}. See "MBM29XL12DF Command Definitions Table" in ■DEVICE BUS OPERATION.

Other sector will be effected if the address other than those for HiddenROM area is selected for the sector address, so please be carefull. Once it is protected, protection can not be cancelled, so please pay the closest attention.

Another method to protect is to issue HiddenROM Protection Bit Program Command. This is able to protect HiddenROM area by command only.

Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. In word mode, 4 Password Program commands (In double word mode. 2 Password Program commands)are required to program the password. The user must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming “0”s. Programming a “1” after a cell is programmed as a “0” results in a time-out by the Embedded Program Algorithm with the cell remaining as a “0”. The password is all F’s when shipped from the factory. All 64-bit password combinations are valid as a password.

Password Programming is permitted if the HiddenROM is enabled.

Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F’s onto the DQ data bus.

The Password Verify command is permitted if the HiddenROM is enabled. Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A_1:A_0) are valid during the Password Verify. Writing the Read/Reset command returns the device back to normal operation.

Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. Once programmed, the Password Protection Mode Locking Bit cannot be erase. If the Password Protection Mode Locking Bit is verified as program without margin, the Password Protection Mode Locking Bit Program command can be executed to improve the program margin. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. Exiting the Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

The Password Protection Mode Locking Bit Program command is permitted if the HiddenROM is enabled.

Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin. By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

The Persistent Sector Protection Mode Locking Bit Program command is permitted if the HiddenROM is enabled.

PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched into the DPBs. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the Read/Reset command.

The PPB Lock Bit Set command is permitted if the HiddenROM is enabled.

DPB Write(Erase) Command

The DPB Write command is used to set or clear a DPB for a given sector. The high order address bits (A_{21} to A_{11}) are issued at the same time as the code 01h or 00h on DQ_7 to DQ_0. All other DQ data bus pins are ignored during the data write cycle. The DPBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DPBs are cleared at power-up or hardware reset.Exiting the DPB Write command is accomplished by writing the Read/Reset command.

The DPB Write command is permitted if the HiddenROM is enabled.

DPB /PPB Verify command

DPB/PPB verify command is uesed to verify the status of several sectors.
Scanning the sector addresses (SA) will produce a logical "1" at the device output DQ_0 for a protected sector.
Otherwise the device will produce "0" at DQ_0 for the sector which is not protected.
The DPB/PPB verify erify command is permitted if the HiddenROM is enabled.

PPB Lock Bit Verify command

PPB Lock Bit verify command is used to verify the status of a PPB Lock Bit.
A logical "1" at the device output DQ_1 indicates that the PPB Lock Bit is set.
If PPB Lock Bit is not set, DQ_1 will output"0".The PPB Lock Bit verify command is permitted if the HiddenROM is enabled.

Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. A_0 and A_1 are used to determine the 16 bit data quantity is used to match separated 16 bits. Writing the Password Unlock command is address order specific. In other words, the lowers address A_1:A_0 = 00, the next cycle command is to A_1:A_0 = 01, then to A_1:A_0 = 10, and finally to A_1:A_0 = 11. Writing out of sequence results in the Password Unlock not returning a match with the password and the PPB Lock Bit remains set.

Once the Password Unlock command is entered, the RY/$\overline{BY}$ pin goes LOW indicating that the device is busy. Also, reading the Bank A results in the DQ6 pin toggling, indicating that the Password Unlock function is in progress. Reading the other bank returns actual array data. Approximately 1µs is required for each portion of the unlock. Once the first portion of the password unlock completes (RY/$\overline{BY}$ is not driven and DQ_6 does not toggle when read), the next cycle is issued, only this time with the next part of the password. Seven cycles Password Unlock commands are required to successfully clear the PPB Lock Bit. As with the first Password Unlock command, the RY/$\overline{BY}$ signal goes LOW and reading the device results in the DQ_6 pin toggling on successive read operations until complete. It is the responsibility of the microprocessor to keep track of the number of Password Unlock cycles, the order, and when to read the PPB Lock bit to confirm successful password unlock.

The Password Unlock command is permitted if the HiddenROM is enabled.

PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (A_{21} to A_{11}) are written at the same time as the program command 60h with A_6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin.

The PPB Program command is permitted if the HiddenROM is enabled. The PPB Program command does not follow the Embedded Program algorithm.

All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written (60h) and A_6 = 1, all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased with-out margin, the erase command should be reissued to improve the program margin.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

The All PPB Erase command is permitted if the HiddenROM is enabled.

Write Operation Status

Detailed in "Hardware Sequence Flags" are all the status flags which can determine the status of the bank for the current mode operation. The read operation from the bank which doesn't operate Embedded Algorithm returns data of memory cells. These bits offer a method for determining whether an Embedded Algorithm is properly completed. The information on DQ_2 is address-sensitive. This means that if an address from an erasing sector is consecutively read, the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consecutively read. This allows users to determine which sectors are in erase and which are not.

The status flag is not output from banks (non-busy banks) which do not execute Embedded Algorithms. For example, a bank (busy bank) is executing an Embedded Algorithm. When the read sequence is [1] < busy bank >, [2] < non-busy bank >, [3] < busy bank >, the DQ_6 toggles in the case of [1] and [3]. In case of [2], the data of memory cells are output. In the erase-suspend read mode with the same read sequence, DQ_6 will not be toggled in [1] and [3].

Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle*1
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1*2
	Program Suspended Mode	Program Suspend Read (Program Suspended Sector)	Data	Data	Data	Data	Data
		Program Suspend Read (Non-Program Suspended Sector)	Data	Data	Data	Data	Data
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

*1: Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle.
*2: Reading from non-erase suspend sector address will indicate logic "1" at the DQ_2 bit.

Notes: • DQ_0 and DQ_1 are reserve pins for future use.
• DQ_4 is limited to Fujitsu internal use.

DQ_7

$\overline{\text{Data}}$ Polling

The device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce a complement of data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ_7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read device will produce a "1" on DQ_7. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in "Data Polling Algorithm".

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the fourth write pulse in the four write pulse sequences.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequences. $\overline{\text{Data}}$ Polling must be performed at sector addresses of sectors being erased, not protected sectors. Otherwise the status may become invalid.

If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on DQ_7 is active for approximately 1 µs, then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on DQ_7 is active for approximately 400 µs, then the bank returns to read mode.

Once the Embedded Algorithm operation is close to being completed, the device data pins (DQ_7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that device is driving status information on DQ_7 at one instant, and then that byte's valid data at the next instant. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if device has completed the Embedded Algorithm operation and DQ_7 has a valid data, data outputs on DQ_0 to DQ_6 may still be invalid. The valid data on DQ_0 to DQ_7 will be read on successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. See "Toggle Bit Status" and "$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram".

DQ_6

Toggle Bit I

The device also features the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the busy bank will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequences. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequences. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written is protected, the toggle bit will toggle for about 1 µs and then stop toggling with data unchanged. In erase, the device will erase all selected sectors except for protected ones. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 µs and then drop back into read mode, having data kept remained.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ_6 to toggle.

The system can use DQ_6 to determine whether a sector is actively erased or is erase-suspended. When a bank is actively erased (that is, the Embedded Erase Algorithm is in progress) , DQ_6 toggles. When a bank enters the Erase Suspend mode, DQ_6 stops toggling. Successive read cycles during erase-suspend-program cause DQ_6 to toggle.

To operate toggle bit function properly, $\overline{CE}$ or $\overline{OE}$ must be high when bank address is changed.

See "AC Wavefrom for Toggle Bit I during Embedded Algorithm Operations".

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count) . Under these conditions DQ_5 will produce "1". This is a failure condition indicating that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down device under these conditions (to approximately 2 mA) . The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in "MBM29XL12DF User Bus Operations Table (DW/$\overline{W}$ = V_{IL})" and "MBM29XL12DF User Bus Operations Table (DW/$\overline{W}$ = V_{IH})" in ■DEVICE BUS OPERATION.

The DQ_5 failure condition may also appear if a user tries to program a non-blank location without pre-erase. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads valid data on DQ_7 bit and DQ_6 never stop toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a “1.” Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset device with the command sequence.

DQ_3
Sector Erase Timer

After completion of the initial sector erase command sequence, sector erase time-out begins. DQ_3 will remain low until the time-out is completed. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates that a valid erase command has been written, DQ_3 may be used to determine whether the sector erase timer window is still open. If DQ_3 is high (“1”) the internally controlled erase cycle has begun. If DQ_3 is low (“0”) , the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See “Hardware Sequence Flags”.

DQ_2
Toggle Bit II

This toggle bit II, along with DQ_6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the non-erase suspended sector will indicate a logic “1” at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows :

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also “Toggle Bit Status” and "DQ_2 vs DQ_6".

Furthermore DQ_2 can also be used to determine which sector is being erased. At the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

To operate toggle bit function properly, $\overline{\text{CE}}$ or $\overline{\text{OE}}$ must be high when bank address is changed.

Reading Toggle Bits DQ_6/DQ_2

Whenever the system initially begins reading toggle bit status, it must read DQ_7 to DQ_0 at least twice in a row to determine whether a toggle bit is toggling. Typically a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ_7 to DQ_0 on the following read cycle.

However, if, after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ_5 is high (see the section on DQ_5) . If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ_5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ_5 has not gone high. The system may continue to monitor the toggle bit and DQ_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. Refer to “Toggle Bit Algorithm”.

Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle *
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle	1 *

* : Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

RY/$\overline{BY}$ (Ready/Busy Pin)

The device provides a RY/$\overline{BY}$ open-drain output pin as a way to indicate to the host system that Embedded Algorithms are either in progress or have been completed. If output is low, the device is busy with either a program or erase operation. If output is high, the device is ready to accept any read/write or erase operation. If the device is placed in an Erase Suspend mode, RY/$\overline{BY}$ output will be high.

During programming, the RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth write pulse. During an erase operation, the RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth write pulse. The RY/$\overline{BY}$ pin will indicate a busy condition during $\overline{RESET}$ pulse. Refer to the following detailed timing diagrams. The RY/$\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up device automatically resets internal state machine to Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequence.

Device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO} (Min). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO} (Min).

If the Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector(s) can not be used.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with Respect to Ground. All pins except A_9, $\overline{OE}$, $\overline{RESET}$ and ACC *1, *2	V_{IN}, V_{OUT}	–0.5	V_{CC}+0.5	V
Power Supply Voltage *1, *2	V_{CC}	–0.5	+4.0	V
A_9, $\overline{OE}$, $\overline{RESET}$ and ACC *1, *3	V_{IN}	–0.5	+13.0	V

*1 : Voltage is defined on the basis of V_{SS}=GND=0V.

*2 : Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions,inputs may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

*3 : Minimum DC input voltage on A_9, $\overline{OE}$, $\overline{RESET}$ and ACC pins is –0.5 V. During voltage transitions, A_9, $\overline{OE}$, $\overline{RESET}$ and ACC pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN} – V_{CC}) does not exceed +9.0 V. Maximum DC input voltage on A_9, $\overline{OE}$, $\overline{RESET}$ and ACC pins is +13.0 V which may overshoot to +14.0V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Part No.	Value		Unit
			Min	Max	
Ambient Temperature	T_A	MBM29XL12DF-70/80	–40	+85	°C
Power Supply Voltage *	V_{CC}	MBM29XL12DF-70	+3.0	+3.6	V
		MBM29XL12DF-80	+2.7	+3.1	V

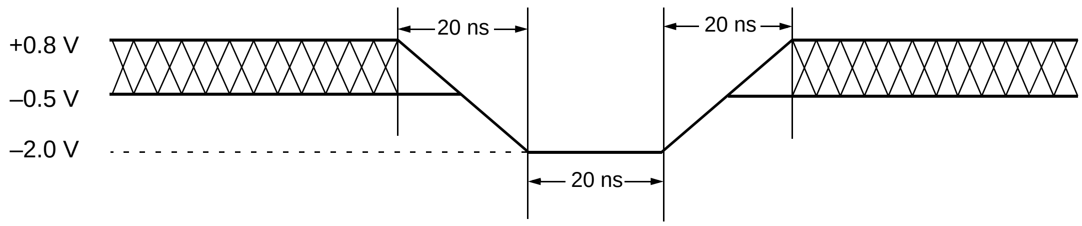
* : Voltage is defined on the basis of V_{SS}=GND=0V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

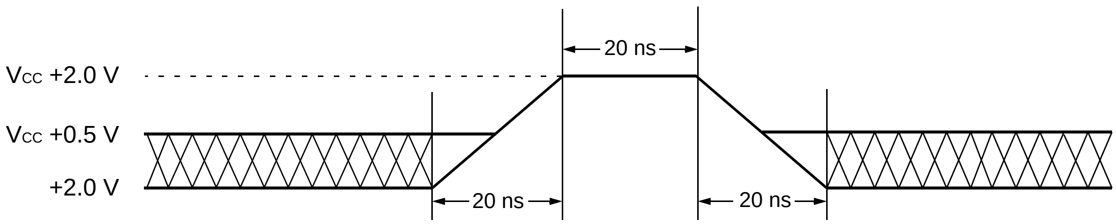
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

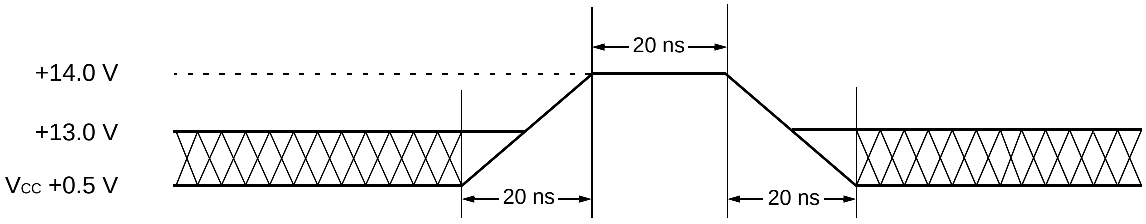
■ MAXIMUM OVERSHOOT / MAXIMUM UNDERSHOOT



Maximum Undershoot Waveform



Maximum Overshoot Waveform 1



Note: This waveform is applied for A_9, $\overline{OE}$, $\overline{RESET}$, and ACC.

Maximum Overshoot Waveform 2

■ DC CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max	–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max	–1.0	—	+1.0	µA
A_9, $\overline{OE}$, $\overline{RESET}$, ACC Inputs Leakage Current	I_{LIT}	$V_{CC} = V_{CC}$ Max, A_9, $\overline{OE}$, $\overline{RESET}$, ACC= 12.5V	—	—	35	µA
ACC Accelerated Program Current	I_{LIA}	$V_{CC} = V_{CC}$ Max, ACC = V_{ACC} Max	—	—	20	mA
V_{CC} Active Current *1 (Initial/Random Read)	I_{CC1}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ f = 10MHz	—	—	70	mA
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ f = 5MHz	—	—	35	mA
V_{CC} Active Current *2	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	35	mA
V_{CC} Current (Standby)	I_{CC3}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V, $\overline{WP} = V_{CC} \pm 0.3$ V	—	1	5	µA
V_{CC} Current (Standby,Reset)	I_{CC4}	$V_{CC} = V_{CC}$ Max, $\overline{RESET} = V_{SSQ} \pm 0.3$ V	—	1	5	µA
V_{CC} Current (Page Mode) *3	I_{CC5}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 40MHz	—	—	15	mA
V_{CC} Current (Automatic Sleep Mode) *4	I_{CC6}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{SS} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V	—	1	5	µA
V_{CC} Active Current*6 (Read-While-Program)	I_{CC7}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	50	mA
V_{CC} Active Current*6 (Read-While-Erase)	I_{CC8}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	50	mA
V_{CC} Active Current*6 (Erase-Suspend-Program)	I_{CC9}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	35	mA

(Continued)

(Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Input Low Voltage	V_{IL}	—	–0.5	—	0.6	V
Input High Voltage *5	V_{IH}	—	V_{CC}–0.2	—	V_{CC}+0.3	V
Voltage for Auteselect and Sector Protection(A_9, $\overline{OE}$, $\overline{RESET}$)*7	V_{ID}	—	11.5	12.0	12.5	V
Voltage for ACC Program Acceleration	V_{ACC}	—	11.5	12.0	12.5	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA, V_{CC} = V_{CC} Min	—	—	0.45	V
Output High Voltage	V_{OH1}	I_{OH} = –2.0 mA, V_{CC} = V_{CC} Min	V_{CC}–0.4	—	—	V
	V_{OH2}	I_{OH} = –100 µA, V_{CC} = V_{CC} Min	V_{CC}–0.2	—	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—	2.3	2.4	2.5	V

*1 : I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2 : I_{CC} active while Embedded Algorithm (Program or Erase) is in progress.

*3 : Addresses except A_1, A_0, (A_{-1}) are fixed.

*4 : Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

*5 : About V_{IH} Min , it should be applied larger voltage.

*6 : Embedded Algorithm (Program or Erase) is in progress.(@5 MHz)

*7 : V_{ID} is only for Sector Group Protection operation and Autoselect mode.

■ AC CHARACTERISTICS

• **Read Only Operations Characteristics**

Parameter	Symbol		Condition	Value *				Unit
				70		80		
	JEDEC	Standard		Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	70	—	80	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	—	70	—	80	ns
Page Read Cycle Time	—	t_{PRC}	—	25	—	30	—	ns
Page Address to Output Delay	—	t_{PACC}	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	—	25	—	30	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE}$ = V_{IL}	—	70	—	80	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	25	—	30	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	25	—	30	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	25	—	30	ns
Output Hold Time From Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	4	—	5	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	—	20	ns

* : Test Conditions :
Output Load: V_{CC} = 2.7 V to 3.1 V :1 TTL gate and 30pF (MBM29XL12DF-70/80)
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V or V_{CC}
Timing measurement reference level
Input: $0.5 \times V_{CC}$
Output: $0.5 \times V_{CC}$

- **Write (Erase/Program) Operations**

Parameter	Symbol		Value						Unit
			70			80			
	JEDEC	Standard	Min	Typ	Max	MIn	Typ	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70	—	—	80	—	—	ns
Address Setup Time	t_{AVWL}	t_{AS}	0	—	—	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling	—	t_{ASO}	12	—	—	12	—	—	ns
Address Hold Time	t_{WLAX}	t_{AH}	45	—	—	45	—	—	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling	—	t_{AHT}	0	—	—	0	—	—	ns
Data Setup Time	t_{DVWH}	t_{DS}	35	—	—	45	—	—	ns
Data Hold Time	t_{WHDX}	t_{DH}	0	—	—	0	—	—	ns
Output Enable Hold Time: Read	—	t_{OEH}	0	—	—	0	—	—	ns
Output Enable Hold Time: Toggle and $\overline{Data}$ Polling	—	t_{OEH}	10	—	—	10	—	—	ns
$\overline{CE}$ High During Toggle Bit Polling	—	t_{CEPH}	20	—	—	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling	—	t_{OEPH}	20	—	—	20	—	—	ns
Read Recover Time Before Write	t_{GHWL}	t_{GHWL}	0	—	—	0	—	—	ns
Read Recover Time Before Write	t_{GHEL}	t_{GHEL}	0	—	—	0	—	—	ns
$\overline{CE}$ Setup Time	t_{ELWL}	t_{CS}	0	—	—	0	—	—	ns
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0	—	—	0	—	—	ns
$\overline{CE}$ Hold Time	t_{WHEH}	t_{CH}	0	—	—	0	—	—	ns
$\overline{WE}$ Hold Time	t_{EHWH}	t_{WH}	0	—	—	0	—	—	ns
Write Pulse Width	t_{WLWH}	t_{WP}	35	—	—	35	—	—	ns
$\overline{CE}$ Pulse Width	t_{ELEH}	t_{CP}	35	—	—	35	—	—	ns
Write Pulse Width High	t_{WHWL}	t_{WPH}	30	—	—	30	—	—	ns
$\overline{CE}$ Pulse Width High	t_{EHEL}	t_{CPH}	30	—	—	30	—	—	ns
Programming Operation: Double Word	t_{WHWH1}	t_{WHWH1}	—	12	—	—	12	—	µs
Programming Operation: Word	t_{WHWH1}	t_{WHWH1}	—	6	—	—	6	—	µs
Sector Erase Operation*1	t_{WHWH2}	t_{WHWH2}	—	0.5	—	—	0.5	—	s
V_{CC} Setup Time	—	t_{VCS}	50	—	—	50	—	—	µs
Rise Time to V_{ID} *2	—	t_{VIDR}	500	—	—	500	—	—	ns
Rise Time to V_{ACC}*3	—	t_{VACCR}	500	—	—	500	—	—	ns
Voltage Transition Time *2	—	t_{VLHT}	4	—	—	4	—	—	µs
Write Pulse Width*2	—	t_{WPP}	100	—	—	100	—	—	µs
$\overline{OE}$ Setup Time to $\overline{WE}$ Active*2	—	t_{OESP}	4	—	—	4	—	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$ Active*2	—	t_{CSP}	4	—	—	4	—	—	µs

(Continued)

(Continued)

Parameter	Symbol		Value						Unit
			70			80			
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Recover Time from RY/$\overline{BY}$	—	t_{RB}	0	—	—	0	—	—	ns
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	—	500	—	—	ns
$\overline{RESET}$ High Level Period Before Read	—	t_{RH}	200	—	—	200	—	—	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay	—	t_{BUSY}	—	—	90	—	—	90	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	70	—	—	80	ns
Erase Time-out Time	—	t_{TOW}	50	—	—	50	—	—	µs
Erase Suspend Transition Time	—	t_{SPD}	—	—	20	—	—	20	µs
DW/$\overline{W}$ Switching Low to Output High-Z	—	t_{FLQZ}	—	—	30	—	—	30	ns
DW/$\overline{W}$ Switching High to Output Active	—	t_{FHQV}	70	—	—	80	—	—	ns

*1 : This does not include the preprogramming time.

*2 : This timing is for Sector Group Protection operation.

*3 : This timing is limited for Accelerated Program operation only.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Value			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	0.5	2	s	Excludes programming time prior to erase
Double Word Programming Time	—	12	150	µs	Excludes system-level overhead
Word Programming Time	—	6	100	µs	Excludes system-level overhead
Chip Programming Time	—	50.3	200	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

Notes : • Typical Erase Conditions: T_A = +25°C, V_{CC} = 2.9 V
• Typical Program Conditions: T_A = +25°C, V_{CC} = 2.9 V, Data = Checker

■ SSOP PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	7.0	10.0	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	6.0	12.0	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	7.5	11.0	pF

Notes : • Test Conditions: T_A = +25°C, f = 1.0 MHz
• DQ_{31}/A_{-1} pin capacitance is stipulated by Output Capacitance.

■ FBGA PIN CAPACITANCE

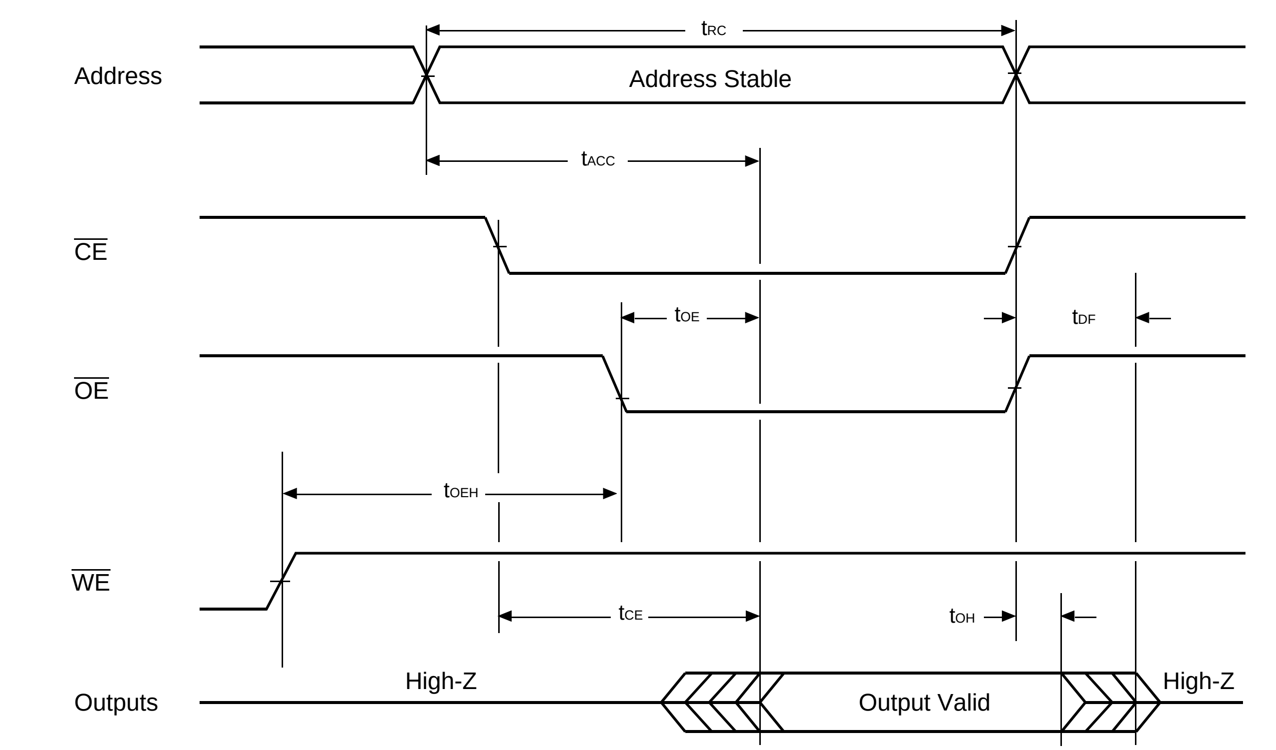
Parameter	Symbol	Test Setup	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0	TBD	TBD	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	TBD	TBD	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	TBD	TBD	pF

Note : • Test Conditions: T_A = +25°C, f = 1.0 MHz
• DQ_{31}/A_{-1} pin capacitance is stipulated by Output Capacitance.

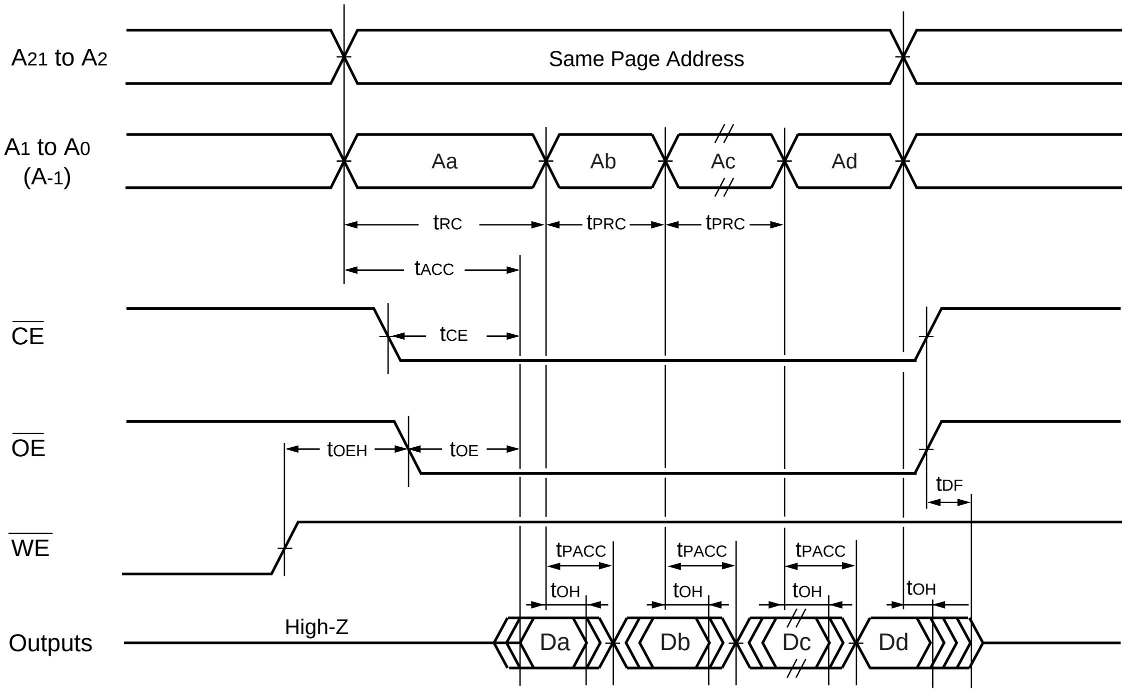
■ TIMING DIAGRAM

• **Key to Switching Waveforms**

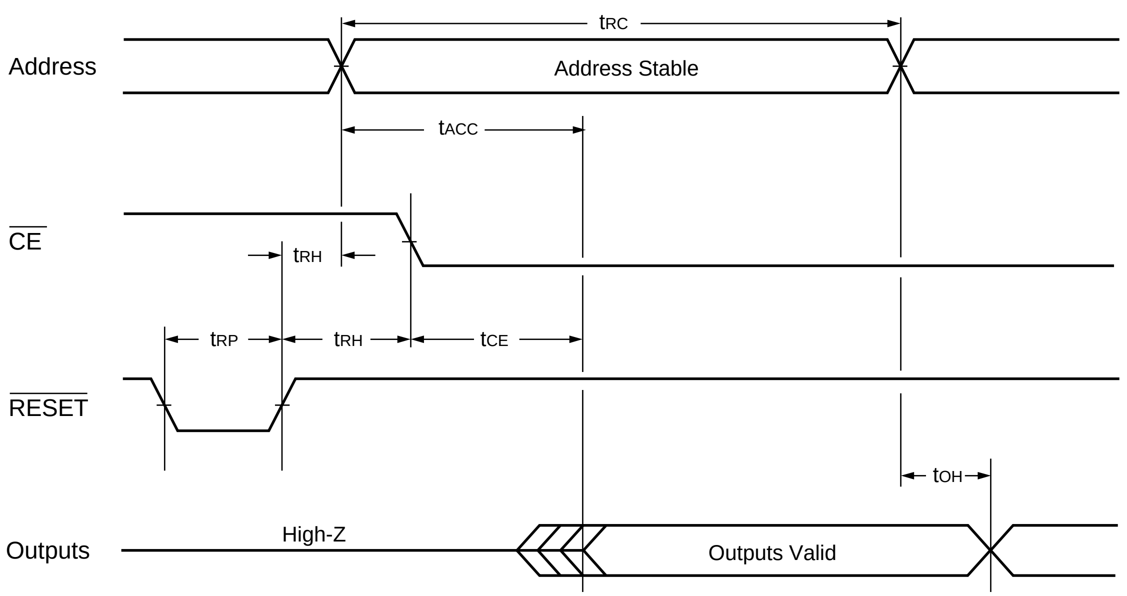
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Change from H to L
	May Change from L to H	Will Be Change from L to H
	"H" or "L": Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State



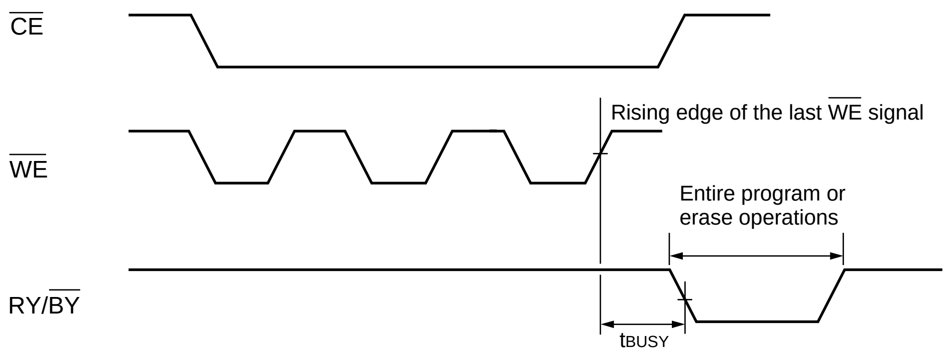
Read Operation Timing Diagram



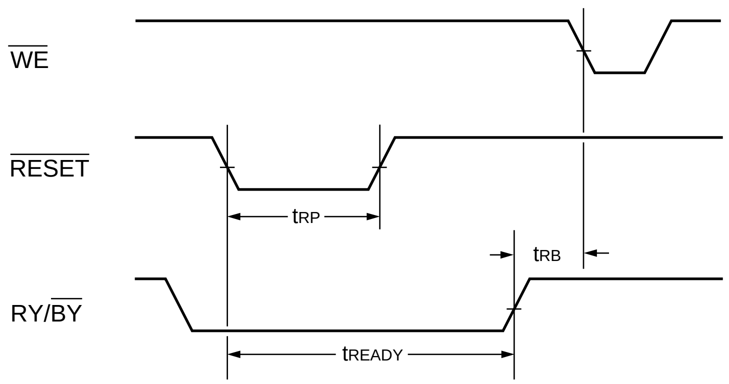
Page Read Operation Timing Diagram



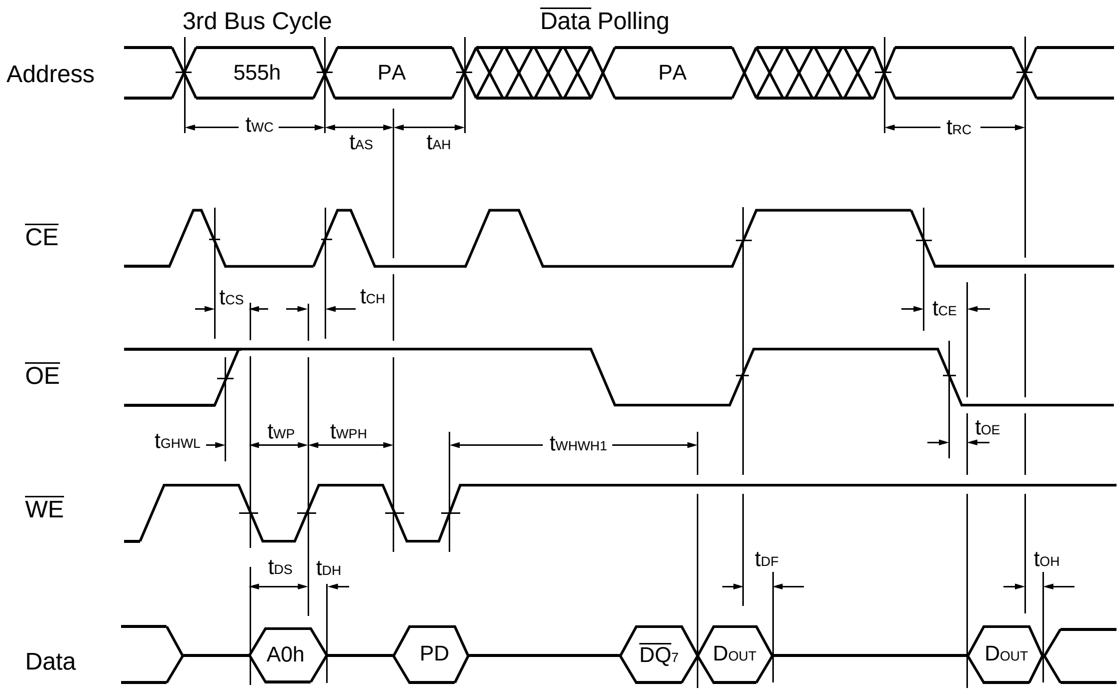
Hardware Reset/Read Operation Timing Diagram



RY/BY Timing Diagram during Program/Erase Operation Timing Diagram

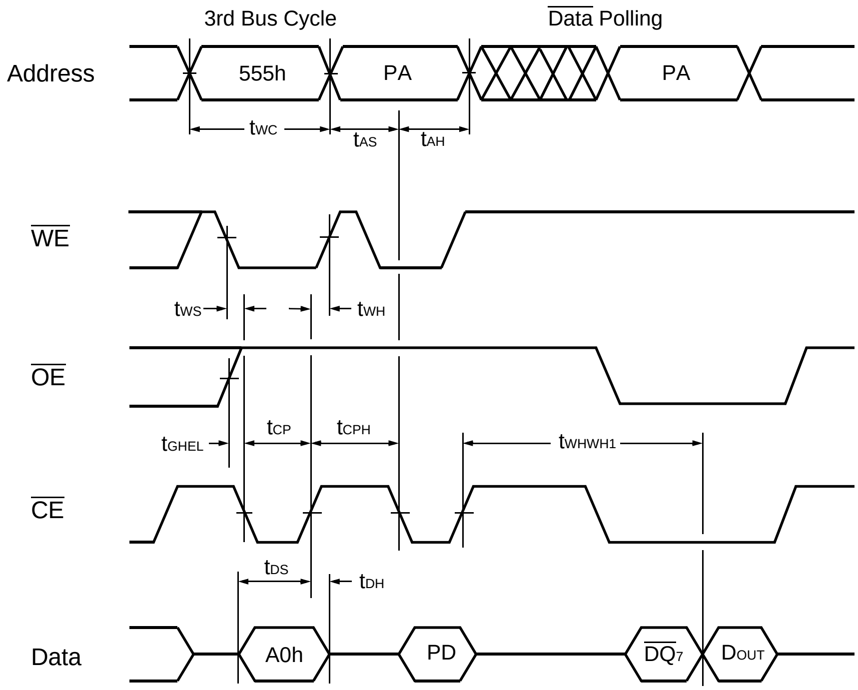


RESET, RY/BY Timing Diagram



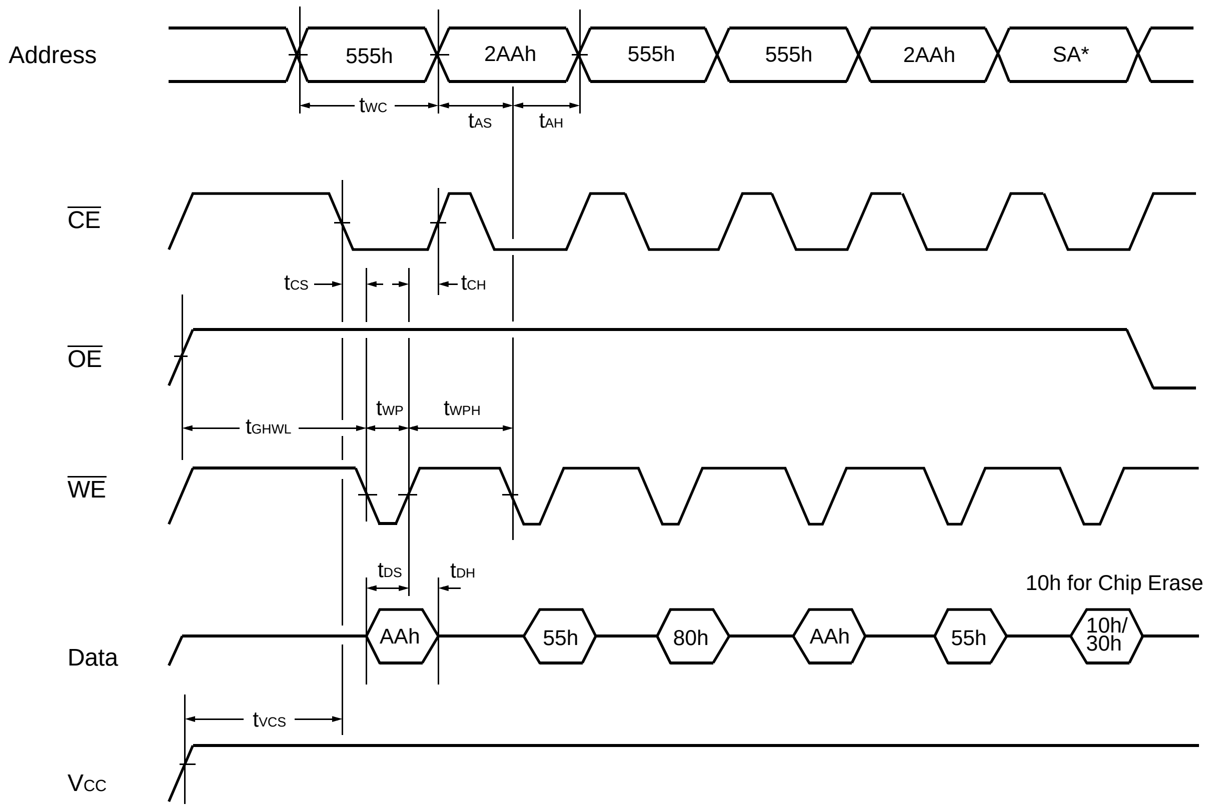
Notes: • PA is address of the memory location to be programmed.
• PD is data to be programmed at word address (x16 mode).
• $\overline{DQ_7}$ is the output of the complement of the data written to the device.
• D_{OUT} is the output of the data written to the device.
• Figure indicates last two bus cycles out of four bus cycle sequence.
• These waveforms are for the ×32 mode. (The addresses differ from ×16 mode.)

Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram



Notes:
- PA is address of the memory location to be programmed.
- PD is data to be programmed at word address (x16 mode).
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×32 mode. (The addresses differ from ×16 mode.)

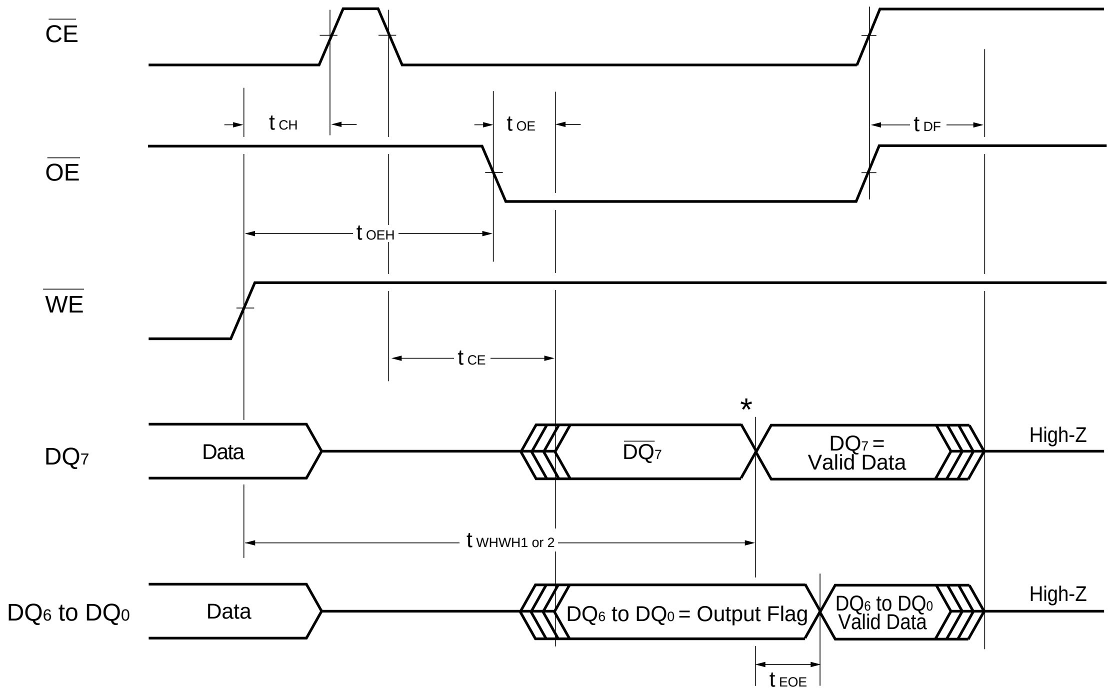
Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram



* : SA is the sector address for Sector Erase. Address = 555h (Double Word). AAAh (Word) for Chip Erase.

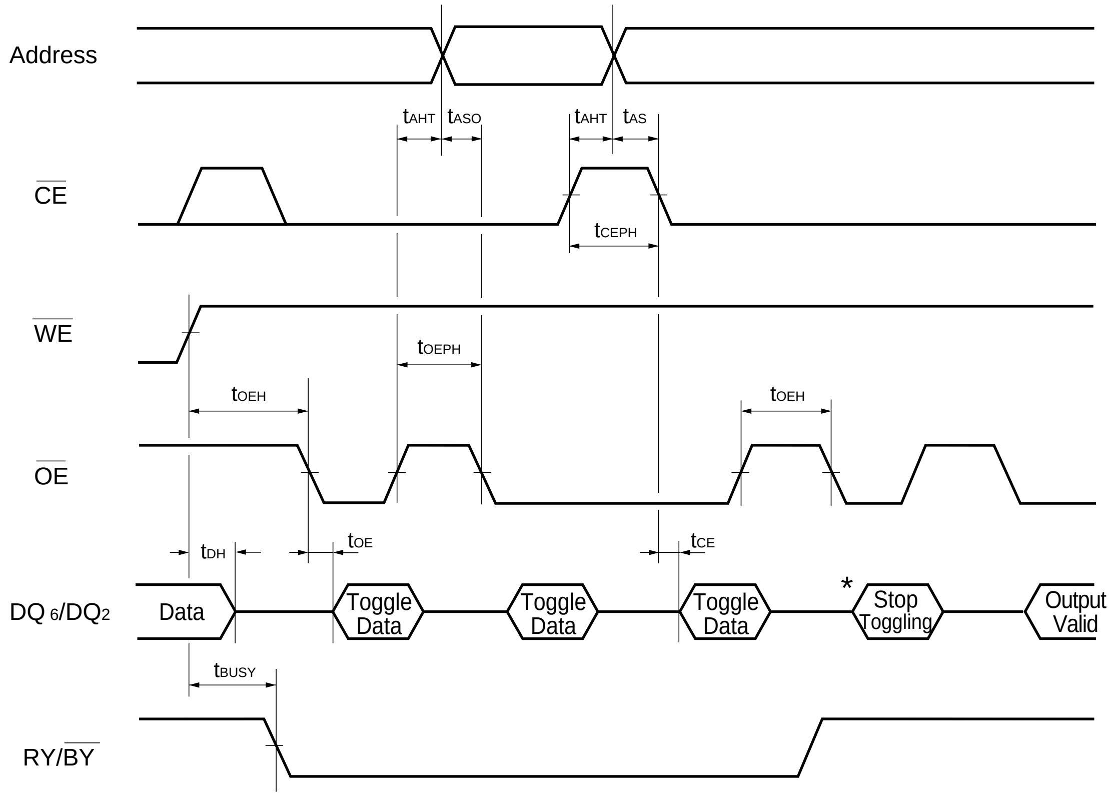
Note : These waveforms are for the ×32 mode. (The addresses differ from ×16 mode.)

Chip/Sector Erase Operation Timing Diagram



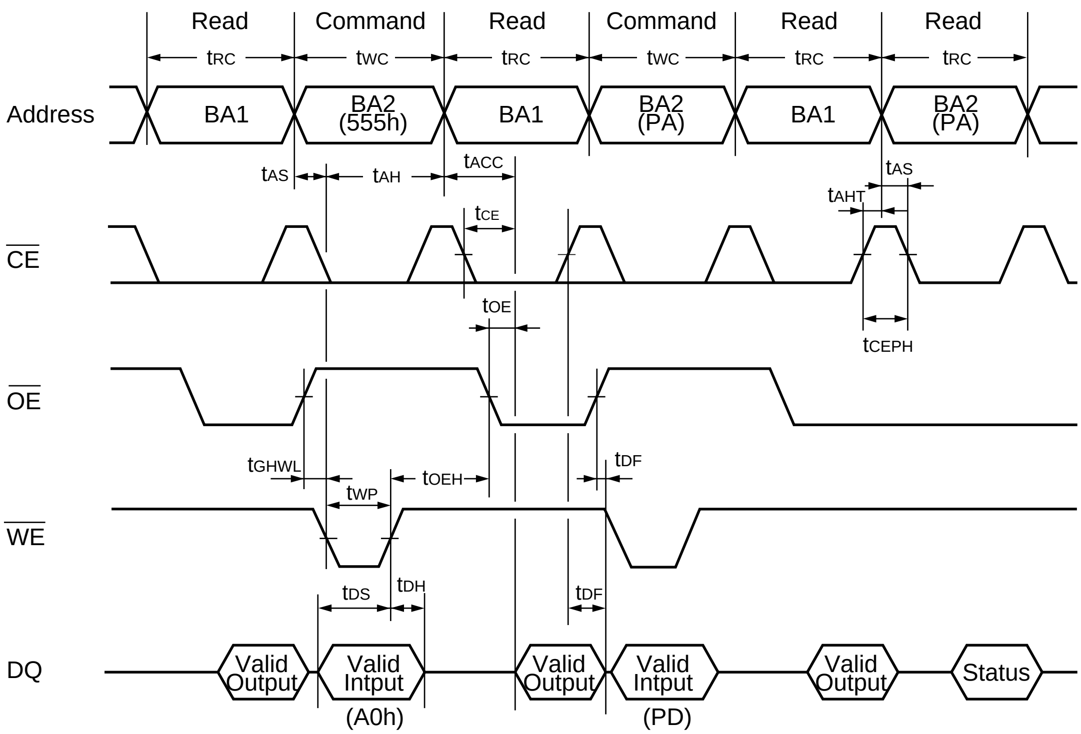
* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

Data Polling during Embedded Algorithm Operation Timing Diagram



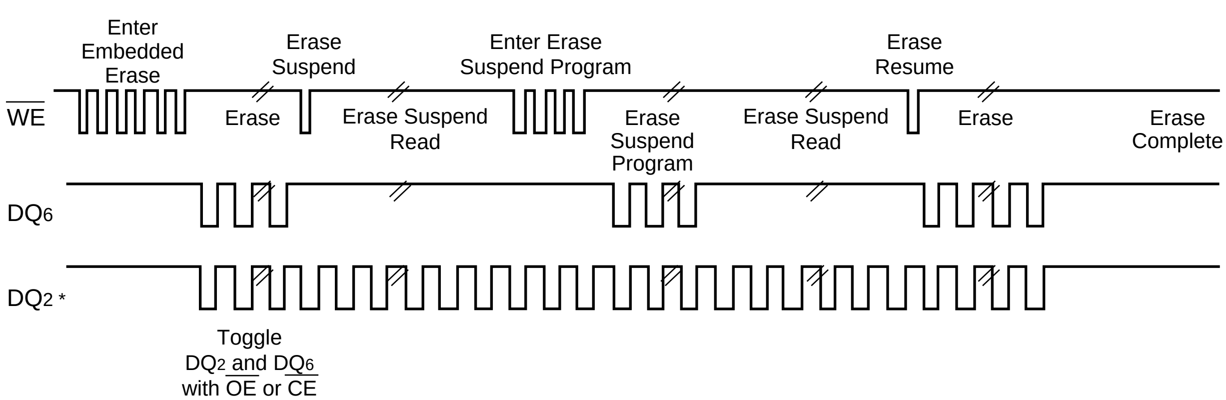
*: DQ6 stops toggling (The device has completed the Embedded operation.)

AC Waveforms for Toggle Bit I during Embedded Algorithm Operations



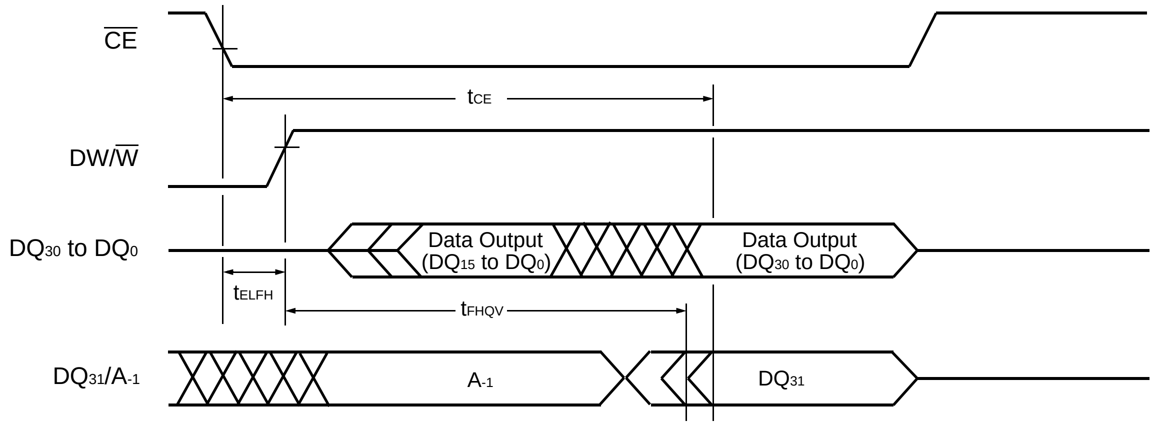
Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1 : Address corresponding to Bank 1
BA2 : Address corresponding to Bank 2

Bank-to-Bank Read / Write(Program and Erase) Timing Diagram

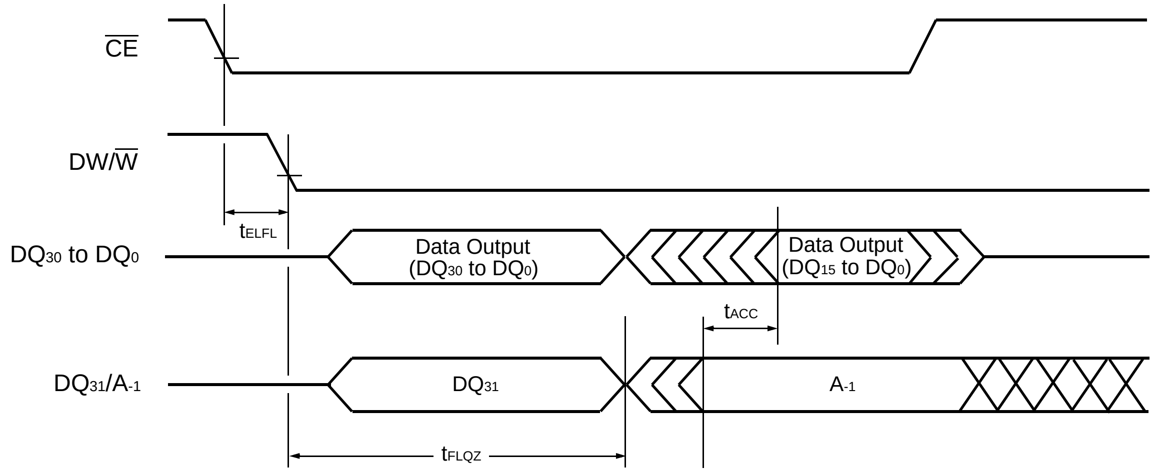


* : DQ_2 is read from the erase-suspended sector.

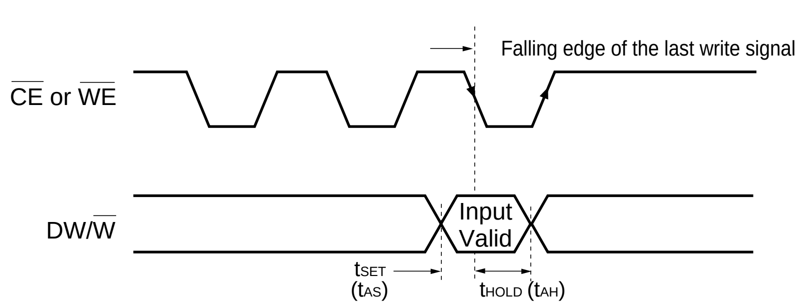
DQ_2 vs. DQ_6



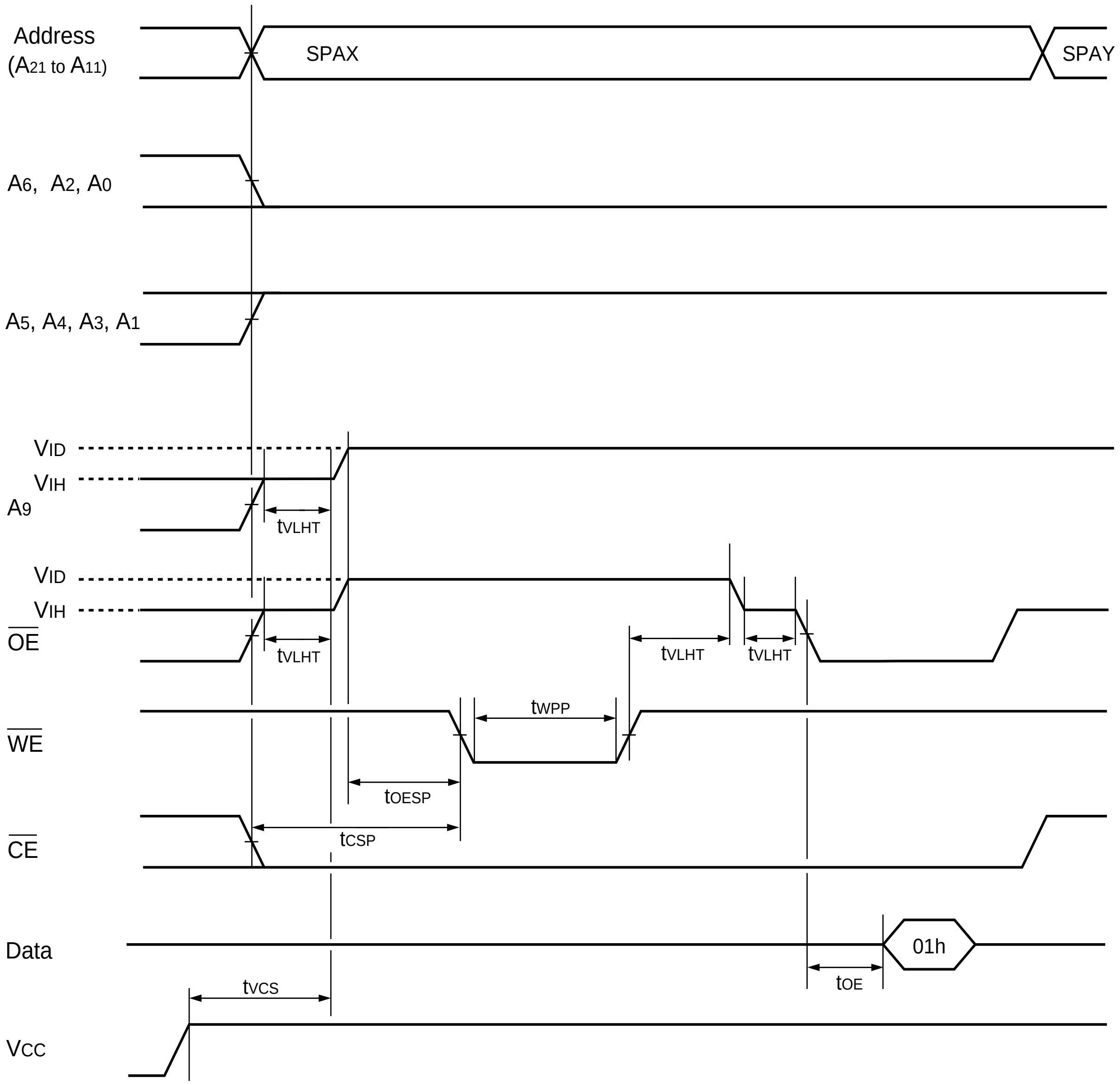
Double Word Mode Configuration Timing Diagram



Word Mode Configuration Timing Diagram



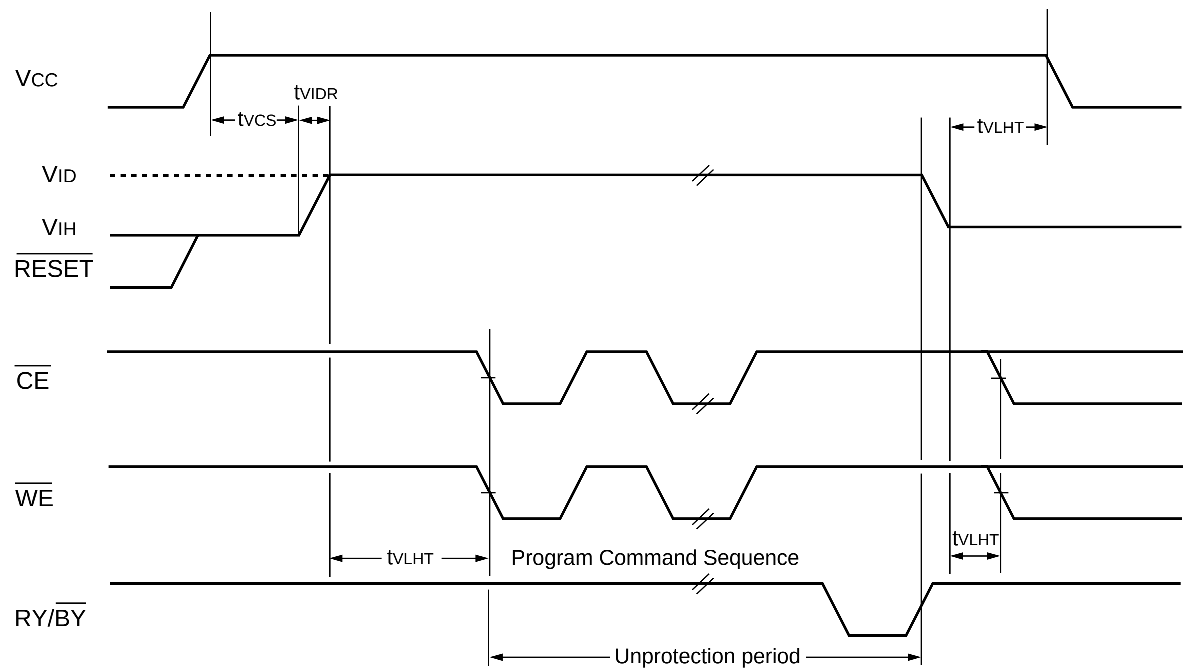
DW/W Timing Diagram for Write Operations



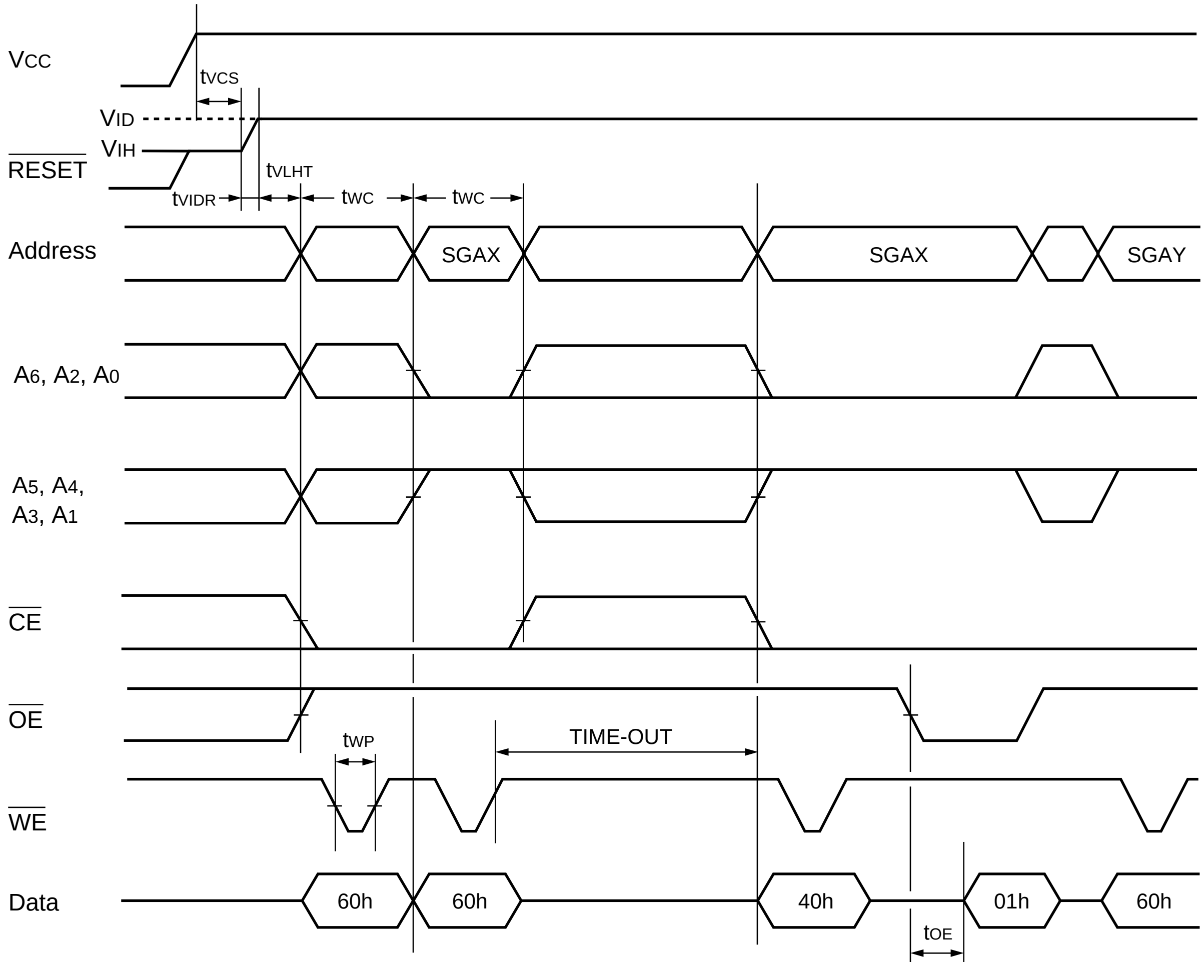
SPAX : Sector Group Address to be protected
SPAY : Next Sector Group Address to be protected

Note : A_{-1} is V_{IL} in word mode.

Sector Group Protection Timing Diagram

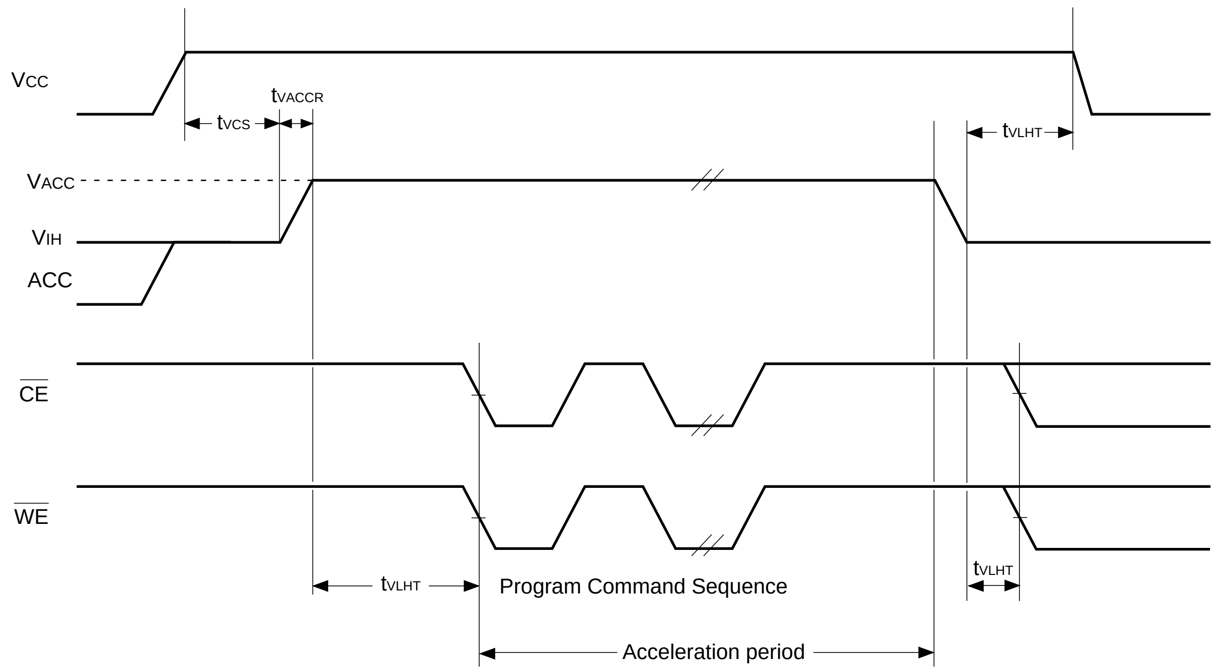


Temporary Sector Group Unprotection Timing Diagram



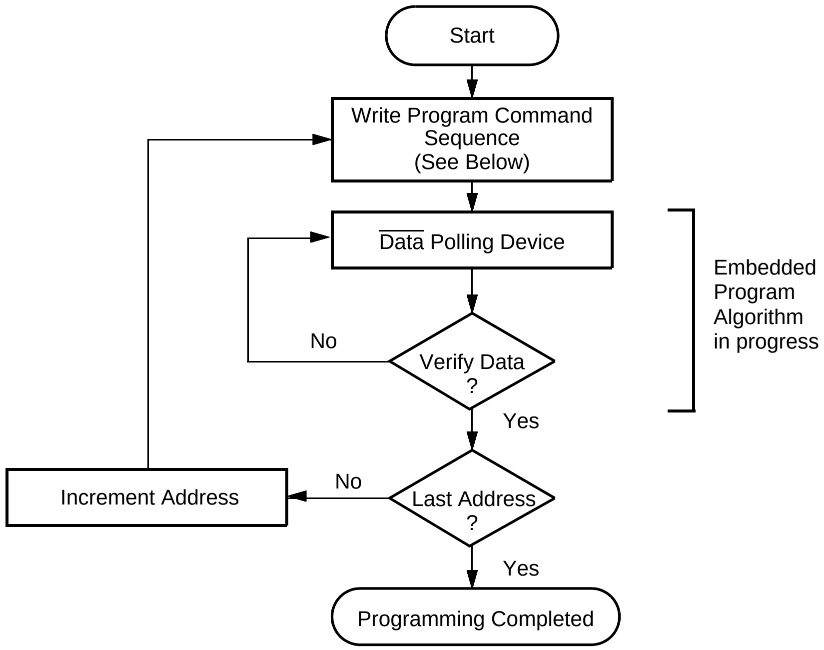
SGAX : Sector Group Address to be protected
SGAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 250 µs (Min)

Extended Sector Group Protection Timing Diagram

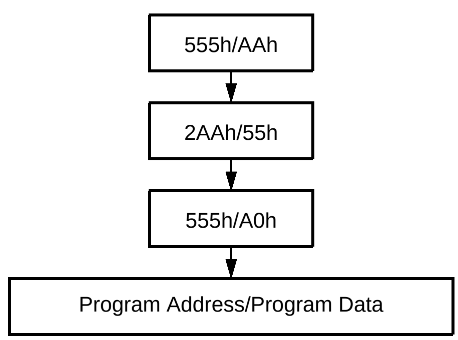


Accelerated Program Timing Diagram

EMBEDDED ALGORITHM



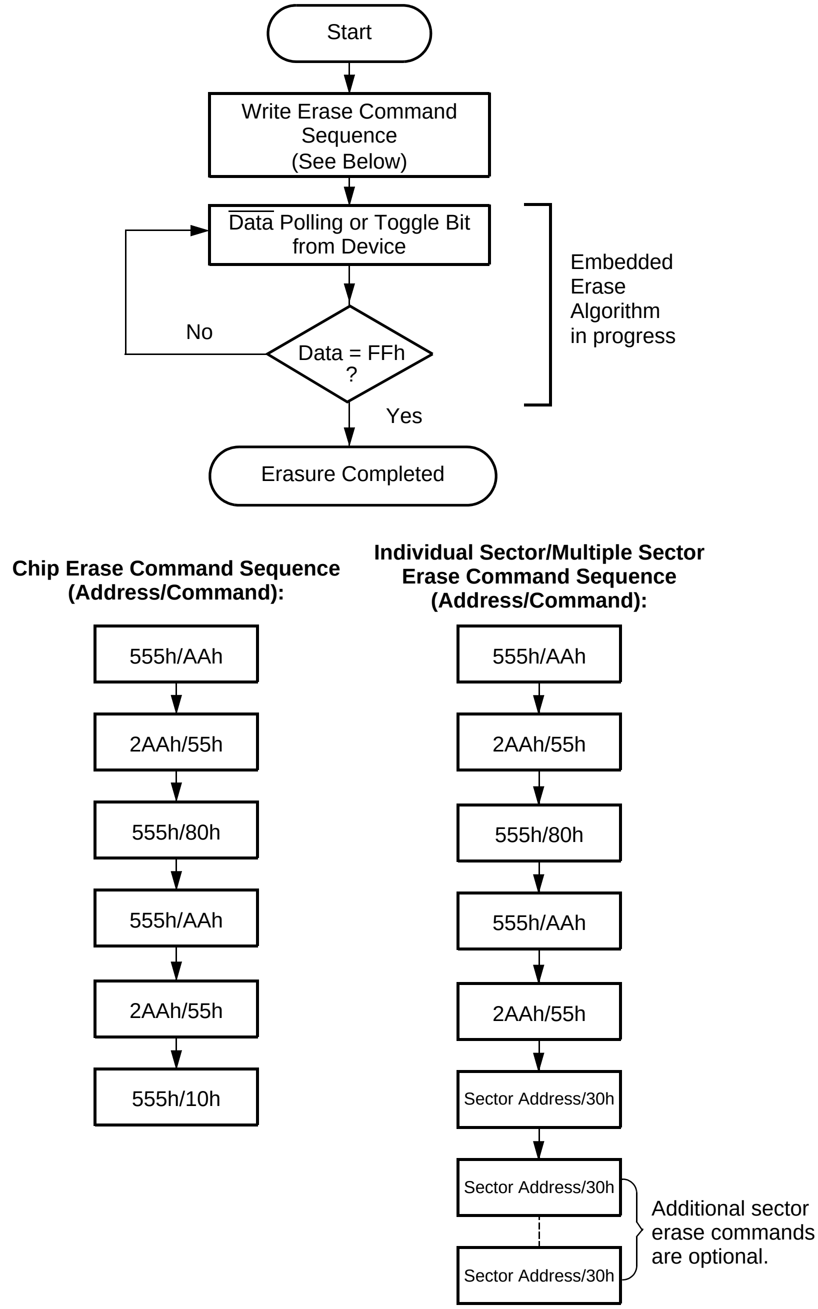
Program Command Sequence (Address/Command):



Notes : • The sequence is applied for ×32 mode.
• The addresses differ from ×16 mode.

Embedded Program™ Algorithm

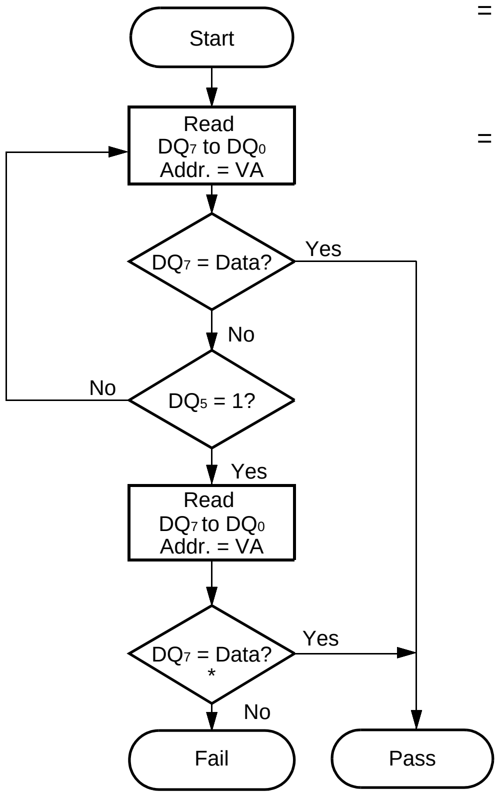
EMBEDDED ALGORITHM



Note : The sequence is applied for ×32 mode.
The addresses differ from ×16 mode.

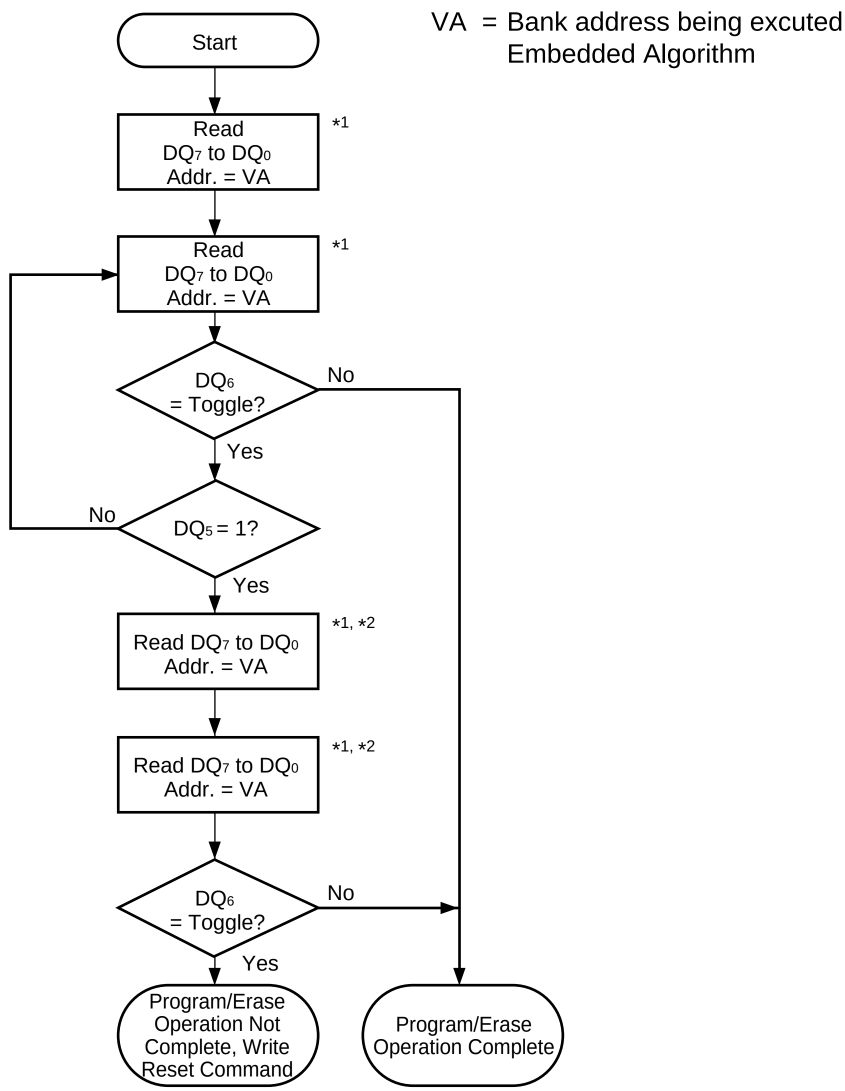
Embedded Erase™ Algorithm

VA = Address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple sector erase operation.
= Any of the sector addresses within the sector not being protected during chip erase operation.



* : DQ_7 is rechecked even if DQ_5 = “1” because DQ_7 may change simultaneously with DQ_5.

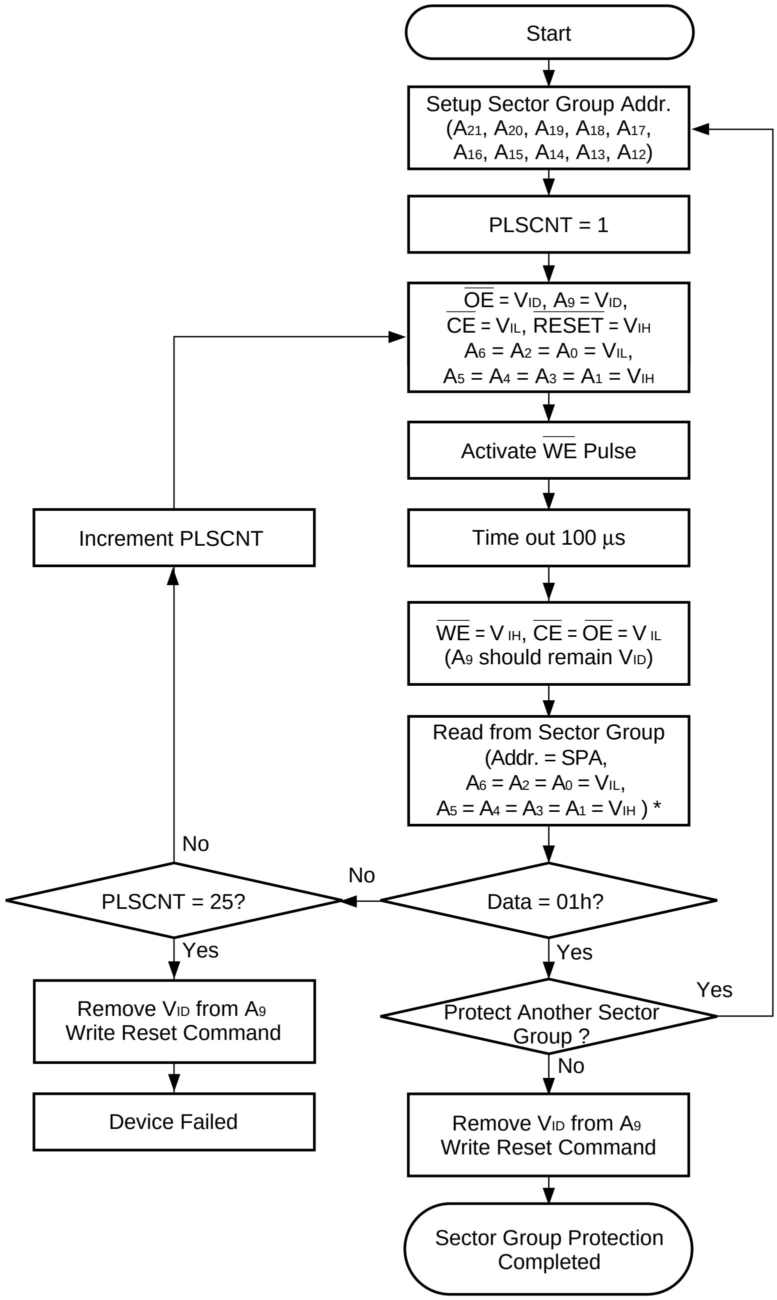
$\overline{\text{Data}}$ Polling Algorithm



*1 : Read toggle bit twice to determine whether it is toggling.

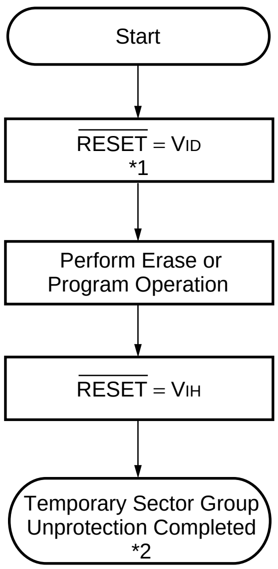
*2 : Recheck toggle bit because it may stop toggling as DQ_5 changes to “1”.

Toggle Bit Algorithm



* : A_{-1} is V_{IL} in word mode.

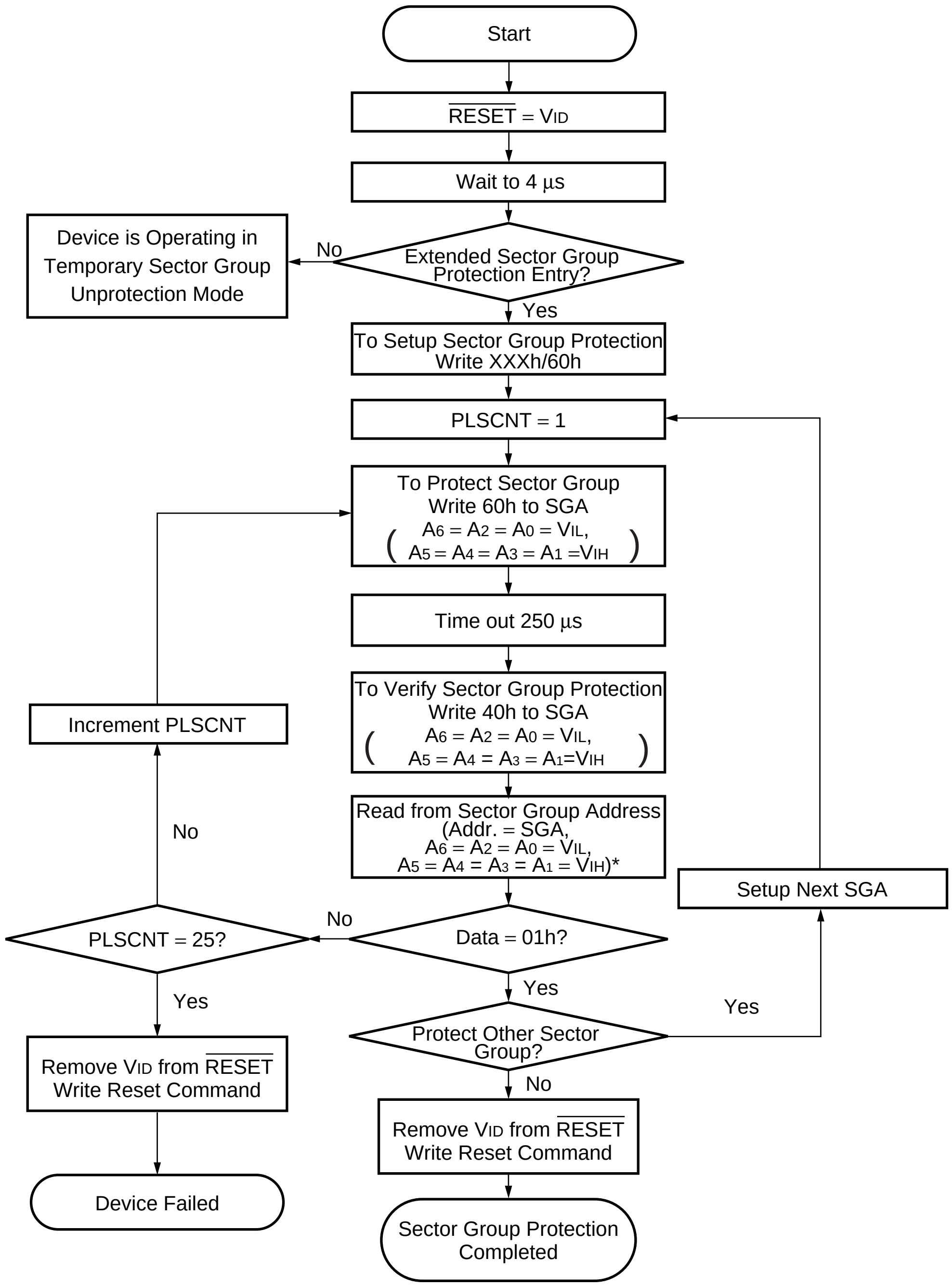
Sector Group Protection Algorithm



*1 : All protected sector groups are unprotected.

*2 : All previously protected sector groups are reprotected once again.

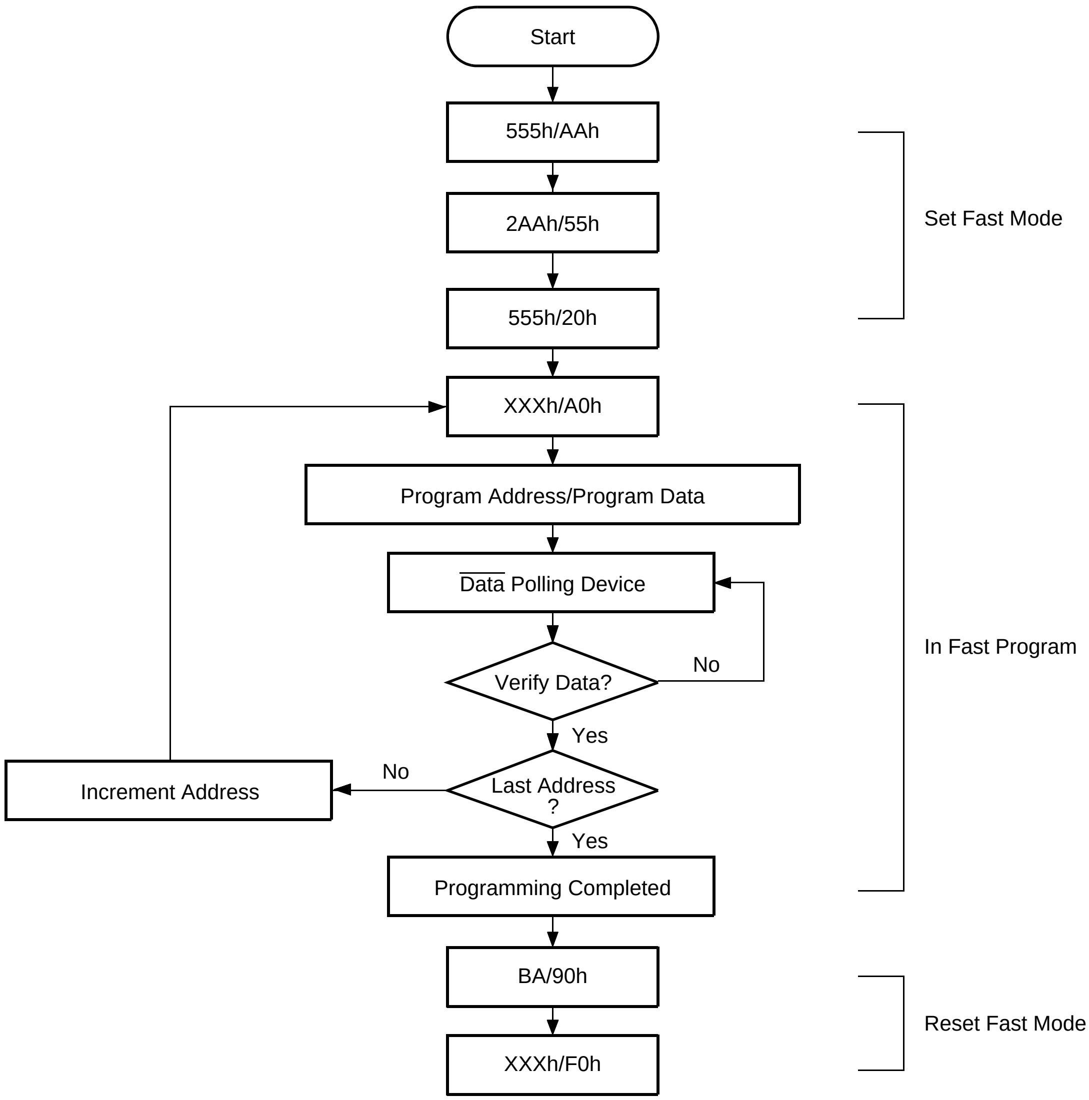
Temporary Sector Group Unprotection Algorithm



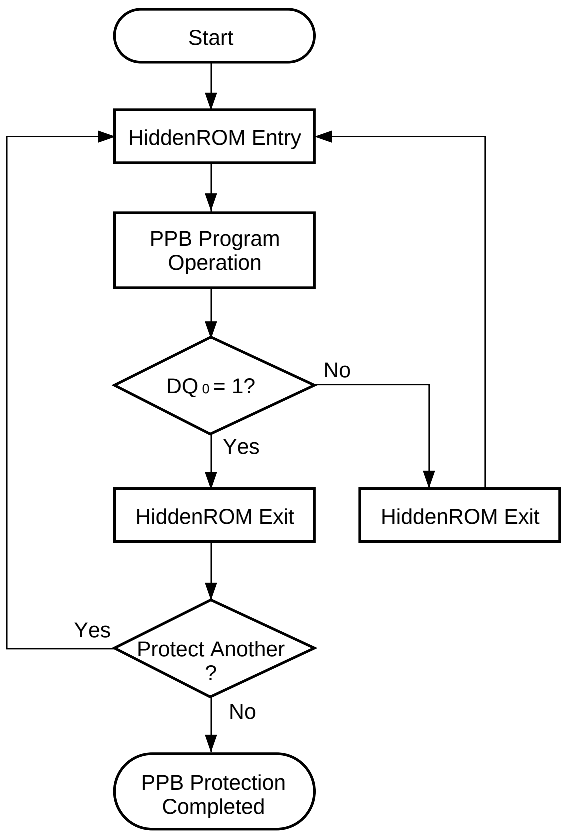
* : A_{-1} is V_{IL} in word mode.

Extended Sector Group Protection Algorithm

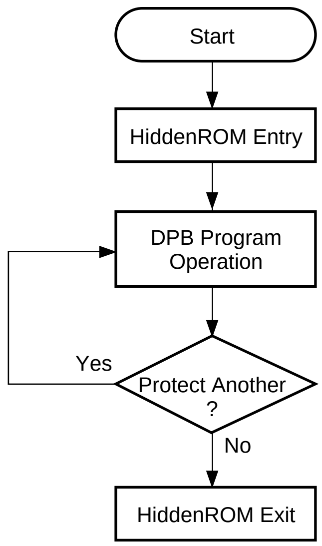
FAST MODE ALGORITHM



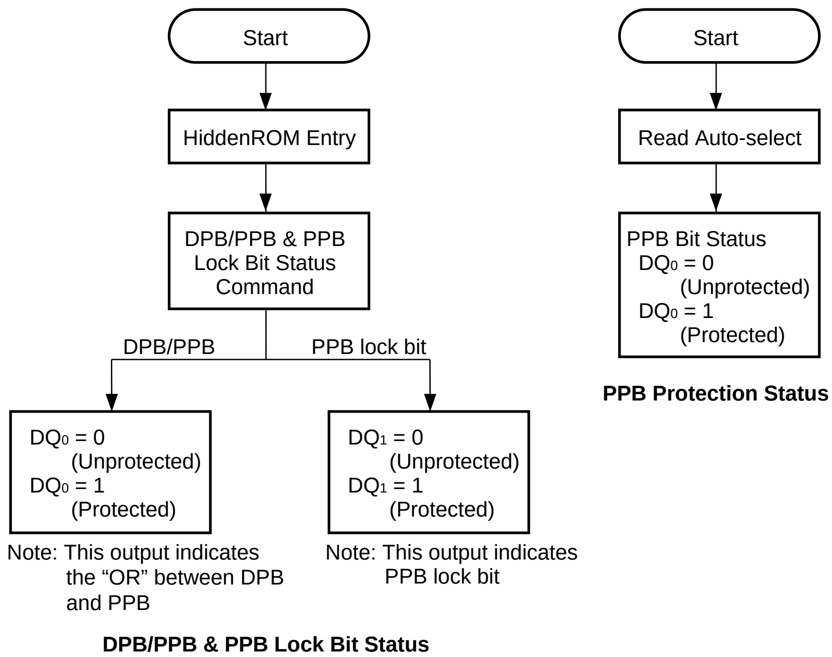
Embedded Program Algorithm for Fast Mode



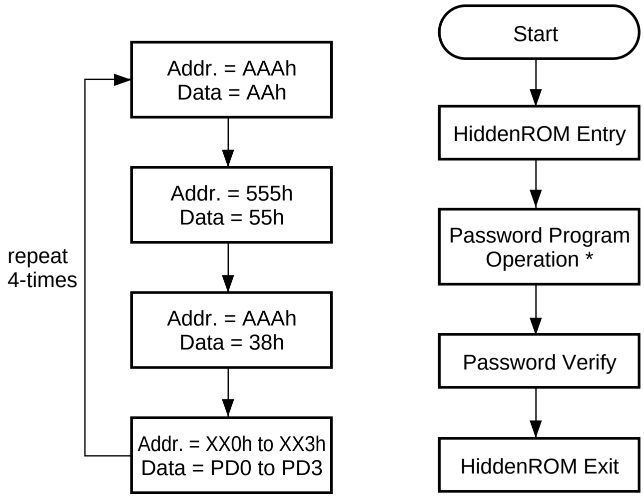
PPB Protection Algorithm



DPB Protection Algorithm



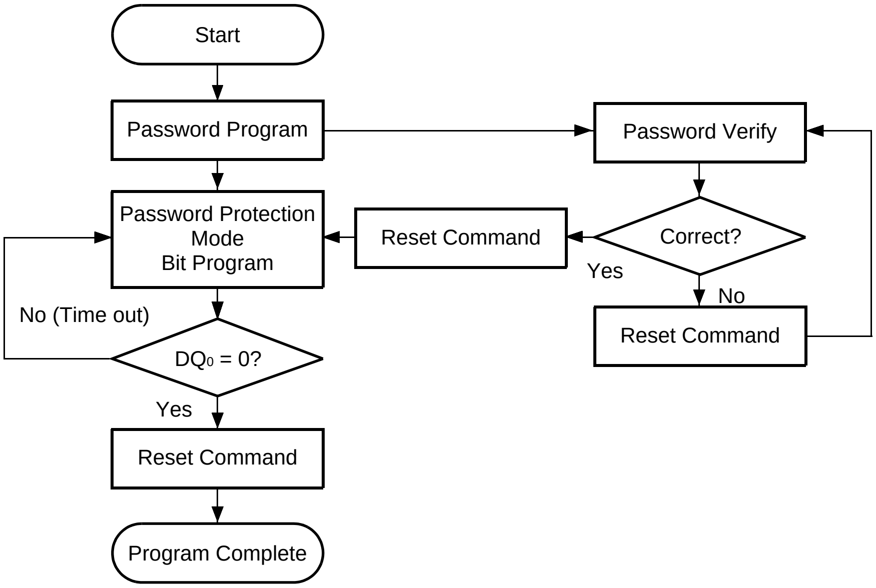
Protection Status



* : Password Program (word mode)

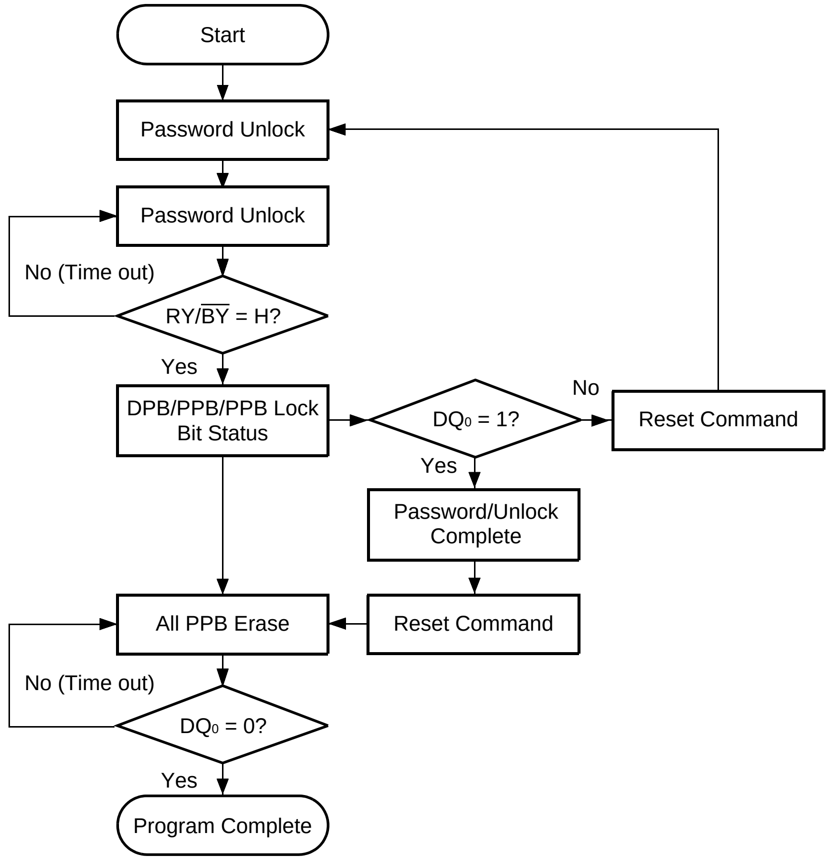
Password Mode Set

Password Mode Choice Method



Password Sector Protect Algorithm

PPB Lock Clear in Password Mode



PPB Lock Bit Clear in Password Mode

■ ORDERING INFORMATION

MBM29XL12D F 70 PFV

PACKAGE TYPE
PFV = 90-pin Shrink Outline L-leaded Package (SSOP)
PBT = 96-ball Fine Pitch Ball Grid Array Package (FBGA)

SPEED OPTION
See "Product Selector Guide".

DEVICE REVISION

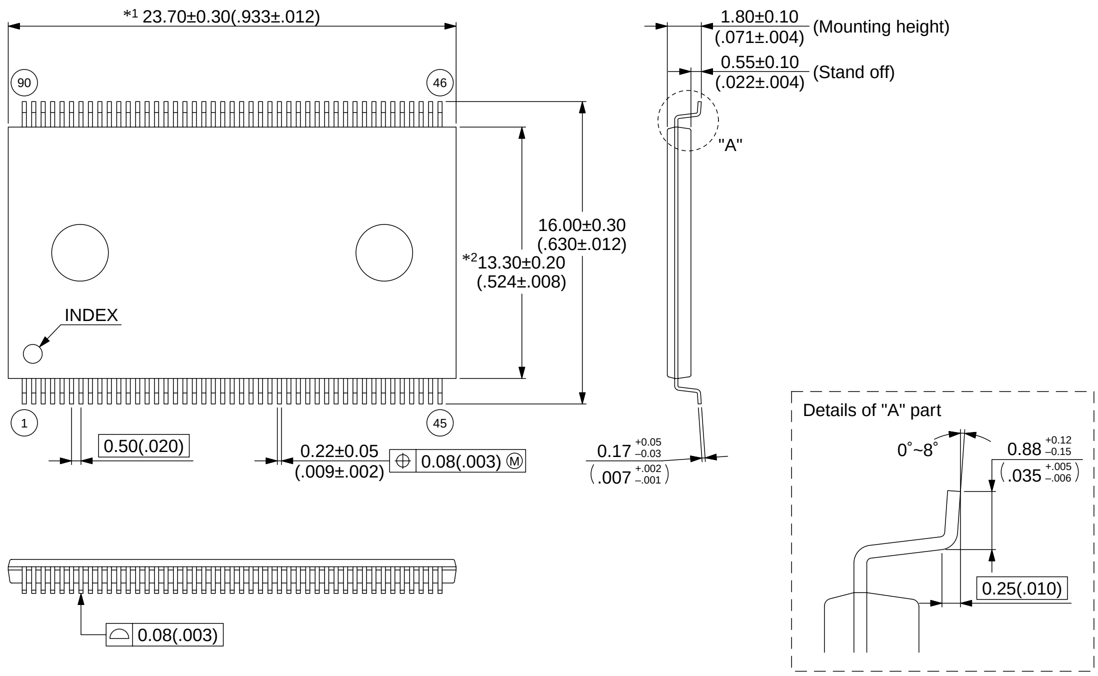
DEVICE NUMBER/DESCRIPTION
MBM29XL12D
128 Mega-bit (8M × 16-Bit or 4M × 32-Bit) Page Mode Flash Memory
3.0 V-only Read, Program, and Erase

Part Number	Package	Access Time (ns)	Remarks
MBM29XL12DF 70PFV MBM29XL12DF 80PFV	90-pin plastic SSOP (FPT-90P-M01)	70 80	
MBM29XL12DF 70PBT MBM29XL12DF 80PBT	96-ball plastic FBGA (BGA-96P-M02)	70 80	

■ PACKAGE DIMENSIONS

90-pin plastic SSOP
(FPT-90P-M01)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.

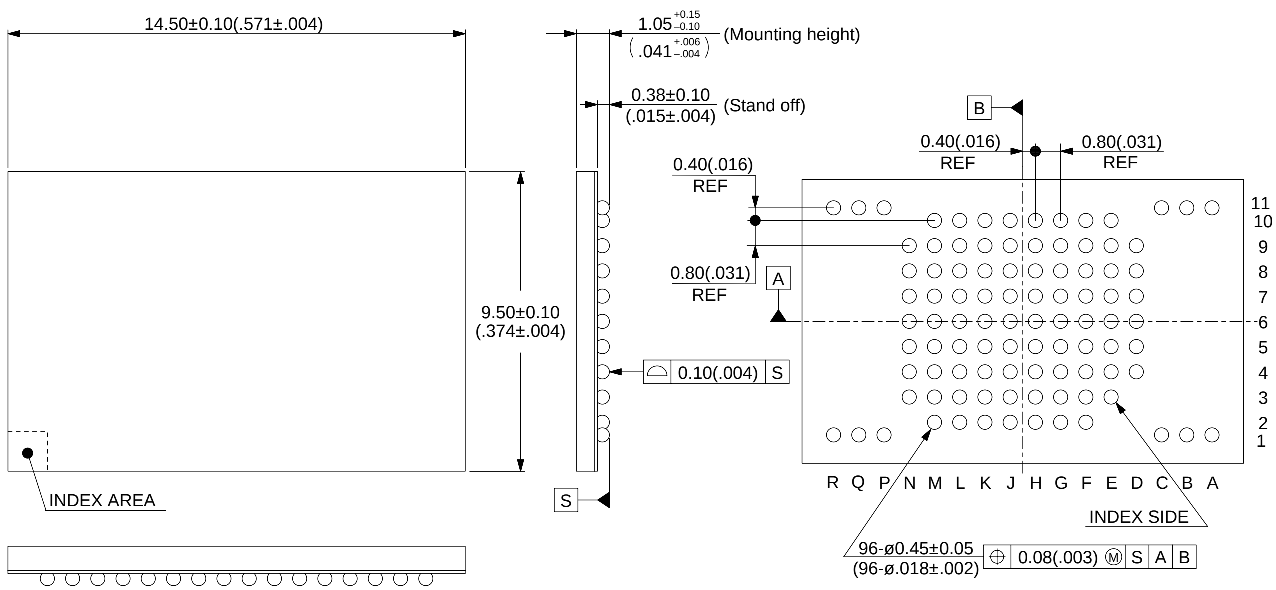


Dimensions in mm (inches)
Note : The values in parentheses are reference values.

(Continued)

(Continued)

96-ball plastic FBGA
(BGA-96P-M02)



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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