

2N718A, 2N1613, 2N1613L



NPN Low Power Silicon Transistor

Rev. V1

Features

- Available in JAN, JANTX and JANTXV per MIL-PRF-19500/181
- Available in TO-18 (2N718A), TO-39 (2N1613) and TO-5 (2N1613L) packages
- Designed for Small Signal General Purpose Switching Applications.



Electrical Characteristics ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Breakdown Voltage, Collector - Emitter	$I_C = 100 \mu\text{A dc}$	$V_{(BR)CEO}$	V dc	30	—
Collector - Base Cutoff Current	$V_{CBO} = 75 \text{ V dc}$	I_{CBO1}	$\mu\text{A dc}$	—	10
Emitter - Base Cutoff Current	$V_{EBO} = 7.0 \text{ V dc}$	I_{EBO1}	$\mu\text{A dc}$	—	10
Collector-Emitter Breakdown Voltage	$I_C = 100 \mu\text{A dc}; R_{BE} = 10 \Omega$	$V_{(BR)CER}$	V dc	50	—
Emitter - Base Cutoff Current	$V_{EB} = 5.0 \text{ V dc}$	I_{EBO2}	nA dc	—	10
Collector - Base Cutoff Current	$V_{CB} = 60 \text{ V dc}$	I_{CBO2}	nA dc	—	10
Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V dc}; I_C = 0.1 \text{ mA dc}$	h_{FE1}		20	
	$V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc}$	h_{FE2}		35	
	$V_{CE} = 10 \text{ V dc}; I_C = 150 \text{ mA dc}$	h_{FE3}		40	120
	$V_{CE} = 10 \text{ V dc}; I_C = 500 \text{ mA dc}$	h_{FE3}		20	
Collector-Emitter Saturated Voltage	$I_C = 150 \text{ mA dc}; I_B = 15 \text{ mA dc}$	$V_{CE(SAT)}$	V dc	—	1.5
Base-Emitter Saturated Voltage	$I_C = 150 \text{ mA dc}; I_B = 15 \text{ mA dc}$	$V_{BE(SAT)}$	V dc	—	1.3

2N718A, 2N1613, 2N1613L



NPN Low Power Silicon Transistor

Rev. V1

Electrical Characteristics (+25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Base Cutoff Current	$T_A = +150^\circ\text{C}$ $V_{CB} = 60\text{ V dc}$	I_{CBO3}	$\mu\text{A dc}$	—	10
Forward-Current Transfer Ratio	$T_A = -55^\circ\text{C}$ $V_{CE} = 10\text{ V dc}; I_C = 10\text{ mA dc}$	h_{FE5}		20	
Dynamic Characteristics					
Small-Signal Short-Circuit Forward Current Transfer Ratio	$V_{CE} = 5\text{ V dc}; I_C = 1\text{ mA dc}; f = 1\text{ kHz}$ $V_{CE} = 10\text{ V dc}; I_C = 5\text{ mA dc}; f = 1\text{ kHz}$	h_{fe}		30 35	100 150
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio	$V_{CE} = 10\text{ V dc}; I_C = 50\text{ mA dc}; f = 20\text{ MHz}$	$ h_{FE} $		3	
Open Circuit Output Capacitance	$V_{CB} = 10\text{ V dc}; I_E = 0;$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$	C_{obo}	pF		25
Small-Signal Short-Circuit Input Impedance	$V_{CB} = 10\text{ V dc}; I_C = 5\text{ mA dc}; f = 1\text{ kHz}$	h_{ib}	ohms	4	8
Small-Signal Open-Circuit Output Admittance	$V_{CB} = 10\text{ V dc}; I_C = 5\text{ mA dc}; f = 1\text{ kHz}$	h_{ob}	μohms	0	1.0
Small-Signal Open-Circuit Reverse Voltage Transfer Ratio	$V_{CB} = 10\text{ V dc}; I_C = 5\text{ mA dc}; f = 1\text{ kHz}$	h_{rb}			3×10^{-4}
Pulse Response	Test Condition A , except test circuit and pulse requirements. See figure 5 of MIL-PRF-19500	$t_{on} + t_{off}$	ns		30

2N718A, 2N1613, 2N1613L



NPN Low Power Silicon Transistor

Rev. V1

Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage	V_{CEO}	30 V dc
Collector - Base Voltage	V_{CBO}	75 V dc
Emitter - Base Voltage	V_{EBO}	7 V dc
Collector Current	I_C	500 mA dc
Collector - Emitter Voltage ($R_{BE} = 10\Omega$)	V_{CER}	50 V dc
Operating & Storage Temperature Range	T_J, T_{STG}	-65°C to $+200^\circ\text{C}$
$T_C = +25^\circ\text{C}$ 2N718A 2N1613 2N1613L	$P_T^{(1)}$	1.8 W 3.0 W 3.0 W
$T_A = +25^\circ\text{C}$ 2N718A 2N1613 2N1613L	$P_{T2}^{(2)}$	0.5 W 0.8 W 0.8 W
Thermal Resistance, Junction to Case 2N718A 2N1613 2N1613L	$R_{\theta JC}$	97°C/W 58°C/W 58°C/W
Thermal Resistance, Junction to Ambient 2N718A 2N1613 2N1613L	$R_{\theta JA}$	325°C/W 175°C/W 175°C/W

- (1) Derate linearly at 17.2 mW/°C for type 2N1613 and 2N1613L and at 10.3 mW/°C for type 2N718A for $T_C > +25^\circ\text{C}$.
(2) See figures 3 and 4 of MIL-PRF-19500/181

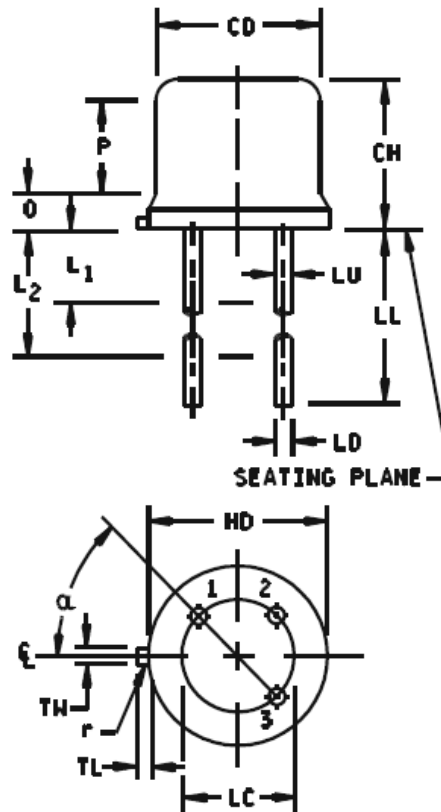
2N718A, 2N1613, 2N1613L

NPN Low Power Silicon Transistor

Rev. V1

Outline Drawing (TO-18)

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		5
LD	.016	.021	0.41	0.53	8, 9
LL	.500	.750	12.70	19.05	7, 9
LU	.016	.019	0.41	0.48	4, 8, 9
L1		.050		1.27	9
L2	.250		6.35		9
TL	.028	.048	0.71	1.22	5
TW	.036	.046	.91	1.17	
P	.100		2.54		3
Q		.030		0.76	6
r		.010		.025	
α	45° TP		45° TP		



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010 inch (0.254 mm).
4. (Three leads) LU applies between L_1 and L_2 . LD applies between L_2 and .5 inch (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond .5 inch (12.70 mm) from seating plane.
5. Measured from maximum diameter of the actual device.
6. Details of outline in this zone optional.
7. The collector shall be electrically connected to the case.
8. Lead number 1 - emitter; lead number 2 - base; lead number 3 - collector.
9. All three leads.
10. In accordance with ANSI Y14.5M, diameters are equivalent to Φx symbology.

FIGURE 1. Physical dimensions 2N718A (TO-18).

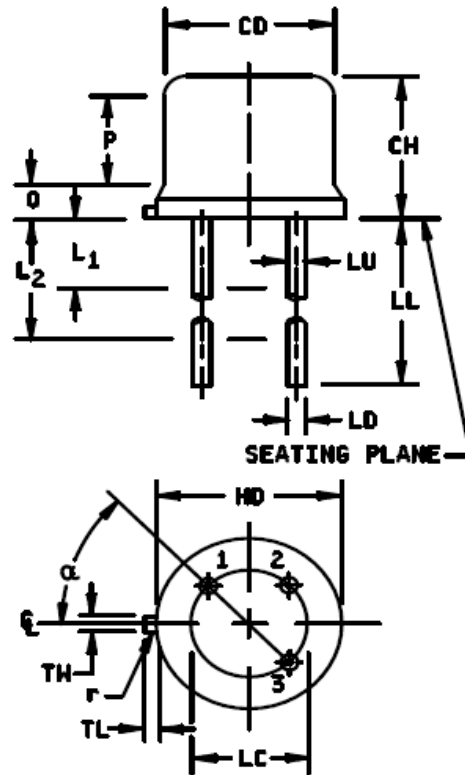
2N718A, 2N1613, 2N1613L

NPN Low Power Silicon Transistor

Rev. V1

Outline Drawing (TO-39, TO-5 Package)

Symbol	Dimensions				Notes
	Inches		Millimeter		
	Min	Max	Min	Max	
CH	.240	.260	6.10	6.60	
LC	.200 TP		5.08 TP		7
LD	.016	.021	0.41	0.53	8,9
LL	See notes 12, and 13				
LU	.016	.019	0.41	0.48	8,9
L ₁		.050		1.27	8,9
L ₂	.250		6.35		8,9
HD	.335	.370	8.51	9.40	
CD	.305	.335	7.75	8.51	
P	.100		2.54		6
Q		.050		1.27	5
r		.010		0.25	
TL	.029	.045	0.74	1.14	4
TW	.028	.034	0.71	0.86	0.71
α	45° TP		45° TP		7



NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of 0.011 inch (0.28 mm).
4. TL measured from maximum HD.
5. Outline in this zone is not controlled.
6. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001, -.000 inch (1.37 +0.03, -0.000 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at a maximum material condition (MMC) relative to the tab at MMC. The device may be measured by direct methods or by the gauging procedure.
8. LU applies between L₁ and L₂. LU applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
9. All three leads.
10. The collector shall be electrically and mechanically connected to the case.
11. r (radius) applies to both inside corners of tab.
12. For transistor types 2N1613, dimension LL is .500 inch (12.70 mm) minimum, and .750 inch (19.05 mm) maximum.
13. For transistor types 2N1613L, dimension LL is 1.500 inches (38.10 mm) minimum, and 1.750 inches (44.45 mm) maximum.
14. Lead number 1 - emitter; lead number 2 - base; lead number 3 - collector.

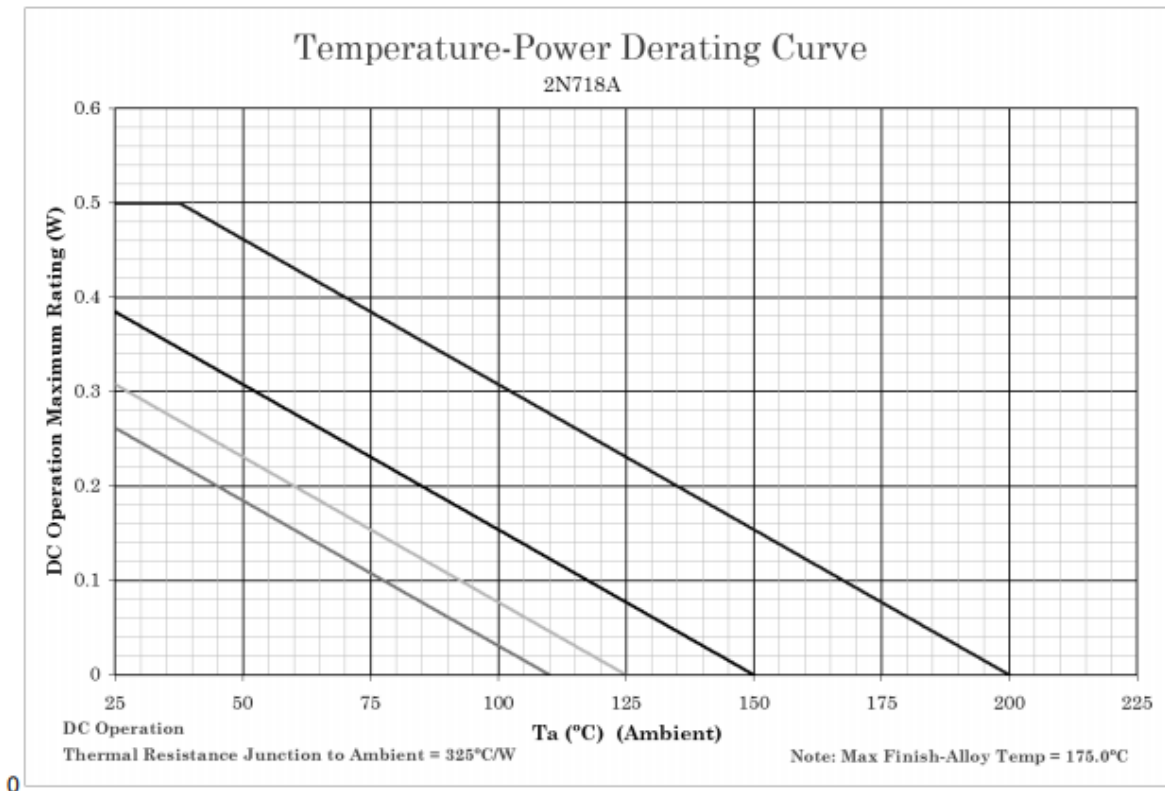
FIGURE 2. Physical dimensions 2N1613 and 2N1613L (similar to TO-5 and TO-39).

2N718A, 2N1613, 2N1613L

NPN Low Power Silicon Transistor

Rev. V1

Temperature-Power Derating Curve (2N718A)



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 3. Temperature-power derating for 2N718A (TO-18 package).

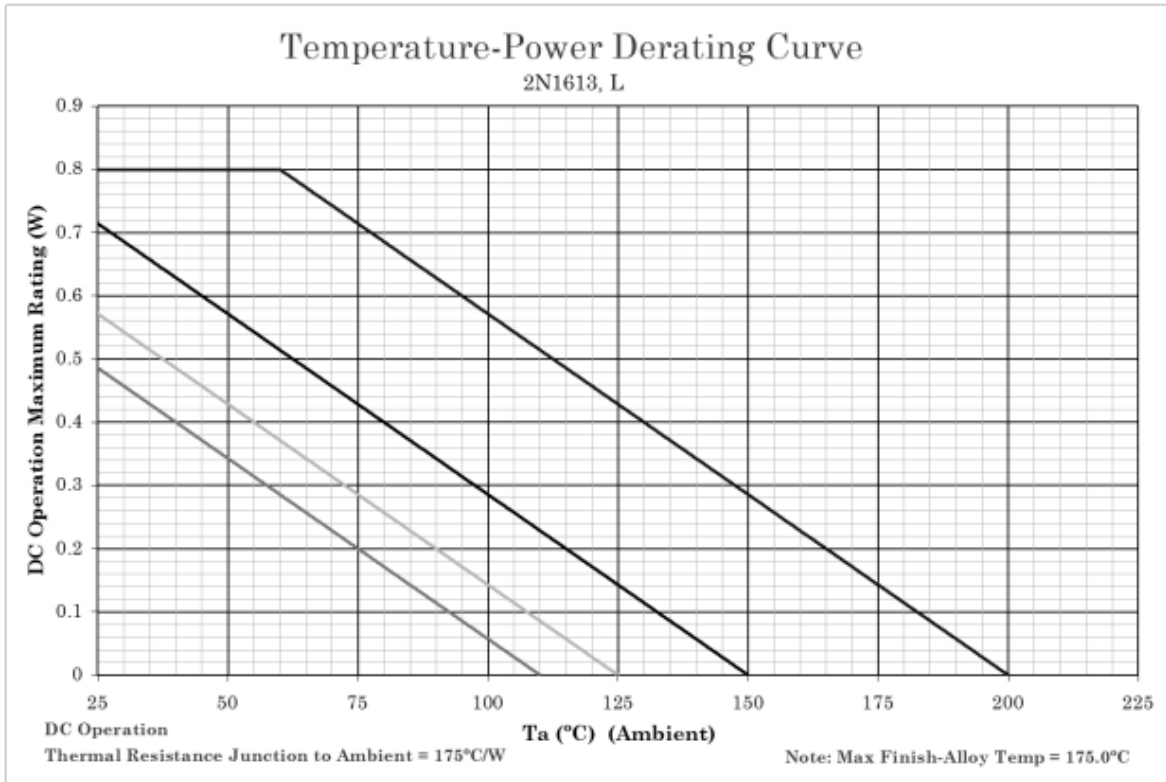
2N718A, 2N1613, 2N1613L



NPN Low Power Silicon Transistor

Rev. V1

Temperature-Power Derating Curve (2N1613, 2N1613L)



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 4. Temperature-power derating for 2N1613 and 2N1613L (TO-5 and TO-39 package).

2N718A, 2N1613, 2N1613L



NPN Low Power Silicon Transistor

Rev. V1

VPT COMPONENTS. ALL RIGHTS RESERVED.

Information in this document is provided in connection with VPT Components products. These materials are provided by VPT Components as a service to its customers and may be used for informational purposes only. Except as provided in VPT Components Terms and Conditions of Sale for such products or in any separate agreement related to this document, VPT Components assumes no liability whatsoever. VPT Components assumes no responsibility for errors or omissions in these materials. VPT Components may make changes to specifications and product descriptions at any time, without notice. VPT Components makes no commitment to update the information and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to its specifications and product descriptions. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document.

THESE MATERIALS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, RELATING TO SALE AND/OR USE OF VPT COMPONENTS PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, CONSEQUENTIAL OR INCIDENTAL DAMAGES, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. VPT COMPONENTS FURTHER DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. VPT COMPONENTS SHALL NOT BE LIABLE FOR ANY SPECIAL, INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS, WHICH MAY RESULT FROM THE USE OF THESE MATERIALS.

VPT Components products are not intended for use in medical, lifesaving or life sustaining applications. VPT Components customers using or selling VPT Components products for use in such applications do so at their own risk and agree to fully indemnify VPT Components for any damages resulting from such improper use or sale.