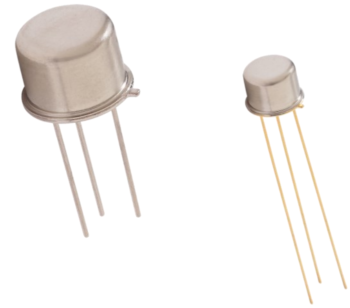
2N1711, 2N1711S
2N1890, 2N1890S

NPN Low Power Silicon Transistor

Rev. V1



Features

- Available in JAN, JANTX and JANTXV per MIL-PRF-19500/225
- TO-5 and TO-39 Packages
- General Purpose Transistors for Low Power Applications
- Ideal for High Performance Low Noise Amplifiers, Oscillators and Switching Circuits

Electrical Characteristics (25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Breakdown Voltage	I_C = 30 mA dc 2N1711, 2N1711S 2N1890, 2N1890S	$V_{(BR)CEO}$	V dc	30 60	—
Collector - Emitter Breakdown Voltage	I_C = 100 mA dc, R_{BE} = 10 Ω 2N1711, 2N1711S 2N1890, 2N1890S	$V_{(BR)CER}$	V dc	50 80	—
Collector - Base Cutoff Current	V_{CB} = 60 V dc 2N1711, 2N1711S V_{CB} = 80 V dc 2N1890, 2N1890S	I_{CBO1}	nA dc	—	10 10
Emitter - Base Cutoff Current	V_{EB} = 5 Vdc	I_{EBO1}	nA dc	—	5.0
Collector - Base Cutoff Current	V_{CB} = 75 V dc 2N1711, 2N1711S V_{CB} = 100 V dc 2N1890, 2N1890S	I_{CBO2}	μA dc	—	100 100
Emitter - Base Cutoff Current	V_{EB} = 7 Vdc	I_{EBO2}	μA dc	—	100
Collector-Emitter Saturation Voltage	I_C = 150 mA dc, I_B = 15 mA dc 2N1711, 2N1711S 2N1890, 2N1890S	$V_{CE(SAT)1}$	V dc	—	1.5 5.0
Collector-Emitter Saturation Voltage	I_C = 50 mA dc, I_B = 5 mA dc, 2N1890, 2N1890S	$V_{CE(SAT)2}$	V dc	—	1.2
Base-Emitter Saturation Voltage	I_C = 150 mA dc, I_B = 15 mA dc 2N1711, 2N1711S 2N1890, 2N1890S	$V_{BE(SAT)1}$	V dc	—	1.3 1.3
Base-Emitter Saturation Voltage	I_C = 50 mA dc, I_B = 5 mA dc 2N1890, 2N1890S	$V_{BE(SAT)2}$	V dc	—	0.9

For further information and support please visit:
info@vptcomponents.com

Electrical Characteristics (25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Forward - Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 10 μA dc V_{CE} = 10 V dc; I_C = 150 mA dc	h_{FE1} h_{FE2}		20 100	300
Forward - Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 500 mA dc 2N1711, 2N1711S	h_{FE3}		50	
Collector Base Cutoff Current	T_A = 150°C V_{CB} = 60 V dc, 2N1711, 2N1711S V_{CB} = 80 V dc, 2N1890, 2N1890S	I_{CBO3}	μA dc	—	10 15
Forward - Current Transfer Ratio	T_A = -55°C V_{CE} = 10 V dc; I_C = 10 mA dc	h_{FE4}		35	
Small-Signal Short-Circuit Forward Current Transfer Ratio	V_{CE} = 5 V dc; I_C = 1 mA dc; f = 1 kHz V_{CE} = 10 V dc; I_C = 5 mA dc; f = 1 kHz	h_{fe1} h_{fe2}		80 90	200 270
Magnitude of Small-Signal Short-Circuit Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 50 mA dc; f = 20 MHz	$\|h_{fe}\|$		3.5	12
Small-Signal Short-Circuit Input Impedance	V_{CB} = 10 V dc; I_C = 5 mA dc; f = 1 kHz	h_{ib}	Ω	4	8
Small-Signal Short-Circuit Input Admittance	V_{CB} = 10 V dc; I_C = 5 mA dc; f = 1 kHz 2N1711, 2N1711S 2N1890, 2N1890S	h_{ob}	μmhos	0.0 0.0	1.0 .3
Small-Signal Open-Circuit Reverse Voltage Transfer Ratio	V_{CB} = 10 V dc; I_C = 5 mA dc; f = 1 kHz 2N1711, 2N1711S 2N1890, 2N1890S	h_{rb}	μmhos		$5x10^{-4}$ $1.5x10^{-4}$
Open Circuit Output Capacitance	V_{CB} = 10 V dc; I_E = 0 mA dc; f = 100 kHz$\leq$f$\leq$ 1mHz 2N1711, 2N1711S 2N1890, 2N1890S	C_{obo}	pF	8 5	25 15
Pulse Response	Test condition A, except test circuit and pulse requirements. See figure 6 of MIL=PRF-19500/225	$t_{on} + t_{off}$	ns		30

Absolute Maximum Ratings (25°C unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage 2N1711, 2N1711S 2N1890, 2N1890S	V_{CEO}	 30 V dc 60 V dc
Collector - Emitter Voltage 2N1711, 2N1711S 2N1890, 2N1890S	V_{CER}	 50 V dc 80 V dc
Collector - Base Voltage 2N1711, 2N1711S 2N1890, 2N1890S	V_{CBO}	 75 V dc 100 V dc
Emitter - Base Voltage	V_{EBO}	7 V dc
Collector Current	I_C	500 mA dc
Total Power Dissipation @ T_C = +25°C @ T_A = +25°C	P_T (2)	 3.0 W 0.8 W
Junction & Storage Temperature Range	T_J, T_{STG}	-65°C to +200°C

Thermal Characteristics (3)

Characteristics	Symbol	Max. Value
Thermal Resistance Junction to Case	$R_{\theta JC}$	30°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	175°C/W

(1) Also applies to the corresponding “S” suffix device.
(2) For derating see figure 2 and figure 3 as shown on pages 5 and 6.
(3) For thermal impedance curves see figure 4 and figure 5 on pages 7 and 8.

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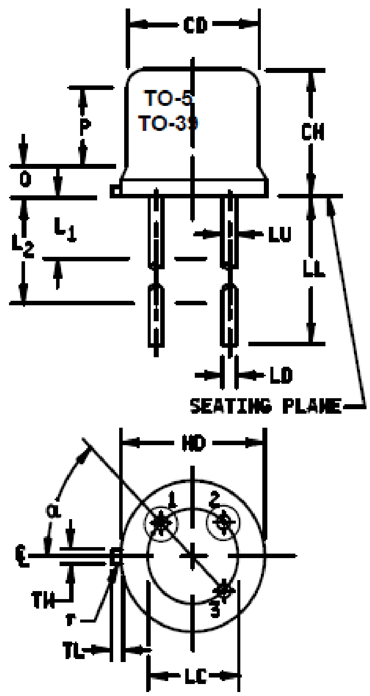
Outline Drawing: TO-5, TO-39 Package Types

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TYP		5.08 TYP		7
LD	.016	.021	0.41	0.53	6
LL	See notes 7, 9, and 10				
LU	.016	.019	0.41	0.48	7
L_1		.050		1.27	7
L_2	.250		6.35		7
P	.100		2.54		5
Q		.050		1.27	
r		.010		0.254	8
TL	.029	.045	0.74	1.14	4
TW	.028	.034	0.71	0.86	3
α	45° TP		45° TP		6
Term 1	Emitter				
Term 2	Base				
Term 3	Collector				

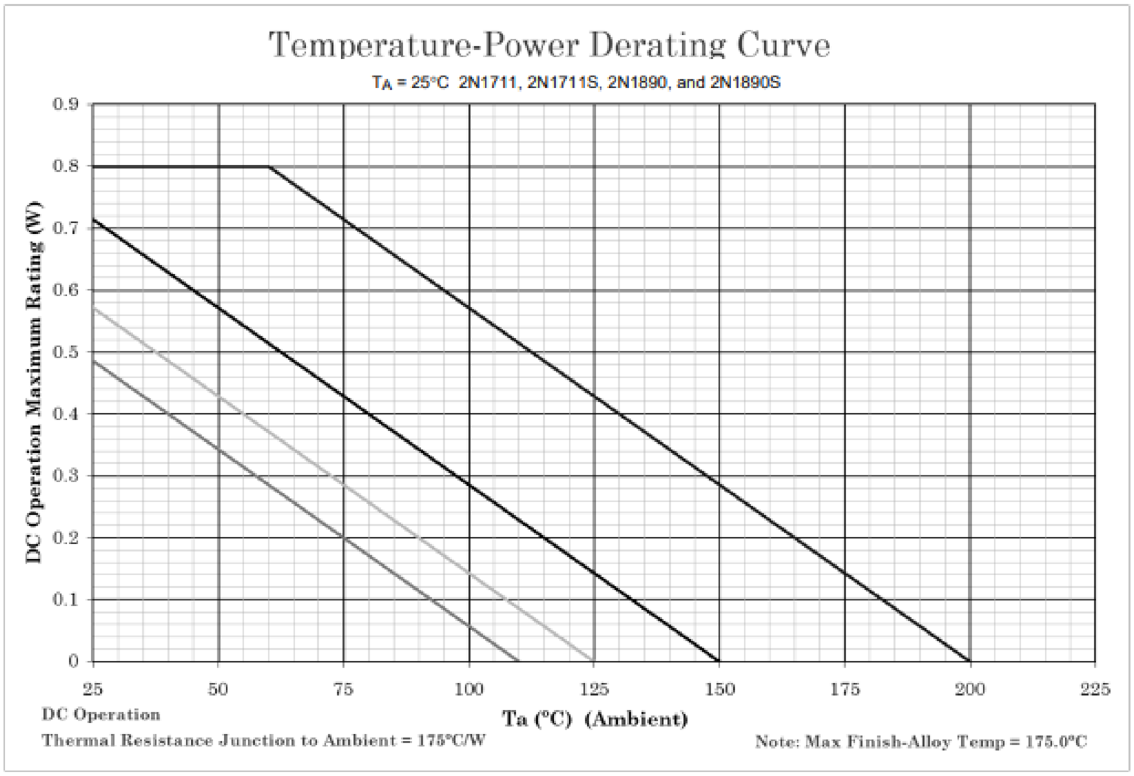


NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r maximum, TW must be held to a minimum length of .021 inch (0.53 mm).
4. TL measured from maximum HD.
5. CD shall not vary more than ±.010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 - .055 inch (1.37 - 1.40 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at a maximum material condition (MMC) relative to the tab at MMC. The device may be measured by direct methods or by gauge and gauging procedure.
7. LU applies between L_1 and L_2. LD applies between L_2 and L minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. r (radius) applies to both inside corners of tab.
9. * For transistor types 2N1711S and 2N1890S, LL is .500 inch (12.70 mm) minimum, and .750 inch (19.05 mm) maximum (TO-39).
10. For transistor types 2N1711 and 2N1890, LL is 1.500 inches (38.10 mm) minimum, and 1.750 inches (44.45 mm) maximum (TO-5).
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 1. Physical dimensions (TO-5 and TO-39).

Temperature-Power Derating Curve

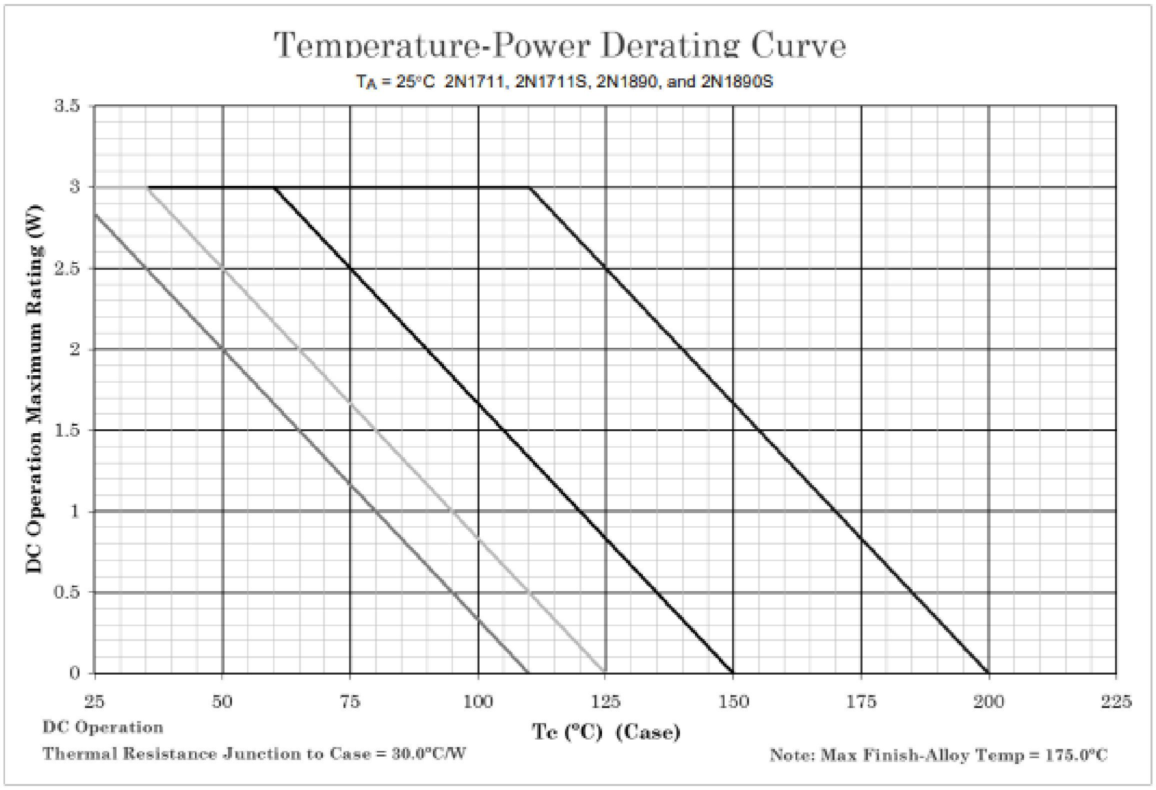


NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 2. Temperature-power derating for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5 and TO-39).

Temperature-Power Derating Curve



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 3. Temperature-power derating for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5 and TO-39).

Thermal Impedance Curves

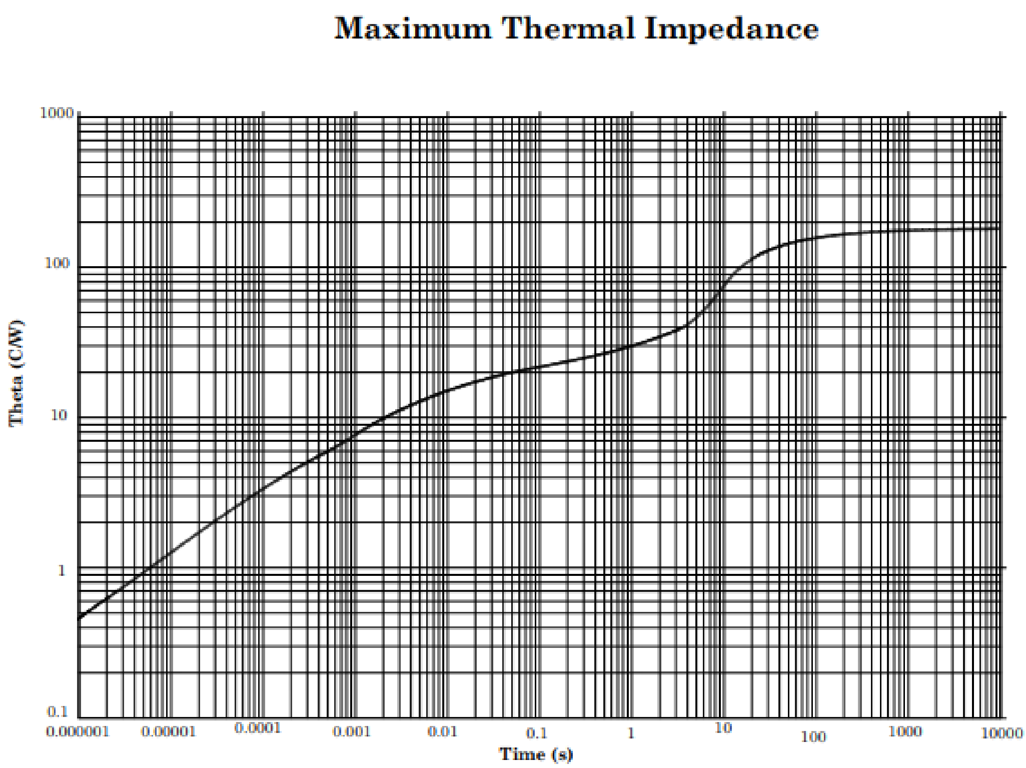


FIGURE 4. Thermal impedance graph ($R_{\theta JA}$) for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5 and TO-39).

Thermal Impedance Curves

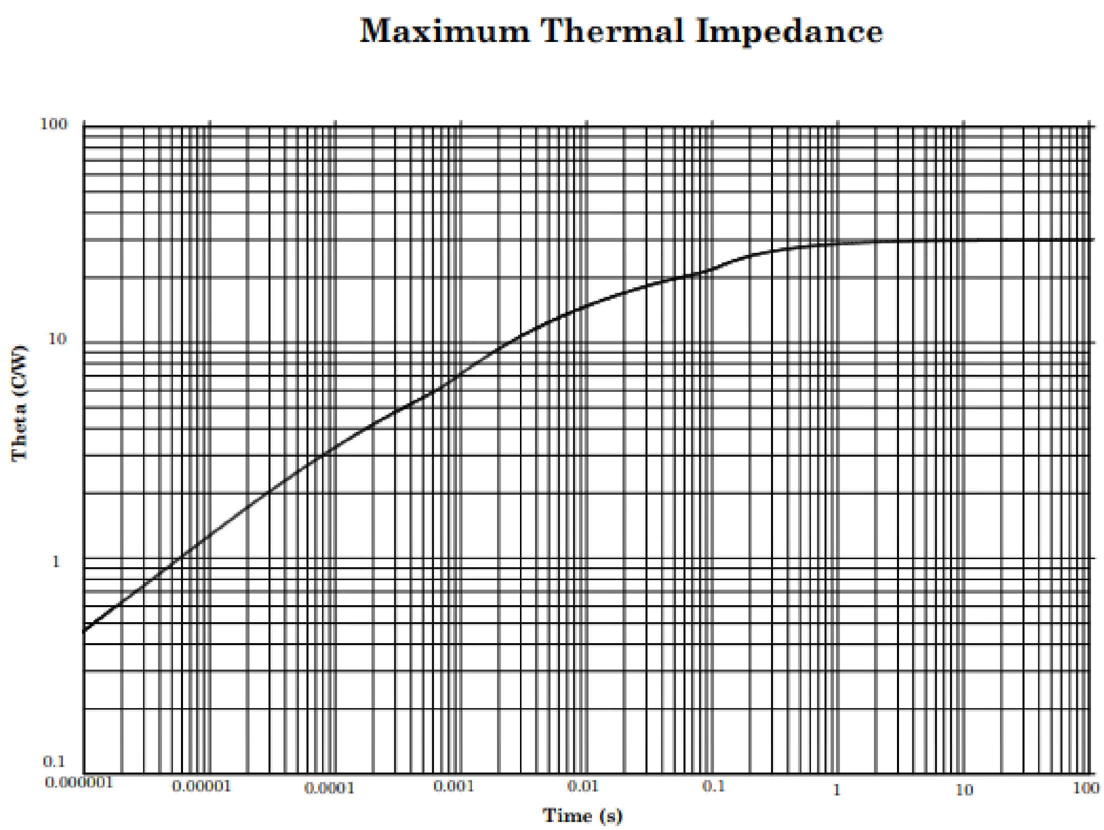


FIGURE 5. Thermal impedance graph ($R_{\theta JC}$) for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5 and TO-39).