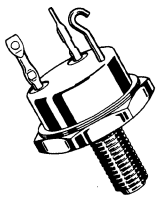
2N1724 (SILICON)
2N1725



CASE 9
(TO-61)

NPN silicon power transistors designed for switching and amplifier applications.

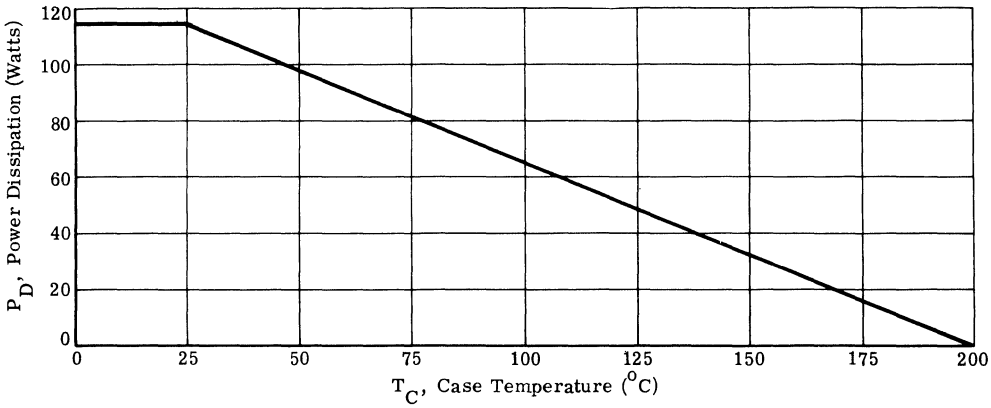
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	120	Vdc
Collector-Emitter Voltage	V_{CE}	80	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current (Continuous)	I_C	5.0	Adc
Power Dissipation	P_D	117	Watts
Thermal Resistance, Junction to Case	θ_{JC}	1.5	$^oC/W$
Junction Operating Temperature Range	T_J	-65 to +200	^oC

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Emitter-Base Cutoff Current		I_{EBO}				mAdc
(V_{EB} = 9 Vdc)	2N1725		-	-	0.5	
(V_{EB} = 10 Vdc)			-	-	10.0	
Collector-Emitter Cutoff Current		I_{CES}				mAdc
(V_{CE} = 60 Vdc, V_{BE} = 0)			-	-	1.0	
(V_{CE} = 60 Vdc, V_{BE} = 0, T_C = 150°C)			-	-	2.0	
(V_{CE} = 120 Vdc, V_{BE} = 0, T_C = 150°C)			-	-	10.0	
Collector-Base Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 3 Vdc, I_E = 0)			-	-	0.1	
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$				Vdc
(I_C = 200 mAdc, I_B = 0)			80	-	-	
DC Current Gain		h_{FE}				
(V_{CE} = 15 Vdc, I_C = 2 Adc)	2N1724		20	40	90	
	2N1725		50	90	150	
(V_{CE} = 15 Vdc, I_C = 2 Adc, T_A = -55°C)	2N1724		12	-	-	
	2N1725		25	-	-	
(V_{CE} = 15 Vdc, I_C = 0.1 Adc)	2N1724		20	-	-	
	2N1725		50	-	-	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2 Adc, I_B = 200 mAdc)				0.5	1.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 2 Adc, I_B = 200 mAdc)				1.2	2.0	
High Frequency Current Gain		h_{fe}				
(V_{CE} = 15 Vdc, I_C = 0.5 Adc, f = 10 MHz)			1.0	1.6	-	
Common Base Output Capacitance		C_{ob}				pF
(V_{CB} = 10 Vdc, f = 0.1 MHz)				260	550	
Switching Times						μs
(I_C = 2 Adc, I_{B1} = $-I_{B2}$ = 0.2 Adc)						
Delay time plus Rise time		$t_d + t_r$	-	0.15	-	
Storage time		t_s	-	1.3	-	
Fall time		t_f		0.14		

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



SAFE OPERATING AREAS

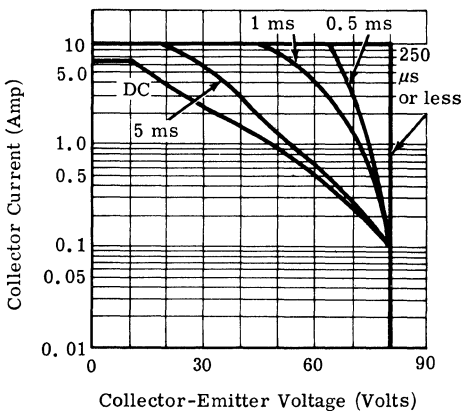
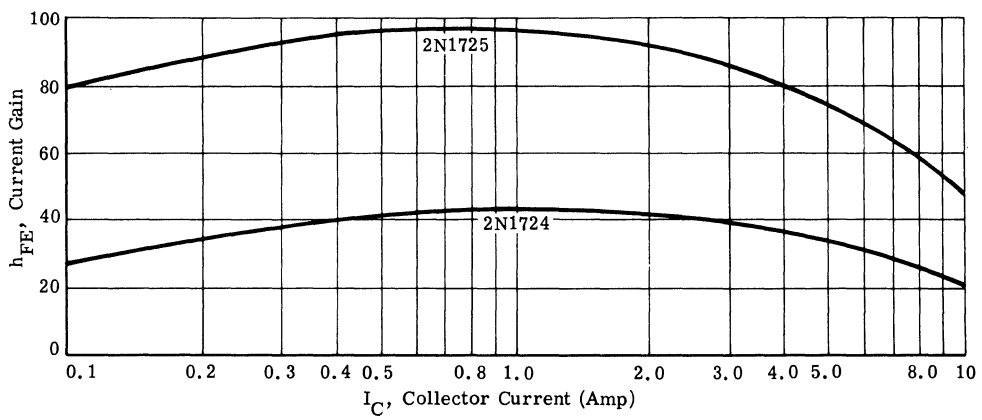


FIGURE 2 — 2N1724, 2N1725

In using these curves the average power derating curve (Fig. 1) must be observed to ensure operation below the maximum junction temperature.

FIGURE 3 — DC CURRENT GAIN versus COLLECTOR CURRENT



2N1742

For Specifications, See 2N499 Data.