

Silicon Controlled Rectifiers

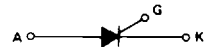
Reverse Blocking Triode Thyristors

... designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Blocking Voltage to 400 Volts

**2N1843
thru
2N1849**

**SCRs
16 AMPERES RMS
50 thru 400 VOLTS**



**CASE 263-04
STYLE 1**

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MAXIMUM RATINGS ($T_J = 100^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage, Note 1 2N1843 2N1844 2N1846 2N1849	V_{DRM} or V_{RRM}	50 100 200 400	Volts
*Non-Repetitive Peak Reverse Voltage 2N1843 2N1844 2N1846 2N1849	V_{RSM}	75 150 300 500	Volts
*Average On-State Current ($T_C = 35^\circ\text{C}$)	$I_{T(AV)}$	10	Amps
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)	I_{TSM}	125	Amps
Circuit Fusing ($t = 8.3$ ms)	I^2t	65	A^2s
*Peak Gate Power	P_{GM}	5	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2	Amps
*Peak Gate Voltage — Forward Reverse	V_{FGM} V_{RGM}	10 5	Volts
*Operating Junction Temperature Range	T_J	40 to +100	$^\circ\text{C}$
*Storage Temperature Range	T_{stg}	-40 to +125	$^\circ\text{C}$

*Indicates JEDEC Registered Data.

(cont.)

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

2N1843 thru 2N1849

THERMAL CHARACTERISTICS

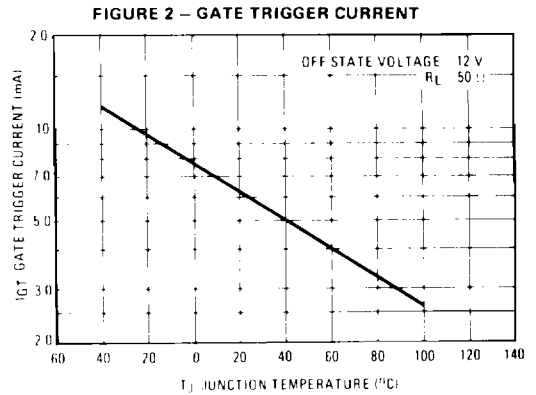
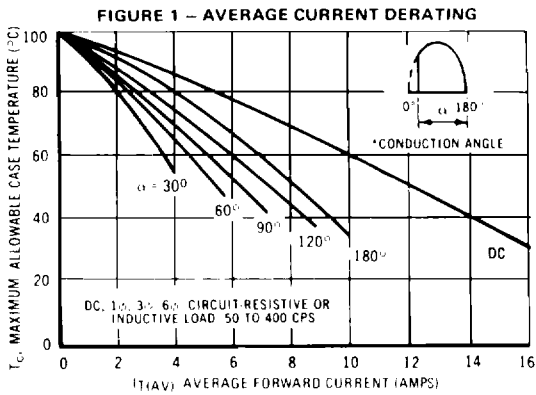
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (V_D Rated V_{DRM} , V_R Rated V_{RRM} , $T_C = 35^\circ\text{C}$) 2N1843 2N1844 2N1846 2N1849	$I_{D(AV)}$, $I_{R(AV)}$	—	—	19 12.5 6 4	mA
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM} , gate open) $T_J = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	I_{DRM} , I_{RRM}	—	—	10 6	μA mA
*Peak On-State Voltage ($I_{TM} = 31.4$ A peak, Pulse Width $\cdot 1$ ms, Duty Cycle $\cdot 2\%$)	V_{TM}	—	—	2.5	Volts
Gate Trigger Current (Continuous dc) ($V_D = 12$ Vdc, $R_L = 50 \Omega$) *($V_D = 12$ Vdc, $R_L = 50 \Omega$, $T_C = 40^\circ\text{C}$)	I_{GT}	—	6	80 150	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12$ Vdc, $R_L = 50 \Omega$) *($V_D = 12$ Vdc, $R_L = 50 \Omega$, $T_C = 40^\circ\text{C}$) *(V_D Rated V_{DRM} , $R_L = 50 \Omega$, $T_C = 100^\circ\text{C}$)	V_{GT}	—	0.65	— 3.5	Volts
Holding Current ($V_D = 12$ Vdc, Gate Open)	I_H	—	7	—	mA
Critical Rate of Rise of Off-State Voltage (V_D Rated V_{DRM} , Exponential Waveform, $T_C = 100^\circ\text{C}$, Gate Open)	dv/dt	—	30	—	$\text{V}/\mu\text{s}$

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