P2N2222A

Amplifier Transistors

NPN Silicon

Features

- These are Pb−Free Devices*

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CBO}	75	Vdc
Emitter−Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	600	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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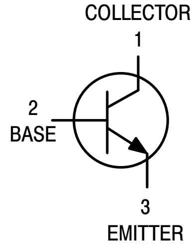
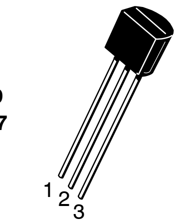
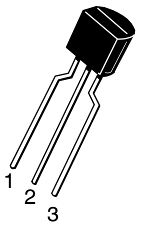
http://onsemi.com



TO−92
CASE 29
STYLE 17

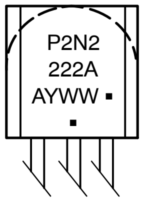


STRAIGHT LEAD
BULK PACK



BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
P2N2222AG	TO−92 (Pb−Free)	5000 Units/Bulk
P2N2222ARL1G	TO−92 (Pb−Free)	2000/Tape & Ammo

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

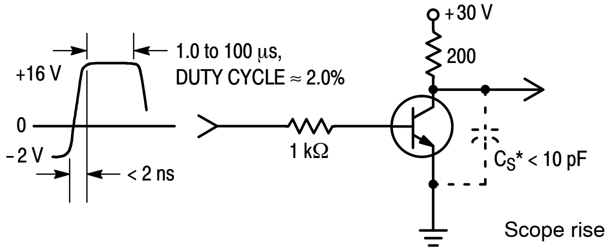
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage	$V_{(BR)CEO}$			Vdc
(I_C = 10 mAdc, I_B = 0)		40	–	
Collector – Base Breakdown Voltage	$V_{(BR)CBO}$	75		Vdc
(I_C = 10 μAdc, I_E = 0)			–	
Emitter – Base Breakdown Voltage	$V_{(BR)EBO}$			Vdc
(I_E = 10 μAdc, I_C = 0)		6.0	–	
Collector Cutoff Current	I_{CEX}			nAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)		–	10	
Collector Cutoff Current	I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)		–	0.01	
(V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)		–	10	
Emitter Cutoff Current	I_{EBO}		10	nAdc
(V_{EB} = 3.0 Vdc, I_C = 0)		–		
Collector Cutoff Current	I_{CEO}			nAdc
(V_{CE} = 10 V)		–	10	
Base Cutoff Current	I_{BEX}			nAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)		–	20	
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 10 Vdc)		35	–	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)		50	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)		75	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = −55°C)		35	–	
(I_C = 150 mAdc, V_{CE} = 10 Vdc) (Note 1)		100	300	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc) (Note 1)		50	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc) (Note 1)		40	–	
Collector – Emitter Saturation Voltage (Note 1)	$V_{CE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)		–	0.3	
(I_C = 500 mAdc, I_B = 50 mAdc)		–	1.0	
Base – Emitter Saturation Voltage (Note 1)	$V_{BE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)		0.6	1.2	
(I_C = 500 mAdc, I_B = 50 mAdc)		–	2.0	
SMALL – SIGNAL CHARACTERISTICS				
Current – Gain – Bandwidth Product (Note 2)	f_T			MHz
(I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)C		300	–	
Output Capacitance	C_{obo}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		–	8.0	
Input Capacitance	C_{ibo}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		–	25	
Input Impedance	h_{ie}			kΩ
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		2.0	8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		0.25	1.25	
Voltage Feedback Ratio	h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		–	8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		–	4.0	
Small–Signal Current Gain	h_{fe}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		50	300	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		75	375	
Output Admittance	h_{oe}			μMhos
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		5.0	35	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		25	200	
Collector Base Time Constant	$rb'C_c$			ps
(I_E = 20 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)		–	150	
Noise Figure	N_F			dB
(I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 1.0 kΩ, f = 1.0 kHz)		–	4.0	

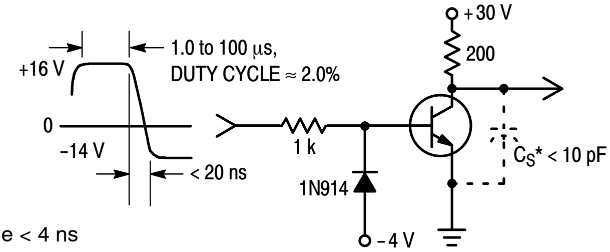
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = −2.0 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) (Figure 1)	t_d	–	10	ns
Rise Time		t_r	–	25	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) (Figure 2)	t_s	–	225	ns
Fall Time		t_f	–	60	ns

SWITCHING TIME EQUIVALENT TEST CIRCUITS





Scope rise time < 4 ns
*Total shunt capacitance of test jig, connectors, and oscilloscope.

Figure 1. Turn−On Time

Figure 2. Turn−Off Time

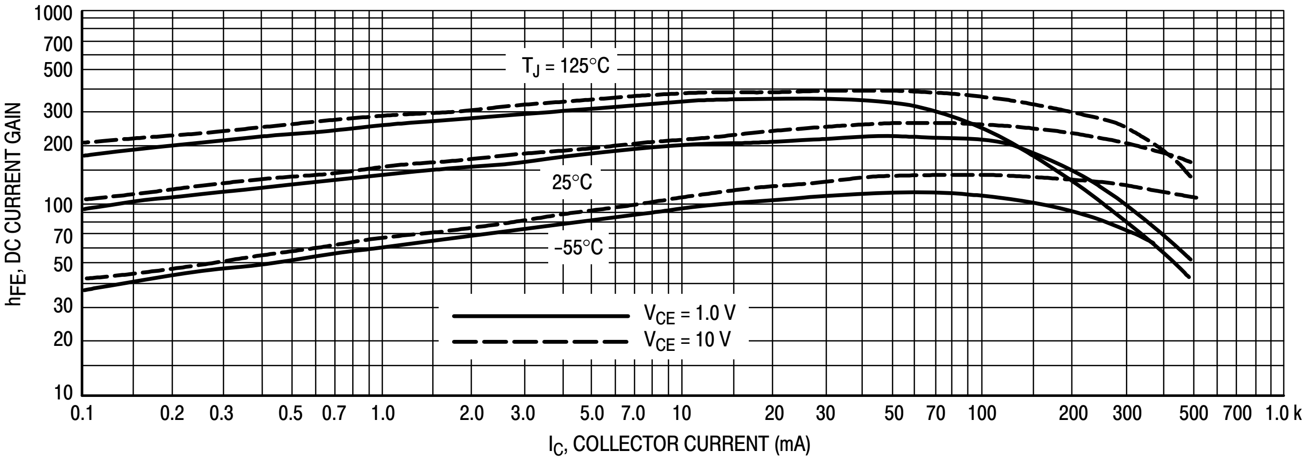


Figure 3. DC Current Gain

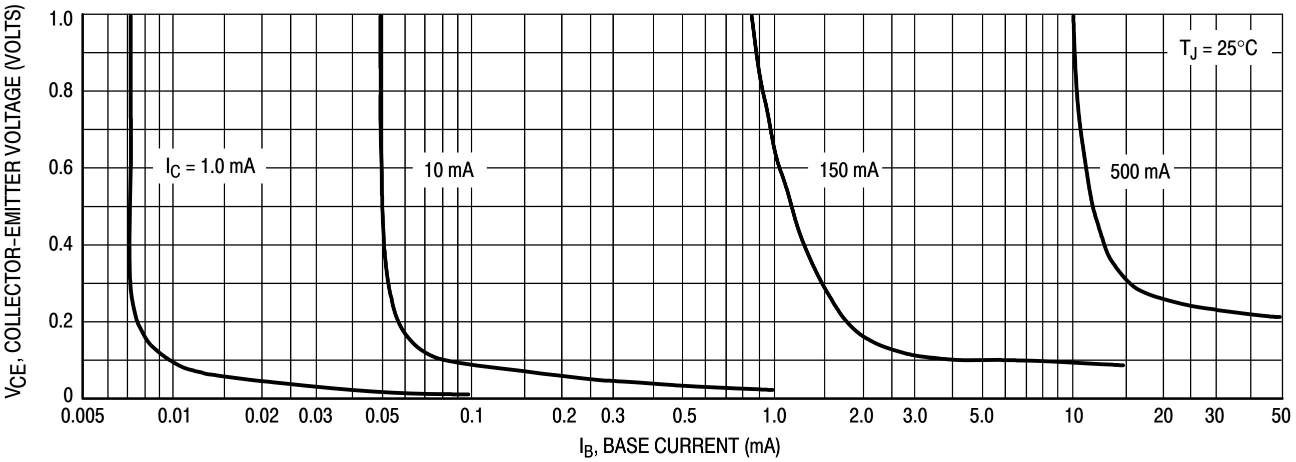


Figure 4. Collector Saturation Region

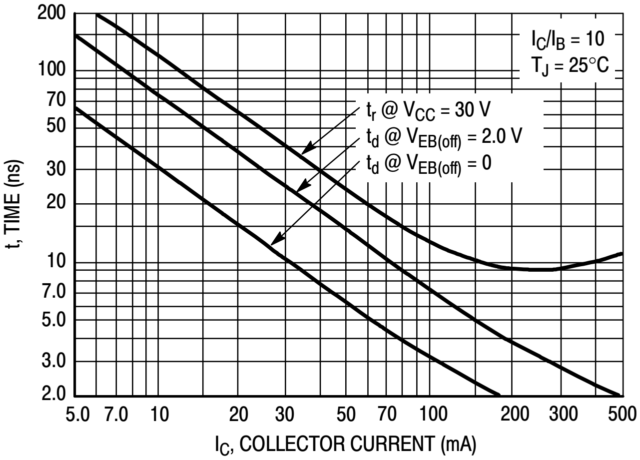


Figure 5. Turn−On Time

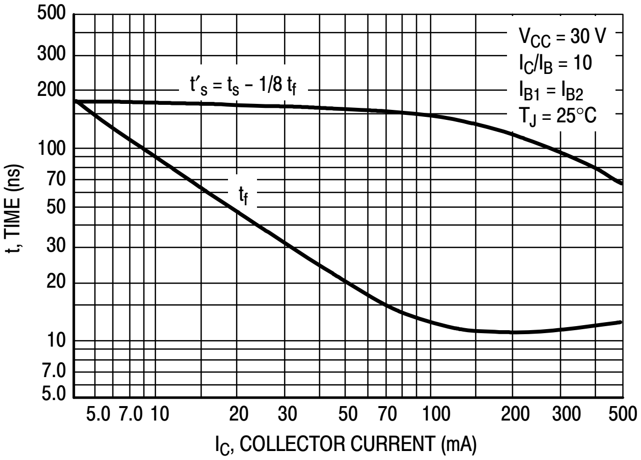


Figure 6. Turn−Off Time

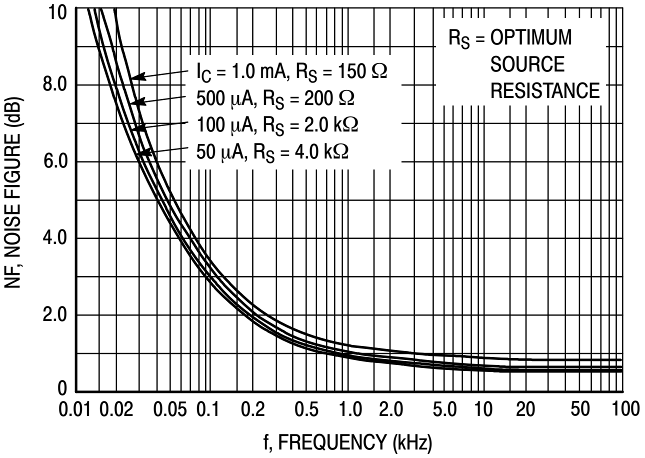


Figure 7. Frequency Effects

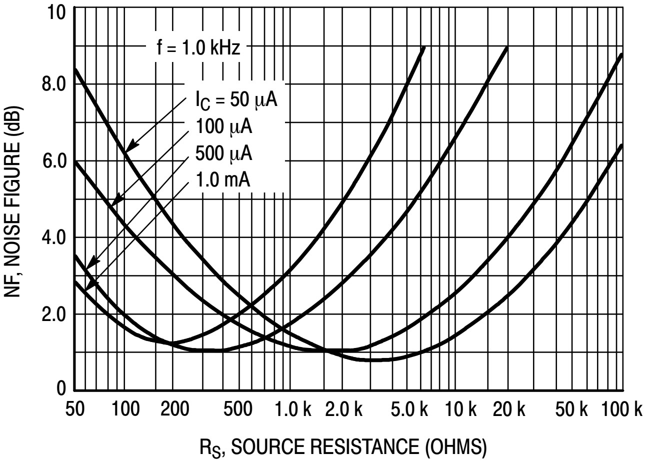


Figure 8. Source Resistance Effects

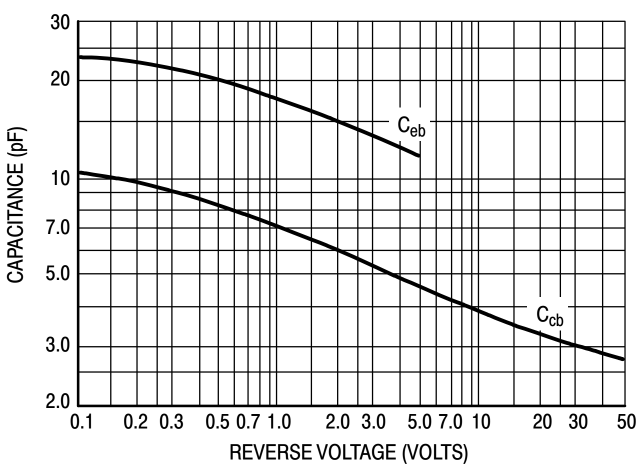


Figure 9. Capacitances

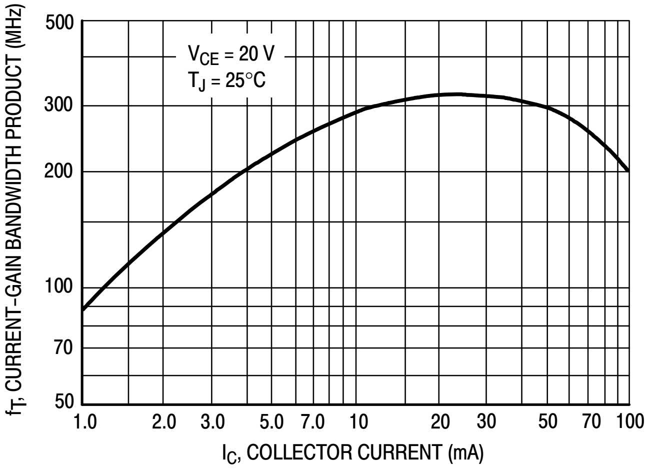


Figure 10. Current−Gain Bandwidth Product

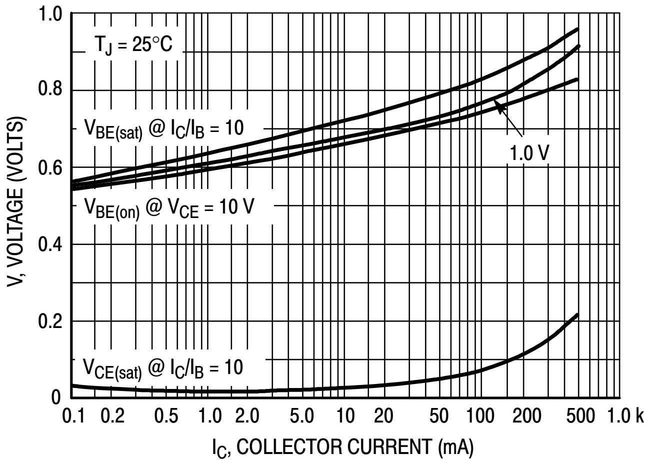


Figure 11. "On" Voltages

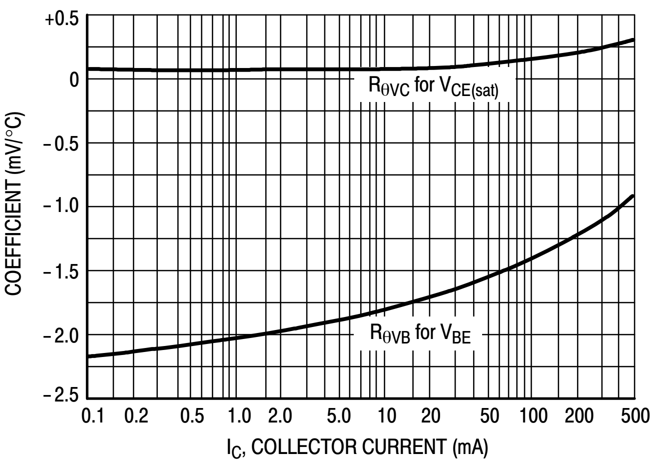
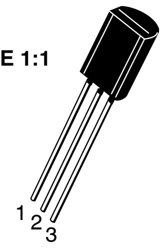


Figure 12. Temperature Coefficients

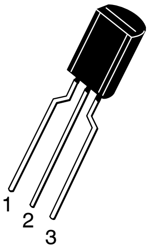
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1



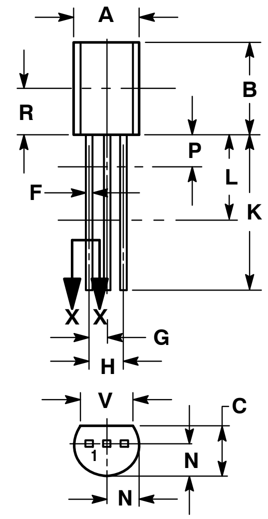
STRAIGHT LEAD



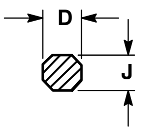
BENT LEAD

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012



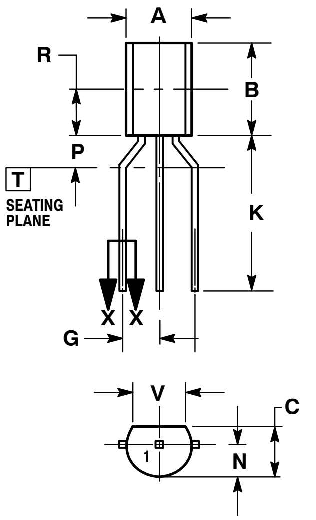
STRAIGHT LEAD



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---



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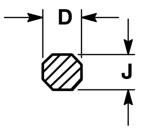

SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
G	0.094	0.102	2.40	2.80
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---

STYLES ON PAGE 2

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

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