2N3950 (SILICON)

NPN silicon RF power transistor designed for high-power RF amplifier applications in military and industrial equipment.

CASE 36
(TO-60)

Emitter common to stud and case

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	65	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector-Current — Continuous	I_C	3.3	Amp
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.8 16	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.4	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

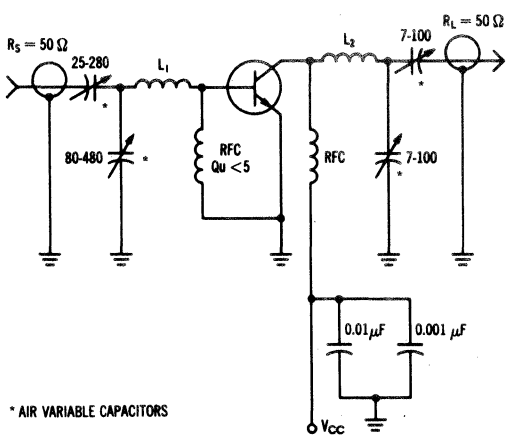
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	62.5	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	2.5	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$BV_{CEO(sus)}$	35	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	BV_{CES}	65	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 65 Vdc, I_E = 0)	I_{CBO}	—	—	10	mAdc
(V_{CB} = 28 Vdc, I_E = 0, T_A = 150°C)		—	—	10	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_E = 500 mAdc, V_{CE} = 28 Vdc, f = 50 MHz)	f_T	—	150	—	MHz
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	80	120	pF
FUNCTIONAL TEST					
Power Gain — Test Circuit — Figure 1, P_{out} = 50 W, V_{CC} = 28 Vdc, R_S = 50 ohms, f = 50 MHz	G_{PE}	8.0	—	—	dB
Collector-Efficiency	η	60	—	—	%

(1) Pulsed through a 25 mH inductor; Duty factor = 50%, Rep. Rate ≤ 60 Hz.

FIGURE 1 — 50 MHz TEST CIRCUIT

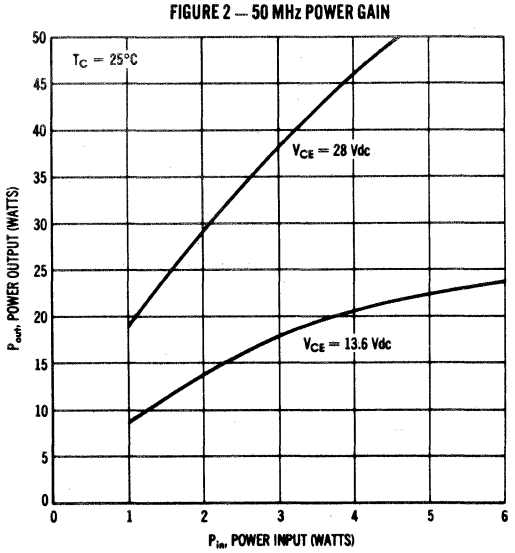


* AIR VARIABLE CAPACITORS

L_1 = 2 TURNS #18 TINNED WIRE, ¼" I.D., AIR WOUND, WINDING LENGTH ⅛".

L_2 = 5 TURNS #16 TINNED WIRE, ⅜" I.D., AIR WOUND, WINDING LENGTH ¾".

FIGURE 2 — 50 MHz POWER GAIN



CLASS C DESIGN DATA FOR V_{CE} = 28 Vdc, T_C = 25°C

(EMITTER GROUNDED DIRECTLY TO THE CHASSIS — NO TUNED-EMITTER TECHNIQUES USED)

FIGURE 3 — POWER OUTPUT

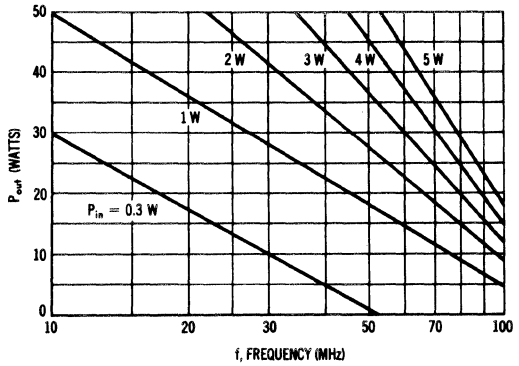


FIGURE 4 — PARALLEL EQUIVALENT OUTPUT CAPACITANCE

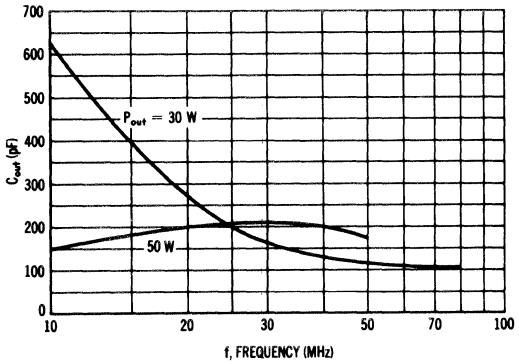


FIGURE 5 — PARALLEL EQUIVALENT INPUT RESISTANCE

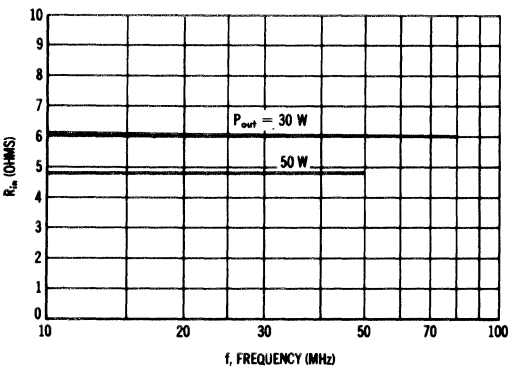
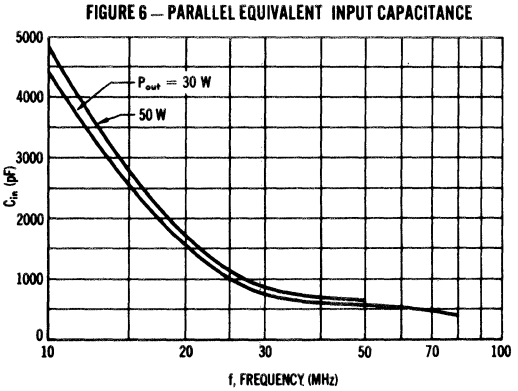


FIGURE 6 — PARALLEL EQUIVALENT INPUT CAPACITANCE



DESIGN NOTES

For Class-C power-amplifier designs, the small-signal parameters are not applicable. Figures 4 thru 6 and 8 thru 10 give the parallel equivalent output capacitance and input capacitance and resistance for Class-C power-amplifier operation.

The parallel resistive portion of the collector load impedance for a power amplifier, R_L' may be computed by assuming a peak voltage swing equal to V_{CC}, and using the expression $R_L' = V_{CC}^2/2P$ where P = RF power output. The computed R_L' may then be combined with the data in Figures 4 through 10 to comprise complete device impedance data for Class-C power-amplifier design.

Due to the high performance capabilities of the 2N3950, care should be exercised during initial tuning of prototype circuits.

Input power should be increased gradually, while stopping at intermediate levels to tune. If tuning difficulties are experienced, or if the power or collector current are abnormal at any intermediate power input level, the difficulties should be resolved before increasing power levels further.

The 2N3950 is designed to provide maximum ruggedness commensurate with its high performance. Operation at loads with high SWR may produce dangerous voltage and current excursions, a condition which should be avoided. In addition, disconnecting the load at full power output could increase device dissipation to over 70 watts which could result in device failure due to dissipation beyond safe limits set by the junction to ambient thermal resistance, regardless of the internal construction and safe area of the device.

CLASS C DESIGN DATA FOR V_{CE} = 13.6 Vdc, T_C = 25°C

(EMITTER GROUNDED DIRECTLY TO THE CHASSIS — NO TUNED-EMITTER TECHNIQUES USED)

FIGURE 7 — POWER OUTPUT

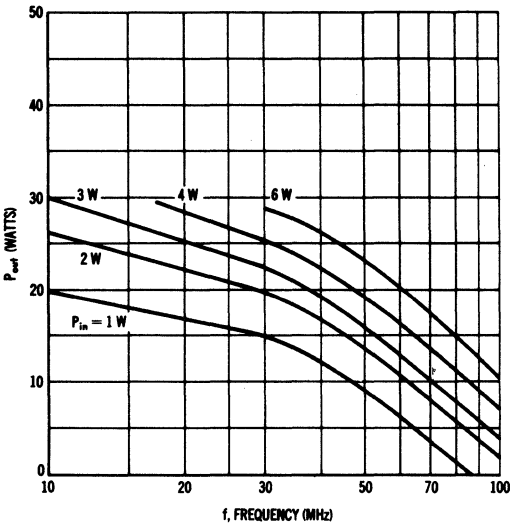


FIGURE 8 — PARALLEL EQUIVALENT OUTPUT CAPACITANCE

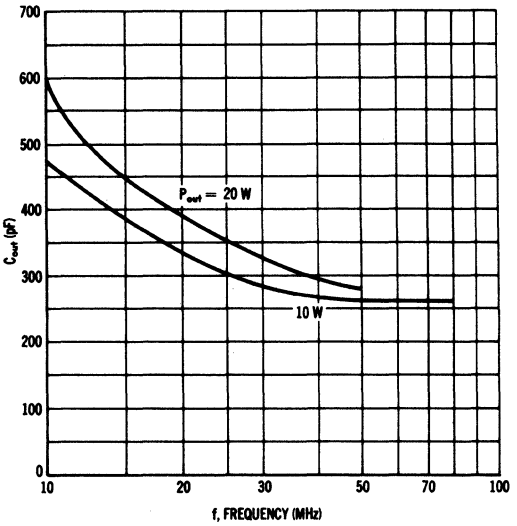


FIGURE 9 — PARALLEL EQUIVALENT INPUT RESISTANCE

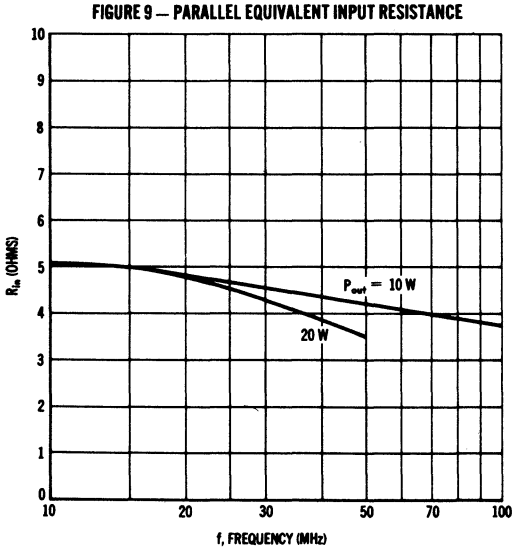


FIGURE 10 — PARALLEL EQUIVALENT INPUT CAPACITANCE