

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	12	Vdc
Collector-Base Voltage	V _{CBO}	20	Vdc
Emitter-Base Voltage	V _{EBO}	4.5	Vdc
Total Device Dissipation @ T _A = 25°C Derate above 25°C	P _D	400 2.3	mW mW/°C
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	750 4.3	mW mW/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.233	°C/mW
Thermal Resistance, Junction to Ambient	R _{θJA}	0.436	°C/mW

2N3959
2N3960

JAN, JTX, JTXV AVAILABLE
CASE 22-03, STYLE 1
TO-18 (TO-206AA)
HIGH FREQUENCY TRANSISTOR

NPN SILICON



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage (I _C = 10 mA _{dc} , I _B = 0)	V _{(BR)CEO}	12	—	—	Vdc
Collector-Base Breakdown Voltage (I _C = 10 μA _{dc} , I _E = 0)	V _{(BR)CBO}	20	—	—	Vdc
Emitter-Base Breakdown Voltage (I _E = 10 μA _{dc} , I _C = 0)	V _{(BR)EBO}	4.5	—	—	Vdc
Collector Cutoff Current (V _{CE} = 10 Vdc, V _{EB} = 2.0 Vdc) (V _{CE} = 10 Vdc, V _{EB} = 2.0 Vdc, T _A = 150°C)	I _{CEX}	—	—	0.005 5.0	μA _{dc}
Collector Forward Current (V _{CE} = 5.0 Vdc, V _{BE} = 0.4 Vdc)	I _{CEX}	—	—	1.0	μA _{dc}
Base Cutoff Current (V _{CE} = 10 Vdc, V _{EB} = 2.0 Vdc)	I _{BL}	—	—	0.005	μA _{dc}

ON CHARACTERISTICS

DC Current Gain (I _C = 1.0 mA _{dc} , V _{CE} = 1.0 Vdc) (I _C = 10 mA _{dc} , V _{CE} = 1.0 Vdc) (I _C = 30 mA _{dc} , V _{CE} = 1.0 Vdc)	h _{FE}	25 40 25	— — —	— 400 —	—
Collector-Emitter Saturation Voltage (I _C = 1.0 mA _{dc} , I _B = 0.1 mA _{dc}) (I _C = 30 mA _{dc} , I _B = 3.0 mA _{dc})	V _{CE(sat)}	— —	— —	0.2 0.3	Vdc
Base-Emitter On Voltage (I _C = 1.0 mA _{dc} , V _{CE} = 1.0 Vdc) (I _C = 30 mA _{dc} , V _{CE} = 1.0 Vdc)	V _{BE(on)}	— —	— —	0.8 1.0	Vdc

SMALL SIGNAL CHARACTERISTICS

Current-Gain — Bandwidth Product (I _C = 5.0 mA _{dc} , V _{CE} = 4.0 Vdc, f = 100 MHz)	2N3959 2N3960	f _T	1000 1300	— —	— —	MHz
(I _C = 10 mA _{dc} , V _{CE} = 10 Vdc, f = 100 MHz)	2N3959 2N3960		1300 1600	— —	— —	
(I _C = 30 mA _{dc} , V _{CE} = 4.0 Vdc, f = 100 MHz)	2N3959 2N3960		1000 1200	— —	— —	
Output Capacitance (V _{CB} = 4.0 Vdc, I _E = 0, f = 1.0 MHz)		C _{obo}	—	2.0	2.5	pF

2N3959 • 2N3960

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit	
Input Capacitance ($V_{EB} = 0.5\text{ Vdc}$, $I_C = 0$, $f = 100\text{ MHz}$)	C_{ibo}	—	1.5	2.5	pF	
Collector Base Time Constant ($I_C = 5.0\text{ mA}$, $V_{CE} = 4.0\text{ Vdc}$)	$rb' C_C$	—	—	30	ps	
		2N3959	—	—		50
		2N3960	—	—		—
($I_C = 10\text{ mA}$, $V_{CE} = 10\text{ Vdc}$)	2N3959	—	—	25	ps	
		2N3960	—	—		40
($I_C = 30\text{ mA}$, $V_{CE} = 4.0\text{ Vdc}$)	2N3959	—	—	30	ps	
		2N3960	—	—		50

SWITCHING CHARACTERISTICS (FIGURE 7)

Turn-On Delay Time ($I_C = 10\text{ mA}$, $V_{out} = 1.0\text{ Vdc}$) ($I_C = 30\text{ mA}$, $V_{out} = 1.0\text{ Vdc}$)		$t_{d(on)}$	—	2.4	—	ns
			—	2.0	—	
Rise Time ($I_C = 10\text{ mA}$, $V_{out} = 1.0\text{ Vdc}$) ($I_C = 30\text{ mA}$, $V_{out} = 1.0\text{ Vdc}$)	Both Devices	t_r	—	3.0	—	ns
	2N3959		—	2.2	—	
	2N3960		—	1.7	—	
Turn-Off Delay Time ($I_C = 10\text{ mA}$, $V_{out} = 1.0\text{ Vdc}$) ($I_C = 30\text{ mA}$, $V_{out} = 1.0\text{ Vdc}$)		$t_{d(off)}$	—	1.6	—	ns
			—	1.6	—	
Fall Time ($I_C = 10\text{ mA}$, $V_{out} = 1.0\text{ Vdc}$) ($I_C = 30\text{ mA}$, $V_{out} = 1.0\text{ Vdc}$)	Both Devices	t_f	—	3.3	—	ns
	2N3959		—	2.3	—	
	2N3960		—	1.9	—	

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FIGURE 1 – TYPICAL DC CURRENT GAIN

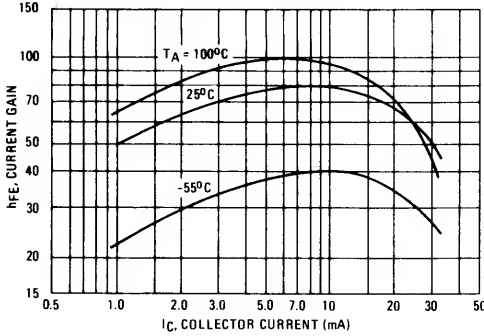


FIGURE 2 – TYPICAL CURRENT-GAIN – BANDWIDTH PRODUCT

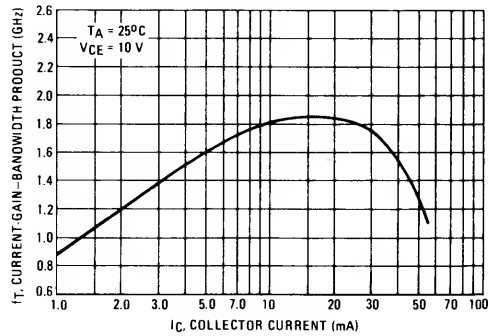


FIGURE 3 – TYPICAL COLLECTOR-BASE TIME CONSTANT

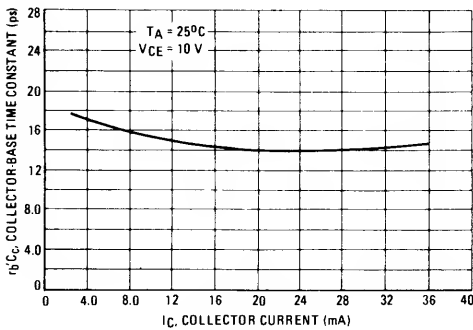
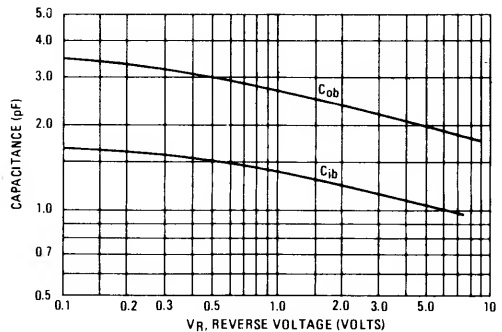


FIGURE 4 – TYPICAL JUNCTION CAPACITANCE



TURN-ON AND TURN-OFF TIMES

FIGURE 5 - $V_{out} = 1.0 \text{ Vdc}$

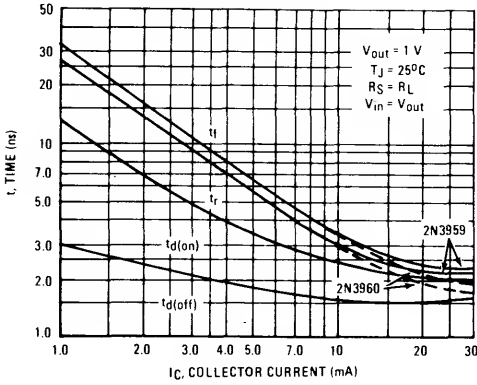


FIGURE 6 - $V_{out} = 2.0 \text{ Vdc}$

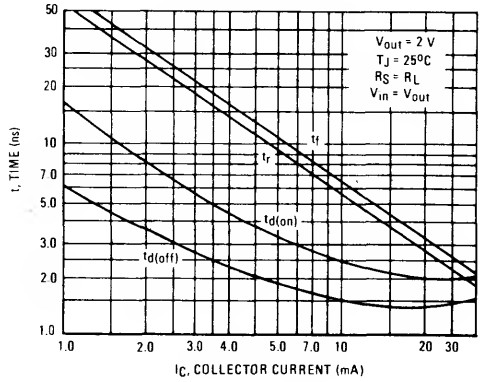
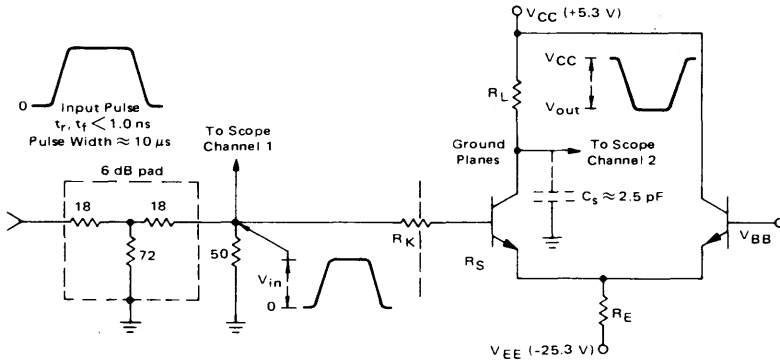


FIGURE 7 - SWITCHING TIMES TEST CIRCUIT



This test set up is designed to simulate a cascade of identical stages. The source resistance (R_S) equals the load resistance (R_L). Values used in the test are shown in the table.

For $V_{in} = V_{out} = 1 \text{ V}$, $V_{BB} = +0.5 \text{ V}$, R_L & R_K values appropriately reduced.

$V_{in} = V_{out} = 2 \text{ volts}$, $V_{BB} = +1.0 \text{ V}$			
i_C (mA)	R_E (k Ω)	R_L (Ω)	R_K (Ω)
10	240	2.0 k	2.0 k
30	8.2	680	680
10	2.4	200	180
30	0.8	68	36