

# n-channel JFET designed for . . .



**Performance Curves NH**  
See Section 4

- Analog Switches
- Choppers
- Commutators

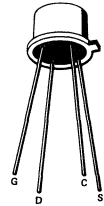
**BENEFITS**

- Low Insertion Loss, No Offset Voltage  
 $R_{DS(on)} < 220 \Omega$
- Short Switching Aperture Times  
 $C_{rss} < 1.5 \text{ pF}$   
 $t_{(on)} + t_{(off)} < 50 \text{ ns Typical}$

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage	.....-30 V
Gate Current	..... 10 mA
Total Device Dissipation (25°C Free-Air Temperature)	..... 300 mW
Power Derating	..... 1.7 mW/°C
Storage Temperature Range	.....-55 to +200°C
Operating Temperature Range	.....-55 to +175°C
Lead Temperature (1/16" from case for 10 seconds)	..... 300°C

**TQ-72**  
See Section 5



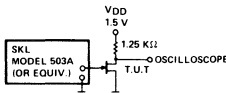
**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic	Min	Typ	Max	Unit	Test Conditions
S T A T I C	1	$I_{GSS}$ Gate Reverse Current			-0.1	nA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$
	2	$V_{GS(off)}$ Gate-Source Cutoff Voltage	-4		-6.0	V	$V_{DS} = 10 \text{ V}, I_D = 10 \text{ nA}$
	3	$BV_{GSS}$ Gate-Source Breakdown Voltage	-30				$I_G = -1 \mu\text{A}, V_{DS} = 0$
	4	$I_{DSS}$ Saturation Drain Current (Note 1)	2.0			mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$
	5	$I_{D(off)}$ Drain Cutoff Current			1.0	nA	$V_{DS} = 10 \text{ V}, V_{GS} = -7 \text{ V}$ $T_A = 150^\circ\text{C}$
6				2.0	$\mu\text{A}$		
D Y N	7	$r_{DS(on)}$ Static Drain-Source ON Resistance			220	$\Omega$	$V_{DS} \leq 0.1 \text{ V}, V_{GS} = 0$
	8	$V_{DS(on)}$ Drain-Source ON Voltage			0.25	V	$I_D = 1 \text{ mA}, V_{GS} = 0$
	9	$I_{DGO}$ Drain Reverse Current			0.1	nA	$V_{DG} = 20 \text{ V}, I_S = 0$ $T_A = 150^\circ\text{C}$
	10				0.2	$\mu\text{A}$	
S W I T C H	11	$r_{ds(on)}$ Drain-Source ON Resistance			220	$\Omega$	$V_{GS} = 0, I_D = 0$ $f = 1 \text{ kHz}$
	12	$C_{iss}$ Common-Source Input Capacitance		3.1	6.0	pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0$ $f = 1 \text{ MHz}$
	13	$C_{rss}$ Common-Source Reverse Transfer Capacitance		0.8	1.5		$V_{DS} = 0, V_{GS} = -7 \text{ V}$
14	$t_{d(on)}$ Turn ON Delay Time		3.0	20	ns	$V_{DD} = 1.5 \text{ V}$ $I_{D(on)} = 1.0 \text{ mA}$ $V_{GS(on)} = 0$ $V_{GS(off)} = -6 \text{ V}$ $R_L = 1.25 \text{ k}\Omega$ See Circuit Below	
15	$t_r$ Rise Time		10.0	100			
16	$t_{off}$ Turn OFF Time		30.0	100			
17	$t_{d(off)}$ Turn OFF Delay Time (Note 2)		10.0				
18	$t_f$ Fall Time (Note 2)		20.0				

\*JEDEC registered parameters unless otherwise noted (apply to min/max only).

**NOTES:**

1. Pulse test duration  $\leq 2 \text{ ms}$ .
2. Non-JEDEC registered parameters:  
 $t_{d(off)} + t_f = t_{off}$ .



**NH**

INPUT PULSE	SAMPLING SCOPE
RISE TIME - 1 ns	RISE TIME - 10 ns
FALL TIME - 1 ns	INPUT RESISTANCE > 5 M $\Omega$ < 10 pF
PULSE WIDTH 1 ns	
PULSE DUTY CYCLE 50%	
INPUT RESISTANCE 50 $\Omega$	