

n-channel JFETs designed for . . .



Performance Curves NC
See Section 5

- Analog Switches
- Choppers
- Amplifiers

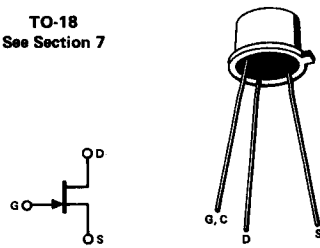
BENEFITS

- Low Insertion Loss
 $R_{DS(on)} < 30 \Omega$ (2N3970)
- Good Off-Isolation
 $I_{D(off)} < 250 \text{ pA}$

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage -40 V
 Gate Current 50 mA
 Total Device Dissipation at 25°C Case Temperature
 (Note 1) 1.8 W
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 60 seconds) 300°C

TO-18
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

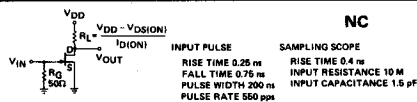
Characteristic	2N3970		2N3971		2N3972		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max		
1 BV _{GSS} Gate Reverse Breakdown Voltage	-40		-40		-40		V	I _G = -1 μA, V _{DS} = 0
2 ID _{GO} Drain Reverse Current		250		250		250	pA	V _{DG} = 20 V, I _S = 0
3		500		500		500	nA	
4 ID(off) Drain Cutoff Current		250		250		250	pA	V _{DS} = 20 V, V _{GS} = -12 V
5		500		500		500	nA	
6 V _{GS(off)} Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	V _{DS} = 20 V, I _D = 1 nA
7 IDSS Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	50	150	25	75	5	30	mA	V _{DS} = 20 V, V _{GS} = 0
8						2		
9 V _{DS(on)} Drain-Source ON Voltage				1.5			V	V _{GS} = 0
10		1						I _D = 5 mA
10								I _D = 10 mA
10								I _D = 20 mA
11 r _{DS(on)} Static Drain-Source ON Resistance		30		60		100	Ω	V _{GS} = 0, I _D = 1 mA
12 r _{ds(on)} Drain-Source ON Resistance		30		60		100	Ω	V _{GS} = 0, I _D = 0
13 C _{iss} Common-Source Input Capacitance		25		25		25	pF	V _{DS} = 20 V, V _{GS} = 0
14 C _{rss} Common-Source Reverse Transfer Capacitance		6		6		6	pF	V _{DS} = 0, V _{GS} = -12 V
15 t _{d(on)} Turn-On Delay Time		10		15		40	ns	V _{DD} = 10 V, V _{GS(on)} = 0
16 t _r Rise Time		10		15		40	ns	I _{D(on)} R _L V _{GS(off)}
17 t _{off} Turn-Off Time		30		60		100	ns	2N3970 20 mA 450 Ω -10 V
								2N3971 10 mA 850 Ω -5 V
								2N3972 5 mA 1.6KΩ -3 V

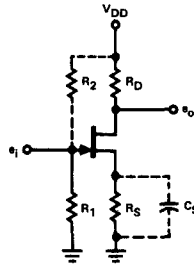
3

*JEDEC registered data.

NOTE:

- Derate linearly at the rate of 10 mW/°C.





Amplifier Design Chart
(C_S for 3 dB Point at 50 Hz)

VDD (V)	RS (Ω)	R1 (MΩ)	R2 (MΩ)	CS (μF)	IDD (mA)	RD (Ω)	eo Max (V)	AV
2N3970								
30	560	1	∞	100	11	1K	3	9
	2.7K	3.3	10	100	6	1K	2.5	8
VDD = 15 VSS = -15	3K	1	Source Follower		7	0	8.5	0.96
	7.5K	1			6	0	8.5	0.96
VDD = 15 VSS = -15	7.5K	1	Source Follower		6	0	15	0.97
2N3971								
20	2K	4.7	11	100	5	1K	1.5	8-11
	330	1	∞	100	8	820	1.5	9
	330	1	∞	0	8	820	3	1.9
30	2K	4.7	11	100	6	2.7K	5	18-24
	330	1	∞	100	8	1.5K	2.5	15
	330	1	∞	0	8	1.5K	5.5	3.3
VDD = 15 VSS = -15	4.7K	1	Source Follower		5	0	11	0.97
2N3972								
10	220	1	∞	0	5	1.2K	1.5	3.5
20	220	1	∞	0	5	2.2K	3.5	7
30	1K	1	12	100	4	3.9K	5	38
	1K	1	12	100	4	5.6K	3.5	40-55
VDD = 15 VSS = -15	4.7K	1	Source Follower		2.5	0	13	0.98
	7.5K	1			1.5	0	13	0.98