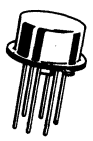
2N4066 (SILICON)
2N4067

DUAL P-CHANNEL
MOS FIELD-EFFECT TRANSISTORS

Enhancement Mode MOS Field-Effect Transistors designed primarily for low-power, chopper or switching applications.

- High Forward Transadmittance –
  $|y_{fs}|$ = 2.5 mmhos (Min) @ V_{DS} = -15 Vdc (2N4067)
- Low Forward Gate Current –
  I_{GF} = 2.5 pAdc (Max) @ V_{GS} = -25 Vdc
- Low Drain-Source "ON" Resistance –
  $r_{ds(on)}$ = 250 Ohms (Max) @ V_{GS} = -15 Vdc (2N4067)

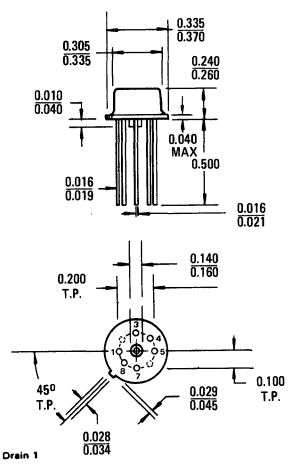
DUAL P-CHANNEL
MOS FIELD-EFFECT
TRANSISTORS



***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	Vdc
Drain-Gate Voltage	V_{DG}	-25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	+25	Vdc
Forward Gate-Source Voltage	V_{GSF}	-25	Vdc
Drain Current	I_D	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.6 4.0	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.7 11.3	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C
Operating Junction Temperature Range	T_J	-65 to +175	°C

*Indicates JEDEC Registered Data.



Pin 1. Drain 1
3. Gate 1
4. Substrate.
5. Gate 2
7. Drain 2
8. Source 1 and 2

Case 642-01

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_{GS} = 0)		$V_{(BR)DSS}$	-30	–	Vdc
Source-Drain Breakdown Voltage (I_S = 10 μAdc, V_{GD} = 0)		$V_{(BR)SDS}$	-30	–	Vdc
Zero-Gate Voltage Source Current		I_{SDS}			
(V_{SD} = -15 Vdc, V_{GD} = 0)			–	1.0	nAdc
(V_{SD} = -15 Vdc, V_{GD} = 0, T_A = 150°C)			–	2.0	μAdc
Zero-Gate Voltage Drain Current (Note 1)		I_{DSS}			
(V_{DS} = -15 Vdc, V_{GS} = 0)			–	1.0	nAdc
(V_{DS} = -15 Vdc, V_{GS} = 0, T_A = 150°C)			–	2.0	μAdc
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V_{DS} = -15 Vdc, I_D = 10 μAdc)		$V_{GS(TH)}$	-3.0	-6.0	Vdc
Forward Gate Current (V_{GS} = -25 Vdc, V_{DS} = 0)		I_{GF}	–	2.5	pAdc
"ON" Drain Current (V_{DS} = -15 Vdc, V_{GS} = -15 Vdc)		$I_{D(on)}$	10	50	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Static Drain-Source "ON" Resistance		$r_{ds(on)}$			Ohms
(V_{GS} = -15 Vdc, I_D = 0, f = 1.0 kHz)	2N4066		–	500	
	2N4067		–	250	
Forward Transadmittance (Note 1)		$\lvert y_{fs} \rvert$			mmhos
(V_{DS} = -15 Vdc, V_{GS} = -15 Vdc, f = 1.0 kHz)	2N4066		1.5	–	
	2N4067		2.5	–	
(V_{DS} = -15 Vdc, V_{GS} = -15 Vdc, f = 1.0 kHz, T_A = 100°C)	2N4066		1.0	–	
	2N4067		1.75	–	
Output Admittance (V_{DS} = -15 Vdc, V_{GS} = -15 Vdc, f = 1.0 kHz)		$\lvert y_{os} \rvert$	–	300	μmhos
Input Capacitance (V_{DS} = -15 Vdc, V_{GS} = -15 Vdc, f = 1.0 MHz)		C_{iss}	–	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	pF
Source-Substrate Capacitance (V_{DU} = -15 Vdc, V_{GS} = 0, I_S = 0, f = 1.0 MHz)		C_{SU}	–	5.0	pF
Drain-Substrate Capacitance (V_{SU} = -15 Vdc, V_{GS} = 0, I_S = 0, f = 1.0 MHz)		C_{DU}	–	5.0	pF
SWITCHING CHARACTERISTICS					
Delay Time	(V_{DD} = -15 Vdc, $I_{D(on)}$ = 10 mAdc,	t_d	–	20	ns
Rise Time		t_r	–	30	ns
Turn-Off Time	$V_{GS(on)}$ = -15 Vdc, $V_{GS(off)}$ = 0)	t_{off}	–	50	ns

*Indicates JEDEC Registered Data.

Note 1: Pulse Test: Pulse Width ≤ 630 ms, Duty Cycle ≤ 10%.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT