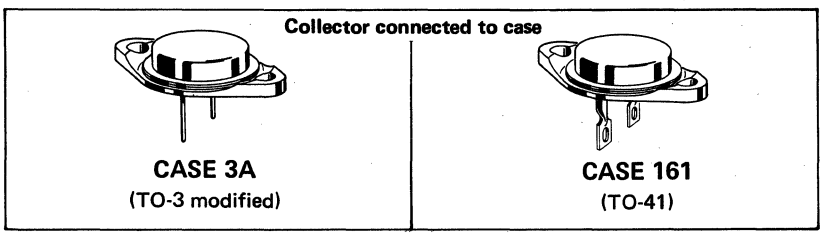
2N4276 (GERMANIUM)
thru
2N4283

PNP germanium power transistors designed for high current applications requiring high-gain and low saturation voltages.



For units with lugs attached, specify devices MP4276 etc. (TO-41 package)

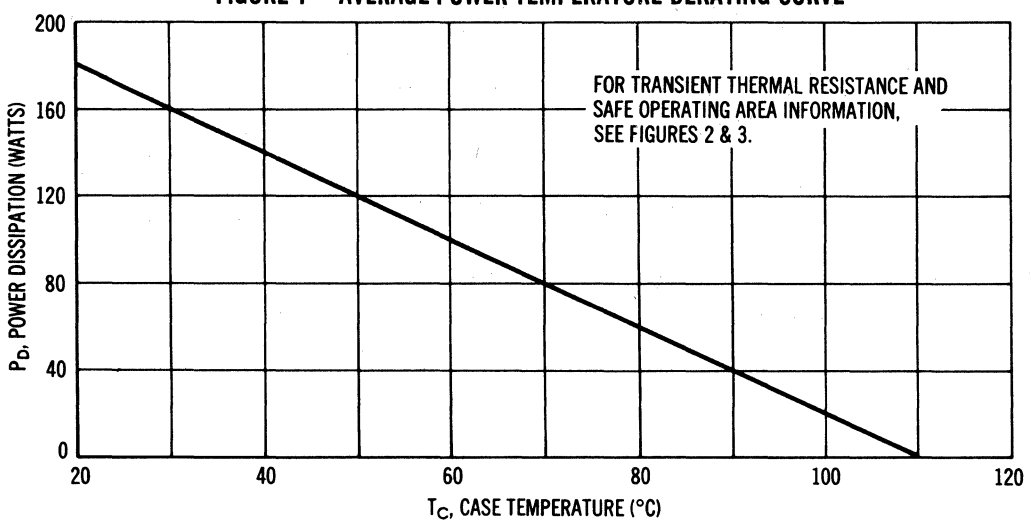
MAXIMUM RATINGS

Rating	Symbol	2N4276 2N4277	2N4278 2N4279	2N4280 2N4281	2N4282 2N4283	Unit
Collector-Emitter Voltage	V_{CEO}	20	30	45	60	Vdc
Collector-Emitter Voltage	V_{CES}	30	45	60	75	Vdc
Collector-Base Voltage	V_{CB}	30	45	60	75	Vdc
Emitter-Base Voltage	V_{EB}	20	25	30	40	Vdc
Collector Current — Continuous *	I_C*	← 60 →				Adc
Total Device Dissipation @ T_C = 25°C	P_D	← 170 →				Watts
Derate above 25°C		← 2.0 →				W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +110 →				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	← 0.5 →	°C/W

FIGURE 1 — AVERAGE POWER-TEMPERATURE DERATING CURVE



*JEDEC Registered Values, For True Capability See Figure 3.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage† (I_C = 1.0 Adc, I_B = 0)	2N4276, 2N4277	BV_{CEO}†	20	-	Vdc
	2N4278, 2N4279		30	-	
	2N4280, 2N4281		45	-	
	2N4282, 2N4283		60	-	
Collector-Emitter Breakdown Voltage (I_C = 300 mAdc, V_{BE} = 0)	2N4276, 2N4277	BV_{CES}	30	-	Vdc
	2N4278, 2N4279		45	-	
	2N4280, 2N4281		60	-	
	2N4282, 2N4283		75	-	
Floating Potential (V_{CB} = 30 Vdc, I_E = 0)	2N4276, 2N4277	V_{EBF}	-	0.5	Vdc
(V_{CB} = 45 Vdc, I_E = 0)	2N4278, 2N4279		-	0.5	
(V_{CB} = 60 Vdc, I_E = 0)	2N4280, 2N4281		-	0.5	
(V_{CB} = 75 Vdc, I_E = 0)	2N4282, 2N4283		-	0.5	
Collector Cutoff Current (V_{CE} = 20 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4276, 2N4277	I_{CEX}	-	15	mAdc
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4278, 2N4279		-	15	
(V_{CE} = 45 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4280, 2N4281		-	15	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4282, 2N4283		-	15	
Collector Cutoff Current (V_{CB} = 2.0 Vdc, I_E = 0)		I_{CBO}	-	0.2	mAdc
(V_{CB} = 30 Vdc, I_E = 0)	2N4276, 2N4277		-	4.0	
(V_{CB} = 45 Vdc, I_E = 0)	2N4278, 2N4279		-	4.0	
(V_{CB} = 60 Vdc, I_E = 0)	2N4280, 2N4281		-	4.0	
(V_{CB} = 75 Vdc, I_E = 0)	2N4282, 2N4283		-	4.0	
Emitter Cutoff Current (V_{BE} = 20 Vdc, I_C = 0)	2N4276, 2N4277	I_{EBO}	-	4.0	mAdc
(V_{BE} = 20 Vdc, I_C = 0, T_C = +71°C)			-	15	
(V_{BE} = 25 Vdc, I_C = 0)	2N4278, 2N4279		-	4.0	
(V_{BE} = 25 Vdc, I_C = 0, T_C = +71°C)			-	15	
(V_{BE} = 30 Vdc, I_C = 0)	2N4280, 2N4281		-	4.0	
(V_{BE} = 30 Vdc, I_C = 0, T_C = +71°C)			-	15	
(V_{BE} = 40 Vdc, I_C = 0)	2N4282, 2N4283		-	4.0	
(V_{BE} = 40 Vdc, I_C = 0, T_C = +71°C)			-	15	
ON CHARACTERISTICS					
DC Current Gain† (I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4276, 2N4278, 2N4280, 2N4282	h_{FE}†	60	180	-
	2N4277, 2N4279, 2N4281, 2N4283		120	240	
(I_C = 60 Adc, V_{CE} = 2.0 Vdc)			15	-	
Collector-Emitter Saturation Voltage† (I_C = 15 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$†	-	0.15	Vdc
(I_C = 60 Adc, I_B = 6.0 Adc)			-	0.3	
Base-Emitter Saturation Voltage† (I_C = 15 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$†	-	0.6	Vdc
(I_C = 60 Adc, I_B = 6.0 Adc)			-	1.0	
SMALL SIGNAL CHARACTERISTICS					
Common-Emitter Cutoff Frequency (I_C = 15 Adc, V_{CE} = 2.0 Vdc)		$f_{\alpha e}$	2.0	-	kHz

† To avoid excessive heating of the collector junction, perform test with pulse method.

FIGURE 2 — TRANSIENT THERMAL RESISTANCE

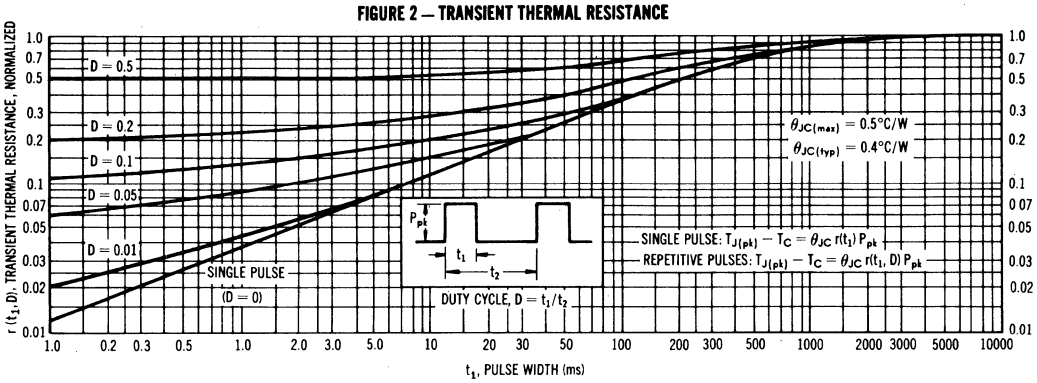
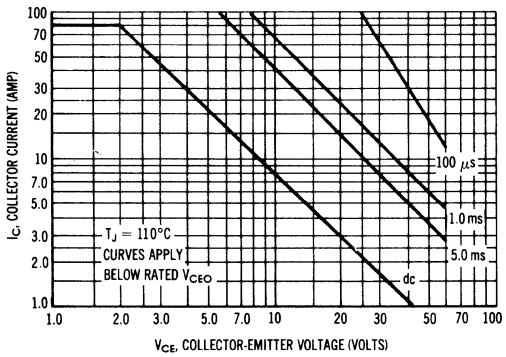


FIGURE 3 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 110°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} < 110°C$. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 4 — SWITCHING TEST CIRCUIT

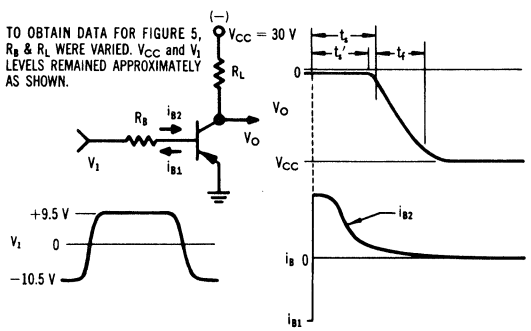
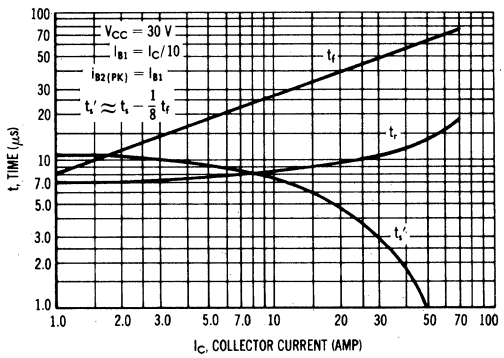


FIGURE 5 — SWITCHING TIMES



The switching performance of this transistor is determined primarily by the gain-bandwidth product, f_T*, and the behavior of the base-spreading resistance, $r_{b'}$.

In the case of rise time, the base-spreading resistance plays a small part, and the test circuit delivers a constant current step of turn-on current to the transistor (I_{B1}). Therefore, the curve of t_r on Figure 5 follows theory closely, i.e.:

$$t_r \approx 0.8 \frac{I_C}{I_{B1}} \cdot \frac{1}{2\pi f_T}$$

From the curve, it can be seen that f_T is roughly constant with current; using the equation, its large signal value can be calculated to be approximately 120 kHz at the 20-Amp level. A lower supply voltage will increase rise time slightly.

Turn-off time is slow because of conductivity modulation which occurs in the base region. When the transistor is held "on" in saturation, the base region becomes filled with excess charge; i.e., charge in excess of that necessary to sustain the circuit limited value of I_C. As a result, the base resistivity and consequently $r_{b'}$ become very low. During turn off, as the excess charge is reduced, the accompanying increase in resistivity causes a marked reduction in the turn-off current, i_{B2}, as can be seen from the waveforms of Figure 4. During fall time, the i_{B2} current is very low causing an extended fall time.

Only a slight improvement in turn-off performance is achieved with a "speed-up" capacitor placed across R_B. This unusual behavior occurs because $r_{b'}$ limits the amount of reverse current which can be achieved. Also, it seems evident that $r_{b'}$ increases with applied reverse current, so that efforts to speed up the turn-off behavior are somewhat futile.

In most applications, switching time will be close to the values shown on Figure 5. Delay time is not shown as it is negligible in comparison to the other times.

* $f_T \approx f_{\alpha e} \times h_{fe}$

TYPICAL DC CHARACTERISTICS

FIGURE 6 — DC CURRENT GAIN

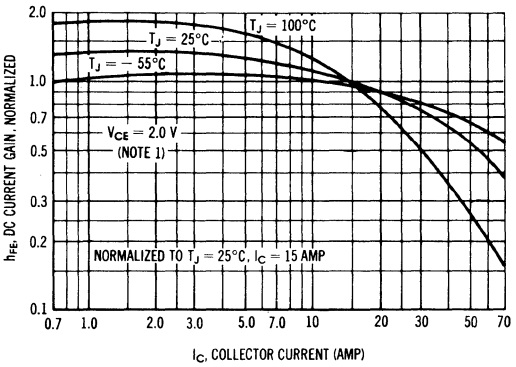


FIGURE 7 — COLLECTOR SATURATION REGION

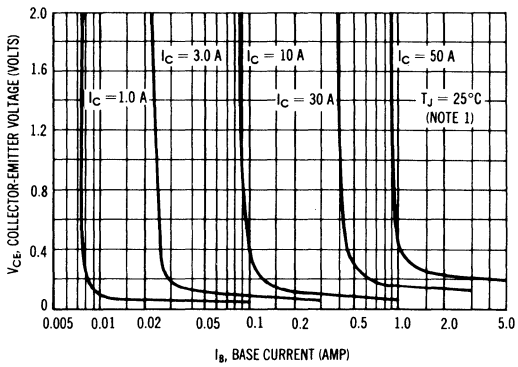


FIGURE 8 — EFFECTS OF BASE-EMITTER RESISTANCE

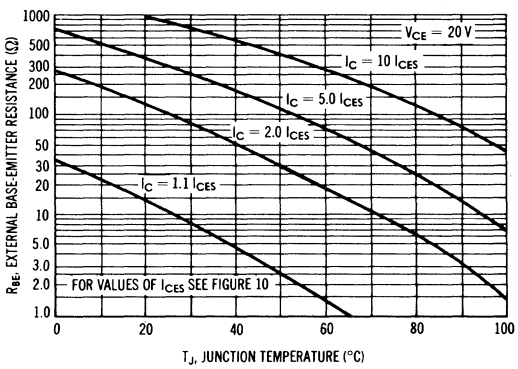


FIGURE 9 — "ON" VOLTAGES

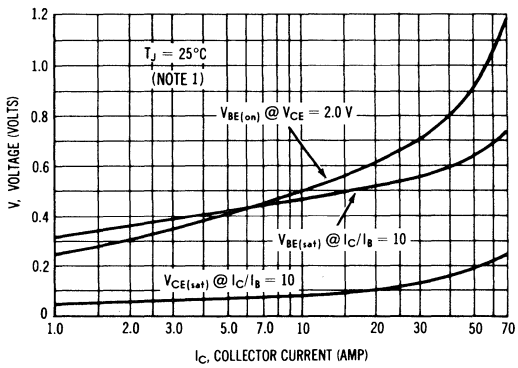
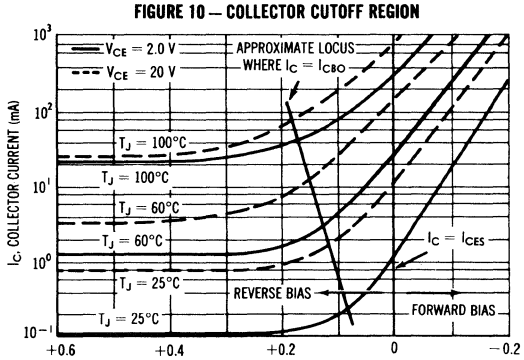


FIGURE 10 — COLLECTOR CUTOFF REGION



NOTE 1: Data is obtained from pulse tests and adjusted to nullify the effect of I_{CBO}.

FIGURE 11 — TEMPERATURE COEFFICIENTS