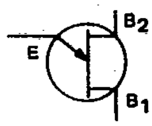
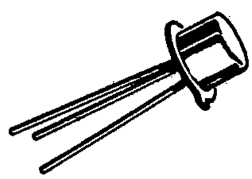
NOT RECOMMENDED FOR NEW DESIGNS

PN Unijunction Transistors
Silicon Unijunction Transistors

2N4851 thru 2N4853

PN UJTs





CASE 22A-01
STYLE 1

. . . designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits.

- Low Peak-Point Current — I_P = 0.4 μA Max
- Low Emitter Reverse Current — I_{EO} = 50 nA Max
- Fast Switching

***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Power Dissipation, Note 1	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current, Note 2	i_e	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage, Note 3	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

*Indicates JEDEC Registered Data.
Notes: 1. Derate 3 mW/°C increase in ambient temperature.
2. Duty cycle ≤ 1%, PRR = (see Figure 6).
3. Based upon power dissipation at T_A = 25°C.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Rating		Fig. No.	Symbol	Min	Typ	Max	Unit
*Intrinsic Standoff Ratio, Note 1 (V_{B2B1} = 10 V)	2N4851 2N4852, 2N4853	4, 8	η	0.56 0.70	— —	0.75 0.85	—
*Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)		11, 12	r_{BB}	4.7	—	9.1	k ohms
*Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = −65 to +125°C)		12	α_{BB}	0.2	—	0.8	%/°C
Emitter Saturation Voltage, Note 2 (V_{B2B1} = 10 V, I_E = 50 mA)			$V_{EB1(sat)}$	—	2.5	—	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)			$I_{B2(mod)}$	—	15	—	mA
*Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	2N4851, 2N4852 2N4853	7	I_{EB2O}	— —	— —	0.1 0.05	μA
*Peak-Point Emitter Current (V_{B2B1} = 25 V)	2N4851, 2N4852 2N4853	9, 10	I_P	— —	— —	2 0.4	μA
*Valley-Point Current, Note 2 (V_{B2B1} = 20 V, R_{B2} = 100 ohms)	2N4851 2N4852 2N4853	13, 14	I_V	2 4 6	— — —	— — —	mA
*Base-One Peak Pulse Voltage	2N4851 2N4852 2N4853	3, 17	V_{OB1}	3 5 6	— — —	— — —	Volts
*Maximum Frequency of Oscillation		5	$f_{(max)}$	—	0.25	—	MHz

3

*Indicates JEDEC Registered Data.

Notes: 1. η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.

2. Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2% to avoid internal heating, which may result in erroneous readings.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

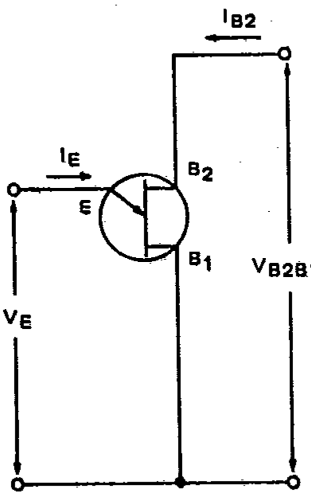


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES

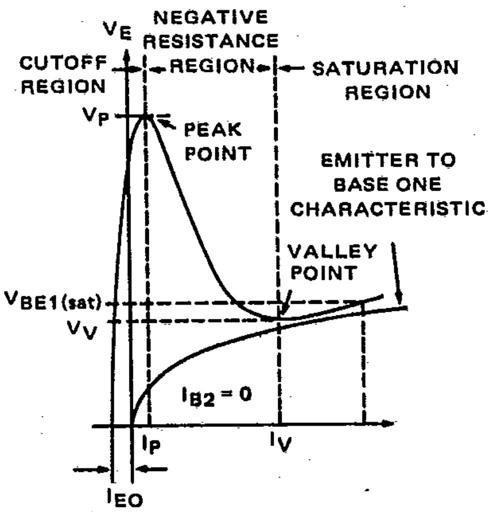


FIGURE 3 — V_{OB1} TEST CIRCUIT

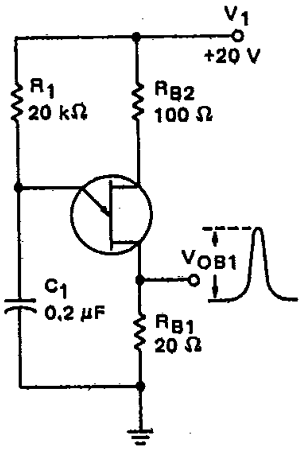
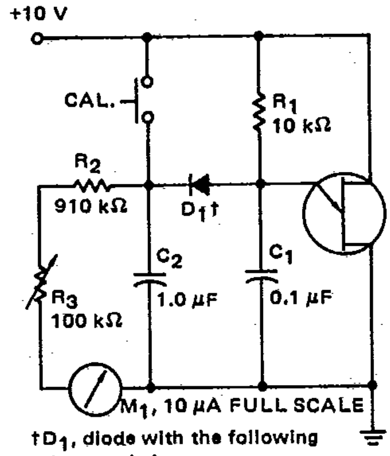


FIGURE 4 — η TEST CIRCUIT



†D_1, diode with the following characteristics:

$V_F = 0.49$ V @ $I_F = 10$ µA
$I_R \leq 2.0$ µA @ $V_R = 20$ V

FIGURE 5 — $f_{(max)}$ TEST CIRCUIT

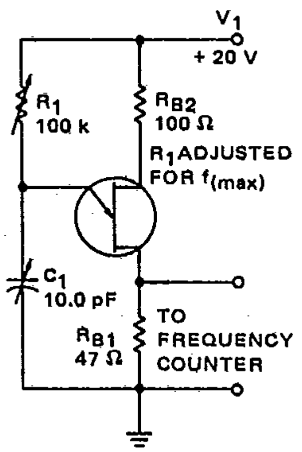
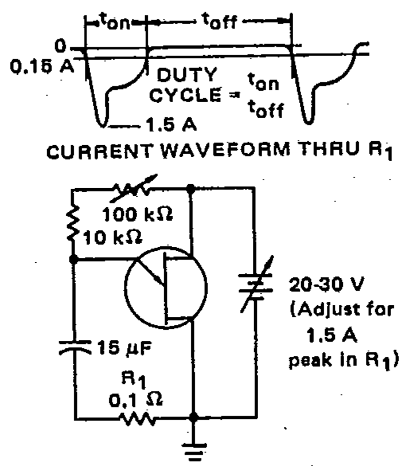


FIGURE 6 — PRR TEST CIRCUIT AND WAVEFORM

DUTY CYCLE ≤ 1%, PRR ≤ 10 pps



TYPICAL CHARACTERISTICS

FIGURE 7 — EMITTER REVERSE CURRENT

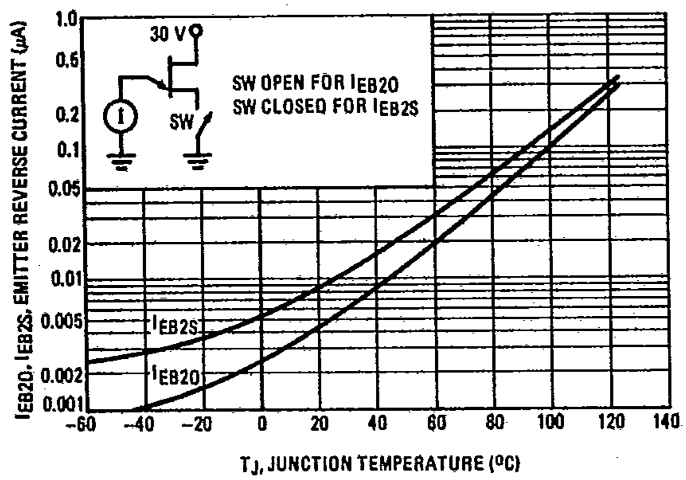
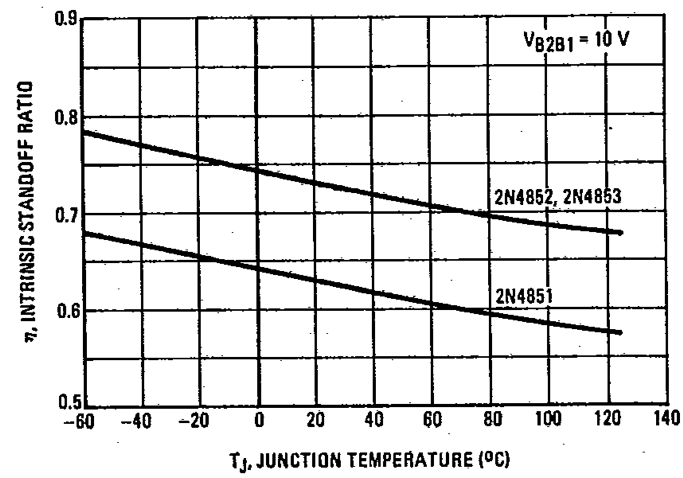


FIGURE 8 — INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 9 — EFFECT OF VOLTAGE

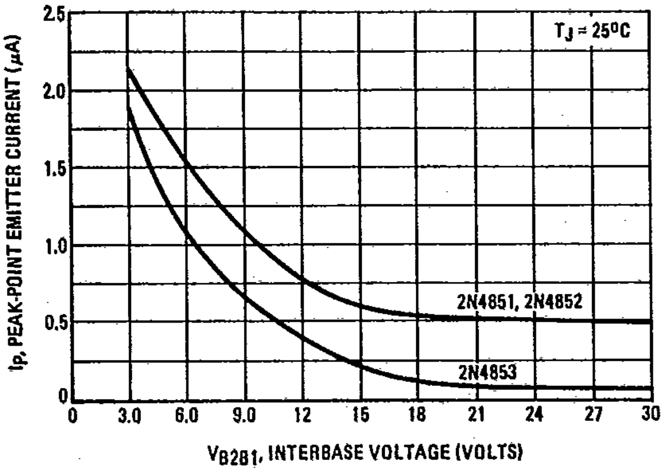
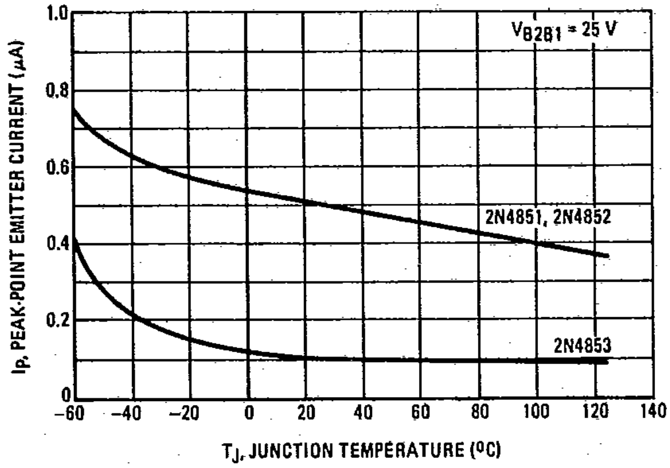


FIGURE 10 — EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 11 — EFFECT OF VOLTAGE

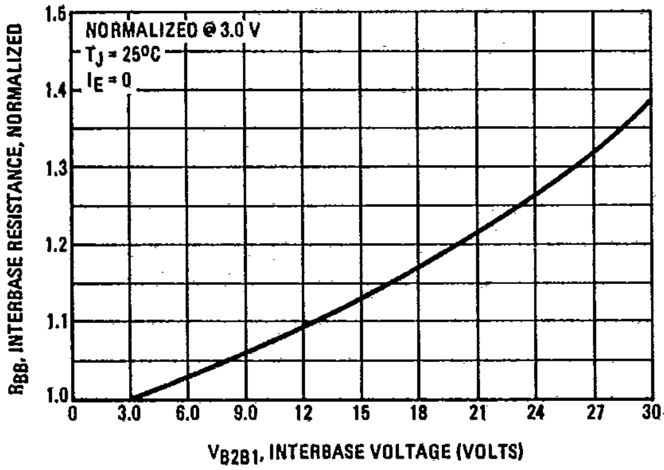
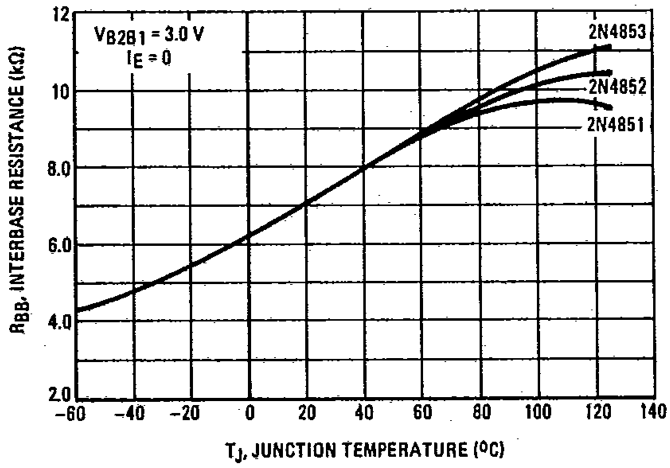


FIGURE 12 — EFFECT OF TEMPERATURE



TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 13 — EFFECT OF VOLTAGE

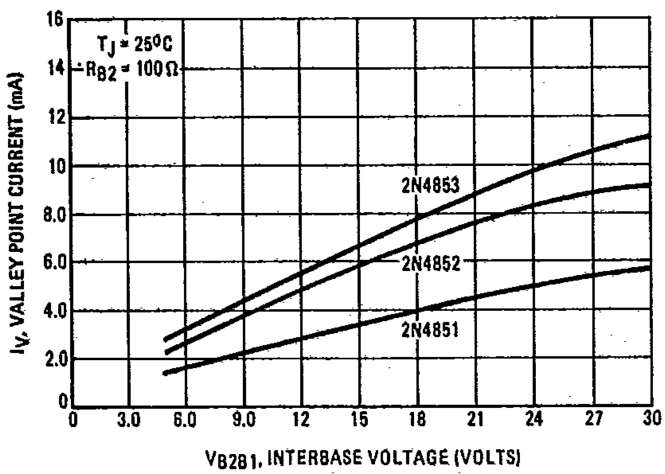
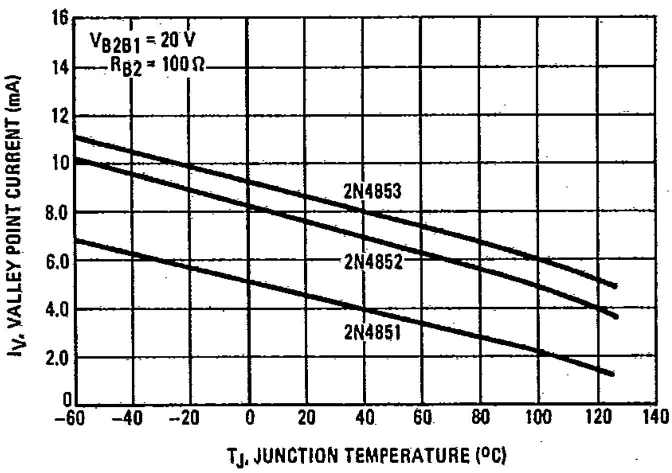


FIGURE 14 — EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 15 – EFFECT OF VOLTAGE

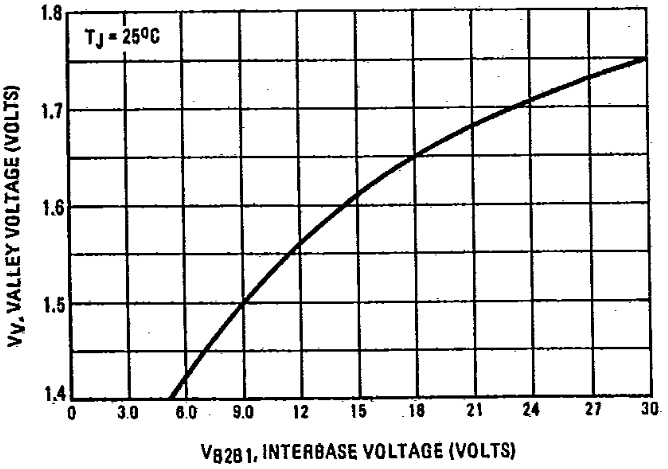


FIGURE 16 – EFFECT OF TEMPERATURE

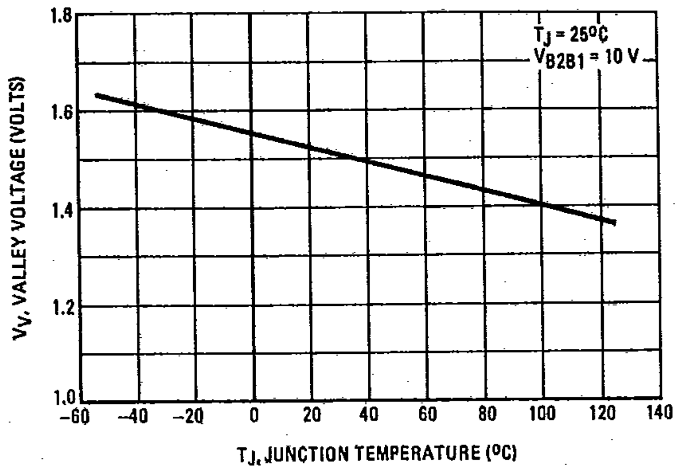


FIGURE 17 – OUTPUT VOLTAGE