n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

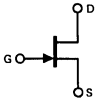
Siliconix

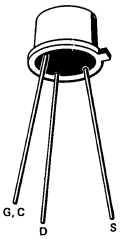
Performance Curves NCB
See Section 4

BENEFITS

- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856A, 59A)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF
- High Speed
  $t_{ON} < 8$ ns

TO-18
See Section 6





*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage,
2N4856A-58A . . . . . −40 V
Reverse Gate-Drain or Gate-Source Voltage,
2N4859A-61A . . . . . −30 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

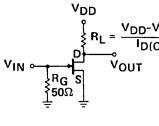
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4856A 2N4859A Min	2N4856A 2N4859A Max	2N4857A 2N4860A Min	2N4857A 2N4860A Max	2N4858A 2N4861A Min	2N4858A 2N4861A Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	2N4856A-58A	−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2			2N4859A-61A	−30		−30		−30				
3		I_{GSS} Gate Reverse Current	2N4856A-58A		−250		−250		−250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4					−500		−500		−500	nA		150°C
5			2N4859A-61A		−250		−250		−250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6					−500		−500		−500	nA		150°C
7		$I_{D(off)}$ Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8					500		500		500	nA		150°C
9		$V_{GS(off)}$ Gate-Source Cutoff Voltage		−4	−10	−2	−6	−0.8	−4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS} Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$ Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D =$ ( )	
12	DYN	$r_{ds(on)}$ Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss} Common-Source Input Capacitance			10		10		10	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss} Common-Source Reverse Transfer Capacitance			4		3.5		3.5			
15	SWITCHING	$t_{d(on)}$ Turn-ON Delay Time			5 (20) [−10]		6 (10) [−6]		8 (5) [−4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} =$ ( ), $V_{GS(off)} =$ [ ], $R_L =$ 464 Ω, 2N4856A, 59A; 953 Ω, 2N4857A, 60A; 1910 Ω, 2N4858A, 61A	
16		t_r Rise Time			3 (20) [−10]		4 (10) [−6]		8 (5) [−4]	ns (mA) [V]		
17		t_{off} Turn-OFF Time			20 (20) [−10]		40 (10) [−6]		80 (5) [−4]	ns (mA) [V]		

NCB

*JEDEC registered data

NOTE:
1 Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF