2N4877 (SILICON)

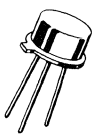
MEDIUM-POWER NPN SILICON TRANSISTOR

. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 4.0 Amp
- DC Current Gain Specified to 4 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-39 Case for Critical Space-Limited Applications.

4 AMPERE
POWER TRANSISTOR

NPN SILICON
60 VOLTS
10 WATTS



* MAXIMUM RATINGS

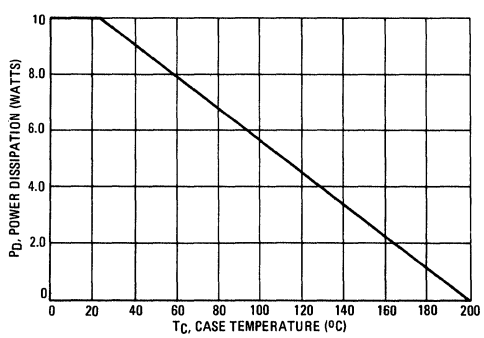
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	4.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 57.2	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data

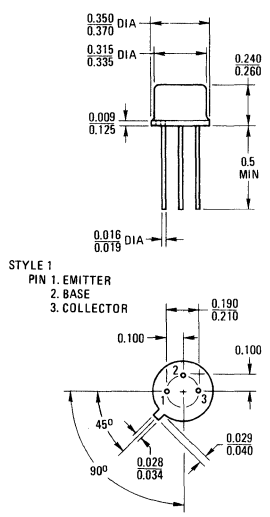
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. All limits are applicable and must be observed.



To convert inches to millimeters multiply by 25.4

All JEDEC dimensions and notes apply

CASE 79 (1)

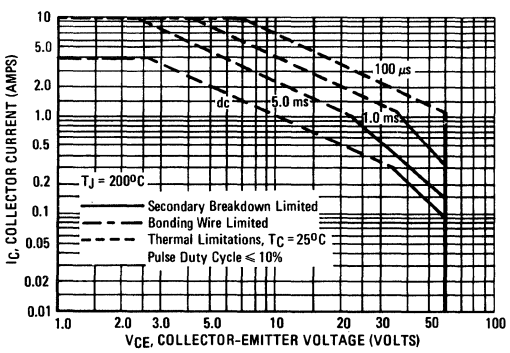
TO-39

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	–	100	μAdc
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)		–	1.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS(1)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	30	–	–
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)		20	100	
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc)	$V_{BE(sat)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	4.0	–	MHz
(I_C = 0.25 Adc, V_{CE} = 10 Vdc, f = 10 MHz)**		30	–	
SWITCHING CHARACTERISTICS				
Rise Time (V_{CC} = 25 Vdc, I_C = 4.0 Adc, I_{B1} = 0.4 Adc)	t_r	–	100	ns
Storage Time (V_{CC} = 25 Vdc, I_C = 4.0 Adc,	t_s	–	1.5	μs
Fall Time I_{B1} = I_{B2} = 0.4 Adc)	t_f	–	500	ns

*Indicates JEDEC Registered Data.
**Motorola guarantees this value in addition to JEDEC Registered Data.
Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 3 – SWITCHING TIME TEST CIRCUIT