p-channel JFETs designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

Performance Curves PSA/PSB See Section 4

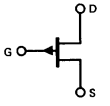
BENEFITS

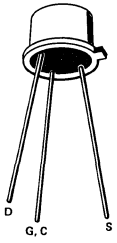
- Low Insertion Loss
  $r_{DS(on)} < 75\ \Omega$ (2N5018)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . .50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature (1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 6





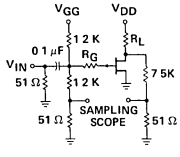
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5018 Min	2N5018 Max	2N5019 Min	2N5019 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		2		2	nA	$V_{GS} = 15$ V, $V_{DS} = 0$	
3		$I_{D(off)}$	Drain Cutoff Current		–10		–10	nA	$V_{DS} = -15$ V, $V_{GS} = 12$ V (2N5018)	
4					–10		–10	µA	$V_{GS} = 7$ V (2N5019)	150°C
5		I_{DGO}	Drain Reverse Current		–2		–2	nA	$V_{DG} = -15$ V, $I_S = 0$	
6					–3		–3	µA		150°C
7		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	$V_{DS} = -15$ V, $I_D = -1\ \mu A$	
8		I_{DSS}	Saturation Drain Current	–10		–5		mA	$V_{DS} = -20$ V, $V_{GS} = 0$	
9		$V_{DS(on)}$	Drain-Source ON Voltage		–0.5		–0.5	V	$V_{GS} = 0$, $I_D = -6$ mA (2N5018), $I_D = -3$ mA (2N5019)	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	$I_D = -1$ mA, $V_{GS} = 0$	
11		$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	$I_D = 0$, $V_{GS} = 0$	f = 1 kHz
12	DYN	C_{iss}	Common-Source Input Capacitance		45		45	pF	$V_{DS} = -15$ V, $V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		$V_{DS} = 0$, $V_{GS} = 12$ V (2N5018), $V_{GS} = 7$ V (2N5019)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	$V_{DD} = -6$ V, $V_{GS(on)} = 0$	
15		t_r	Rise Time		20		75			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		25			
17		t_f	Fall Time		50		100			

	$V_{GS(off)}$	$I_{D(on)}$	R_L
2N5018	12 V	–6 mA	910 Ω
2N5019	7 V	–3 mA	1.8K Ω

*JEDEC registered data

NOTE:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged



PSA/PSB

INPUT PULSE	SAMPLING SCOPE
RISE TIME < 1 ns	RISE TIME 0 4 ns
FALL TIME < 1 ns	INPUT RESISTANCE 10 MΩ
PULSE WIDTH 100 ns	INPUT CAPACITANCE 1 5 pF
REPETITION RATE 1 MHz	