2N5070 (SILICON)

The RF Line

NPN SILICON RF POWER TRANSISTORS

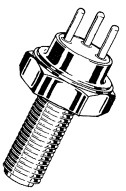
. . . designed primarily for applications as a high-power linear amplifier from 2.0 to 75 MHz.

- Optimized for Operation from a 28-Volt Supply
- Power Out @ 28 Vdc, 30 MHz – 25 W (PEP)
- Intermodulation Distortion at 25 W (PEP)
  IMD = 30 dB (Max)
- Isothermal-Resistor Design Results in Rugged Device

25 W (PEP) – 30 MHz

RF POWER TRANSISTOR

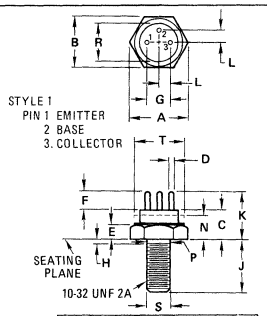
NPN SILICON



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous Peak	I_C	3.3 10	Adc
Base Current – Continuous	I_B	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	70 400	Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.57	13.08	0.495	0.515
B	10.77	11.10	0.424	0.437
C	5.46	8.13	0.215	0.320
D	0.762	1.17	0.030	0.046
E	2.29	3.43	0.090	0.135
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	9.53	11.56	0.375	0.455
K	9.02	12.19	0.355	0.480
L	2.29	2.79	0.090	0.110
N	–	4.19	–	0.165
P	4.14	4.80	0.163	0.189
R	8.13	9.14	0.320	0.360
T	9.14	11.10	0.360	0.437

All JEDEC dimensions and notes apply

Emitter connected to case

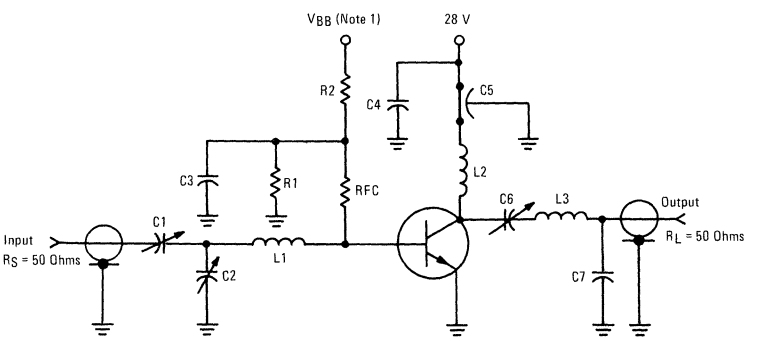
CASE 36
TO-60

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	–	Vdc
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, R_{BE} = 5.0 ohms)	$V_{CER(sus)}$	40	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	5.0	mAdc
Collector Cutoff Current	I_{CEX}			mAdc
(V_{CE} = 60 Vdc, V_{BE} = −1.5 Vdc)		–	10	
(V_{CE} = 60 Vdc, V_{BE} = −1.5 Vdc, T_C = 150°C)		–	10	
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	I_{CBO}	–	10	mAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	10	mAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		10	100	
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)		10	100	
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product(2) (I_C = 1.0 Adc, V_{CE} = 15 Vdc, f = 50 MHz)	f_T	100	–	MHz
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	85	pF
FUNCTIONAL TEST (Figure 1)				
Power Input (P_{out} = 25 W (PEP), Z_G = 50 Ohms, V_{CE} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	P_{in}	–	1.25	Watt (PEP)
Collector Efficiency (P_{out} = 25 W (PEP), Z_G = 50 Ohms, V_{CE} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	η	40	–	%
Intermodulation Distortion (P_{out} = 25 W (PEP), Z_G = 50 Ohms, V_{CE} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	IMD	–	-30	dB

*Indicates JEDEC Registered Data.
(1)Pulsed thru 25 mH Inductor, Duty Cycle = 50%, Repetition Rate = 60 Hz.
(2)f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – 30 MHz LINEAR TEST CIRCUIT



L1: 3 Turns No. 12 AWG, 1/4" I.D., 1/2" Long
L2: 6 Turns No. 14 AWG, 3/8" I.D., 3/4" Long
L3: 5 Turns No. 10 AWG, 3/4" I.D., 3/4" Long
C1: 140-680 pF, ARCO 468 or Equivalent
C2: 170-780 pF, ARCO 469 or Equivalent
C3: 0.05 μF, Ceramic Capacitor
C4: 0.1 μF, Ceramic Capacitor
C5: 1000 pF, Feedthrough Capacitor
C6: 24-200 pF, ARCO 425, or Equivalent
C7: 32-250 pF, ARCO 426, or Equivalent
Q: 2N5070
R1: 1.0 Ω, 5.0 W
R2: 50 Ohms, 25 W
RFC: 350 Ferrite Choke, Ferroxcube* #VK200 01-03B, or Equivalent

*Ferroxcube Corp. of America, Saugerties, N. Y.

Note 1: Adjust V_{BB} for a collector quiescent current of 20 mA with no RF input signal.

FIGURE 2 – LINEAR OUTPUT POWER versus FREQUENCY

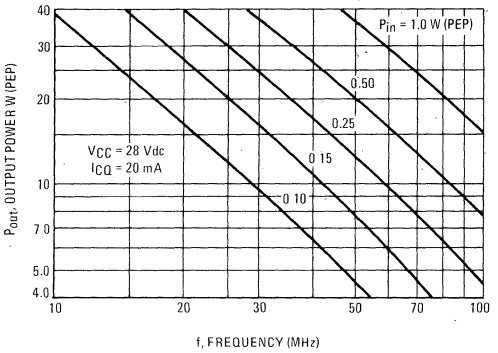


FIGURE 3 – TYPICAL OUTPUT POWER versus INPUT POWER

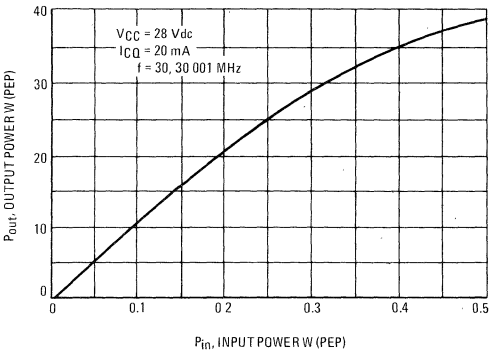


FIGURE 4 – TYPICAL OUTPUT POWER versus INPUT POWER

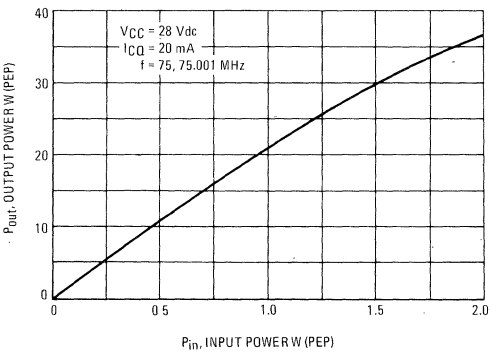
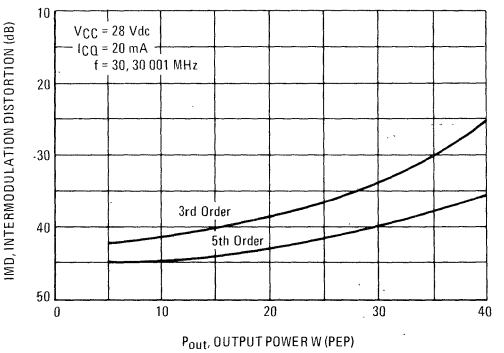


FIGURE 5 – TYPICAL INTERMODULATION DISTORTION versus OUTPUT POWER



LINEAR OUTPUT POWER versus SUPPLY VOLTAGE

FIGURE 6 – f = 30 MHz

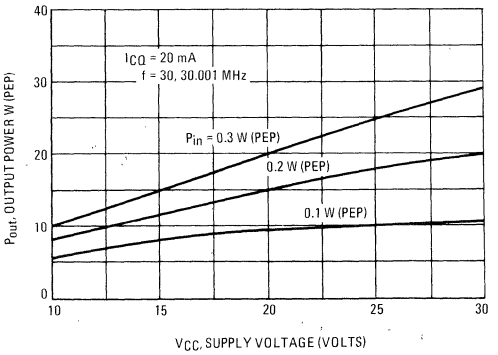


FIGURE 7 – IMD = -30 dB

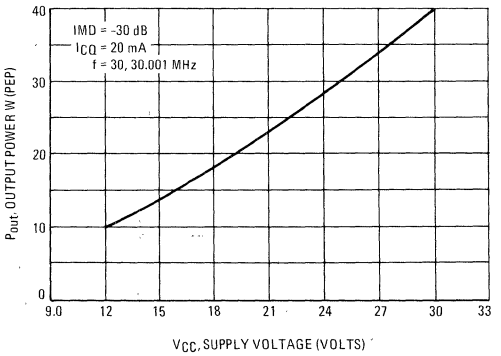


FIGURE 8 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

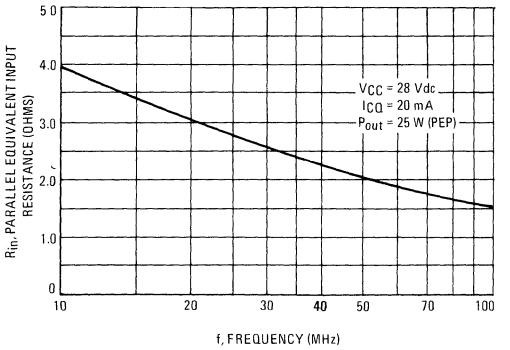


FIGURE 9 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

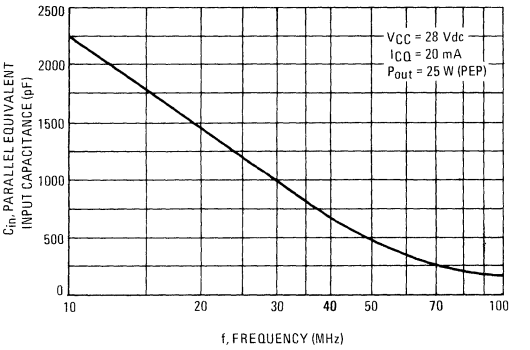


FIGURE 10 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

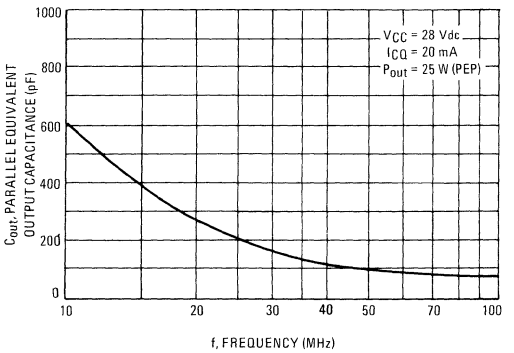
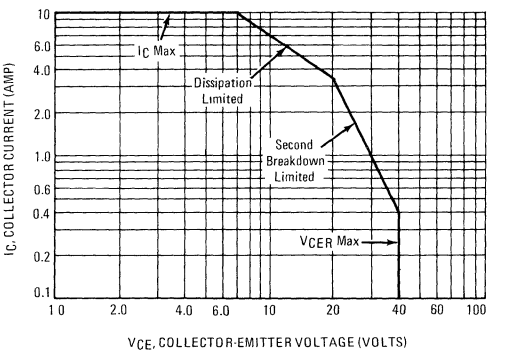


FIGURE 11 – DC SAFE OPERATING AREA



APPLICATIONS INFORMATION

The 2N5070 transistor is designed for linear power amplifier operation in the HF/VHF region (2 to 75 MHz). It features guaranteed linear amplifier performance rather than the conventional performance demonstrated in a class C* amplifier.

Class C operation is inherently non-linear, but in many power amplifier applications non-linear operation does not present major problems. With a single frequency driving signal, the only spurious signals generated are harmonics and these can be suppressed in the amplifier tuned networks and output filter.

For single sideband (SSB), low level amplitude modulation (AM), and other types of complex signals, class C operation is generally not satisfactory. For instance, when a signal contains multiple frequencies at close spacings, odd-order non-linearities will generate spurious outputs which are within the passband of the tuned circuits and filters; therefore, the spurious outputs are not suppressed before they reach the antenna or other load. As a result, such complex signals require linear amplification if the amplified signal is to be free of spurious outputs.

A detailed analysis of spurious signals generated by non-linearities and linearity requirements of various applications is described in Chapter 12 of Reference 1.

The following discussion concerns itself with a detailed description of the 2N5070 characterization curves and general information on solid state linear power amplifier design.

The Two-Tone Test

The 2N5070 functional test specification consists of a linear power amplifier test with guaranteed limits on power output, gain, efficiency, and intermodulation distortion (IMD) output levels. A two-tone test signal is used with the test amplifier as shown in Figure 1.

The two-tone test is one of many methods commonly used for testing linear amplifier performance. This test involves driving the amplifier with two RF signals, of equal amplitude, separated in frequency from each other by approximately 1 kHz.

When a two-tone test signal consisting of frequencies f_1 and f_2 is passed through a non-linear amplifier, odd order non-linearities generate spurious signals near the desired carrier. The level of these spurious signals provides a measure of the degree of non-linearity of the amplifier. This type of non-linearity is called intermodulation distortion (IMD). The spurious signals generated by IMD are further classified according to the exponential order of the amplifier non-linearity, i.e., 3rd order IMD products, 5th order IMD products, etc. The 3rd and 5th order IMD products are usually the most significant encountered with linear power amplifiers. Data on both 3rd and 5th order IMD are included in the 2N5070 characterization.

Third order IMD generates spurious signals near the operating frequency at frequencies $2f_1 - f_2$ and $2f_2 - f_1$; and 5th order IMD spurious signals are at frequencies $3f_1 - 2f_2$ and $3f_2 - 2f_1$.

Specifications and Characterization

The two-tone functional amplifier test is performed in a manner identical to the conventional class C functional test with two exceptions: a two-frequency signal is used in place of a single frequency, and amplifier linearity is added to the items tested and specified.

The functional test procedure for the 2N5070 requires driving the test amplifier with a two frequency signal and measuring power output, gain, efficiency, and linearity.

Power output, gain, and efficiency measurement methods are the same for both linear and class C amplifiers.

Since a multiple frequency test signal has an instantaneous power level which varies with time, power levels are normally expressed in peak envelope power (PEP). This is the average power level of the envelope at its greatest amplitude point.

When the test signal consists of multiple signals with equal amplitudes and different frequencies, the relationship of average power and PEP is given by the following expression:

$$\text{Average power} = \frac{\text{PEP}}{N}$$

where N = the number of input frequencies.

Therefore, when measuring the power level of a standard two-tone test signal, a true average reading power meter will indicate 1/2 the PEP of the signal.

Linearity is tested by measuring the amplitudes of the 3rd and 5th order IMD products. The ratio of one of the 3rd order products to one of the two desired frequencies is then expressed as a power ratio in decibels (dB). This is repeated for the 5th order products. The smaller of these two ratios (usually the 3rd order) is then included in the electrical characteristics specification as intermodulation distortion ratio (IMD).

2N5070 Performance Curves

Figures 2 through 4 show typical power output and gain characteristics versus frequency and/or input power. These curves are similar to those found on other RF power transistor data sheets with one exception, a two-frequency test signal was used rather than a single frequency signal.

The curves shown in Figure 5 are unique to transistors characterized for linear power amplifier service and show the typical IMD levels versus power output.

The 2N5070 features guaranteed IMD performance at the -30 dB level. However, the designer may desire IMD greater or less than -30 dB for a particular application. Figure 5 provides data on IMD levels that can be expected as a function of output power.

Figure 6 shows the variation in gain with dc supply voltage and provide data on gain only. It does not include information on IMD ratio.

Figure 7 reflects the power output that can be obtained at a fixed IMD ratio for operation with dc supply voltages other than 28 Vdc.

Figures 8 through 10 show the large signal impedance characteristics of the 2N5070. These are similar to curves shown on other Motorola data sheets except a two-frequency test signal was used rather than a single frequency signal.

It must be stressed that the data shown in Figures 8 through 10 do not represent y, z, h, s, or any standard two-port parameter set. The actual transistor impedance levels during normal operation in an amplifier are given. For a detailed discussion of RF power transistor large signal impedance, see Reference 2.

Linear Amplifier Design

The following is a discussion of some general design considerations for solid-state linear power amplifiers. While this is not a detailed analysis of linear amplifier design, some general guidelines are provided.

The major difference between linear power amplifiers and class C power amplifiers is in the dc bias circuitry. As stated in the introduction, class C operation usually involves a collector dc supply as

APPLICATIONS INFORMATION (continued)

the only bias voltage with $V_E = V_B = 0$. The collector current is zero until the input RF signal turns the transistor "on".

In contrast, a linear amplifier is normally operated with forward bias and some collector current flowing when no signal is present.

The magnitude of no-signal collector current and the bias circuitry may vary with the application. Optimum no-signal collector current for the 2N5070 was found to be approximately 20 mA.

The key to bias circuitry for good linearity lies in maintaining the base-emitter dc voltage relatively constant as the RF signal amplitude varies. The inherent nature of a forward-biased RF power transistor is to bias itself "off" with increasing RF drive signal. Therefore, a constant voltage source is required for base voltage.

Temperature effects also complicate the situation, since V_{BE} decreases with increasing temperature.

A simple solution to the bias problem involves the use of a forward-biased diode mounted on the transistor heat sink for thermal coupling to the transistor. A large capacitor (several hundred microfarads) in parallel with the diode helps maintain a constant V_{BE} with RF drive and improves linearity, while the diode provides temperature compensation to prevent thermal runaway. It is also possible to use complex active circuitry for biasing, and some rather exotic schemes have been developed to provide the same results.

Another important consideration is the collector-output network. Normally, a network with low impedance to ground for harmonics provides better linearity than a network with high harmonic impedances; therefore, some experimentation with network configuration is in order. Proper impedance matching remains the primary factor in both input and output network design. Further, it must also be stressed that the collector load impedance should be designed for the PEP, not the average power output. See Chapter 13 of Reference 1 for a detailed discussion of network design considerations.

Feedback may also be employed to improve linearity and may take the form of either neutralization or negative RF feedback. The possibilities here are limited only by the designer's imagination. Of course, negative RF feedback involves a decrease in gain to improve linearity.

REFERENCES

1. Pappenfus, Bruene, Schoenike, "Single Sideband Principles and Circuits", McGraw-Hill.
2. Hejhall, "Systemizing RF Power Amplifier Design", Motorola Semiconductor Products Inc., Application Note AN-282A.

•"Class C", as used here refers to operation with the no signal conditions $I_C = 0$, and $V_{BE} = 0$, and a theoretical conduction angle of less than 180^o, even though the actual conduction angle may be more than 180^o.