RCA
Solid State
Division

RF Power Transistors

2N5090

JEDEC TO-60

High-Power Silicon N-P-N Overlay Transistor

High-Gain Type for Class A, B, or C Operation in VHF/UHF Circuits

Features:

- **Maximum safe-area-of-operation curve**
- **1.2 W (min.) output at 400 MHz (7.8 dB gain)**
- **1.6 W (typ.) output at 175 MHz (12 dB gain)**
- **Hermetic stud-type package**
- **All electrodes isolated from stud**

RCA-2N5090● is an epitaxial silicon n-p-n planar transistor employing the RCA-developed "overlay" emitter-electrode design. It is intended for rf amplifier, frequency-multiplier, and oscillator service in vhf and uhf communications equipment.

The overlay structure contains many isolated emitter sites connected in parallel by means of a diffused grid structure and a deposited metal overlay. The overlay design provides a very high emitter-periphery-to-emitter-area ratio and results in low output capacitance, high rf-current-handling capability, and high power gain.

●Formerly RCA Dev. No.TA7146.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10Ω	V_{CER}	55	V
* With base open	V_{CEO}	30	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	0.4	A
*CONTINUOUS BASE CURRENT	I_B	0.4	A
*TRANSISTOR DISSIPATION	P_T		
At case temperatures up to 100°C		4	W
At case temperatures above 100°C. . Derate linearly at 0.04 W/°C			
*TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to +200	°C
*LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/16 in. (1.58 mm) from insulating wafer for 10 s max.		230	°C

*In accordance with JEDEC registration data format JS-6 RDF-3.

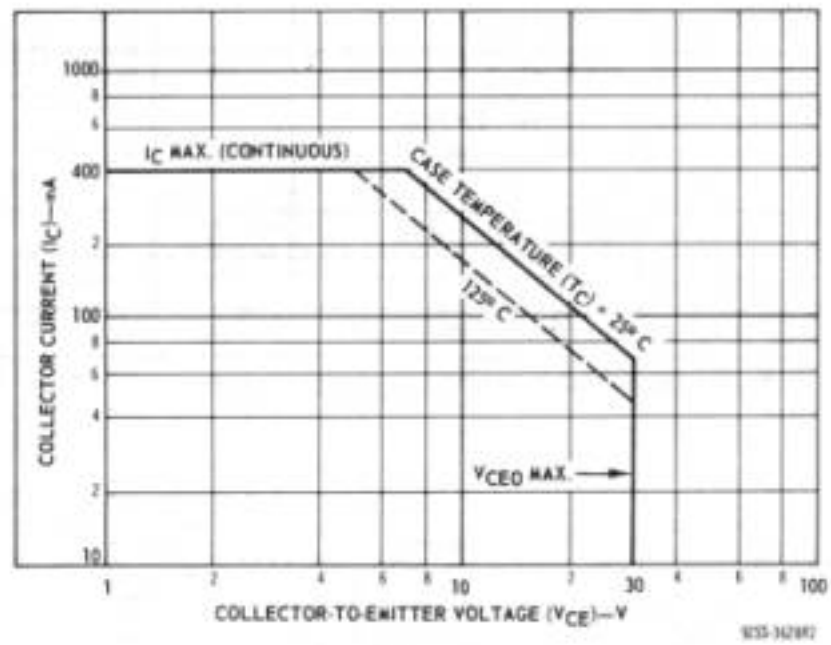


Fig.1—Safe area for dc operation.

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector Voltage-V	DC Base Voltage-V	DC Current mA					
			V_{CE}	V_{BE}	I_E	I_B	I_C	MIN.	MAX.	
*	Collector-Cutoff Current: With base open	I_{CEO}	28			0		–	0.02	mA
	With base-emitter junction reverse-biased	I_{CEV}	55	−1.5				–	0.1	
	With base-emitter junction reversed-biased & T_C = 200°C		30	−1.5				–	5	
*	Emitter-Cutoff Current	I_{EBO}		3.5				–	0.1	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.1	55	–	V
*	Collector-to-Emitter Sustaining Voltage: With base-open	$V_{CEO(sus)}$				0	5	30	–	V
	With external base-to-emitter resistance (R_{BE}) = 10Ω	$V_{CER(sus)}$					5	55[a]	–	
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
*	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				20	100	–	1.0	V
*	DC Forward-Current Transfer Ratio	h_{FE}	5 5				360 50	5 10	– 200	
	Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$						–	25	°C/W

[a]Pulsed through a 25-mH inductor; duty factor = 0.05%.

DYNAMIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector Voltage V	Output Power (P_{OE}) W	Input Power (P_{IE}) W	Collector Current (I_C) mA	Frequency (f) MHz	MIN.	MAX.	
	Power Output (Class C amplifier, unneutralized) (See Fig. 2)	P_{OE}	V_{CC} = 28		0.2		400	1.2	–	W
	Gain-Bandwidth Product	f_T	V_{CE} = 15			50		500	–	MHz
*	Magnitude of Common Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio	$\lvert h_{fe} \rvert$	V_{CE} = 15			50		2.5	–	
*	Available Amplifier Signal Input Power	P_i		1.2			400	–	0.2	W
*	Collector Efficiency	η_C		1.2				45	–	%
*	Collector-to-Base Capacitance	C_{obo}	V_{CB} = 30				1	–	3.5	pF

*In accordance with JEDEC registration data format JS-6 RDF-3.

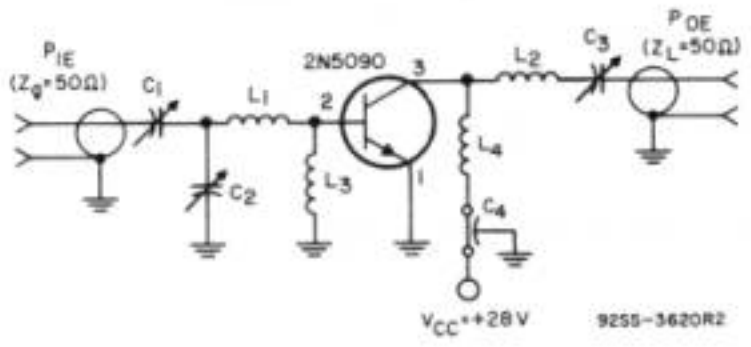


Fig.2–400-MHz rf amplifier for output power test.

C_1: 0.9-7 pF, ARCO 400, or equivalent
C_2, C_3: 1.5-20 pF, ARCO 402, or equivalent
C_4: 1,000 pF, feedthrough type
L_1: 2 turns No.18 wire, ¼ in. (6.35 mm) ID, 1/8 in. (3.17 mm) long
L_2: 3 turns No.16 wire, ¼ in. (6.35 mm) ID, 3/8 in. (9.52 mm) long
L_3: 0.1 μH, RFC
L_4: 2 turns No.18 wire, 1/8 in. (3.17 mm) ID, 1/8 in. (3.17 mm) long

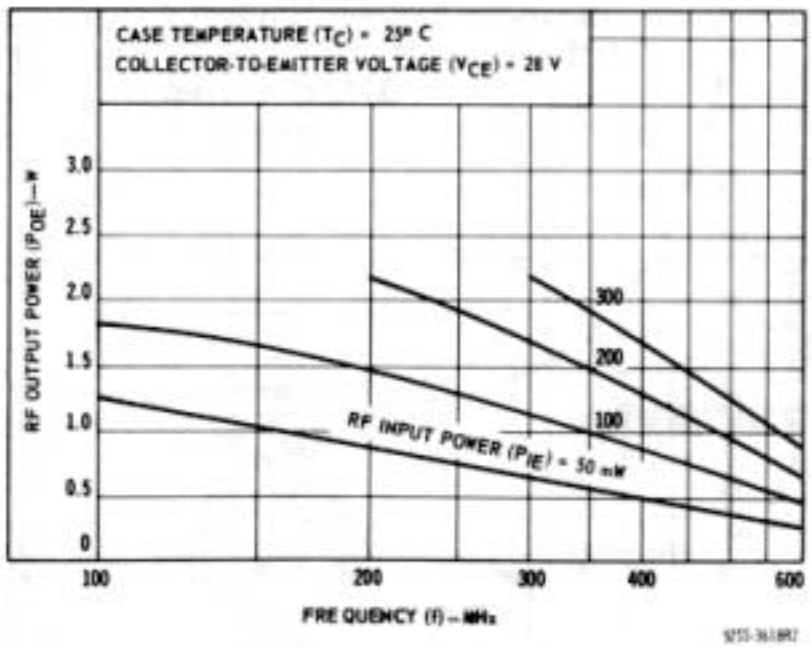


Fig.3—Typical output power vs. frequency.

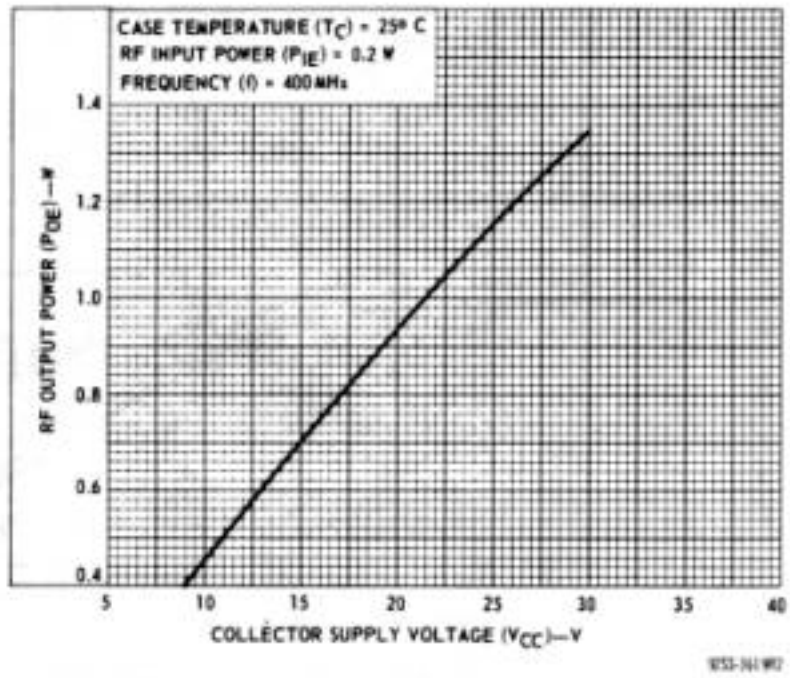


Fig.4—Typical output power vs. collector supply voltage.

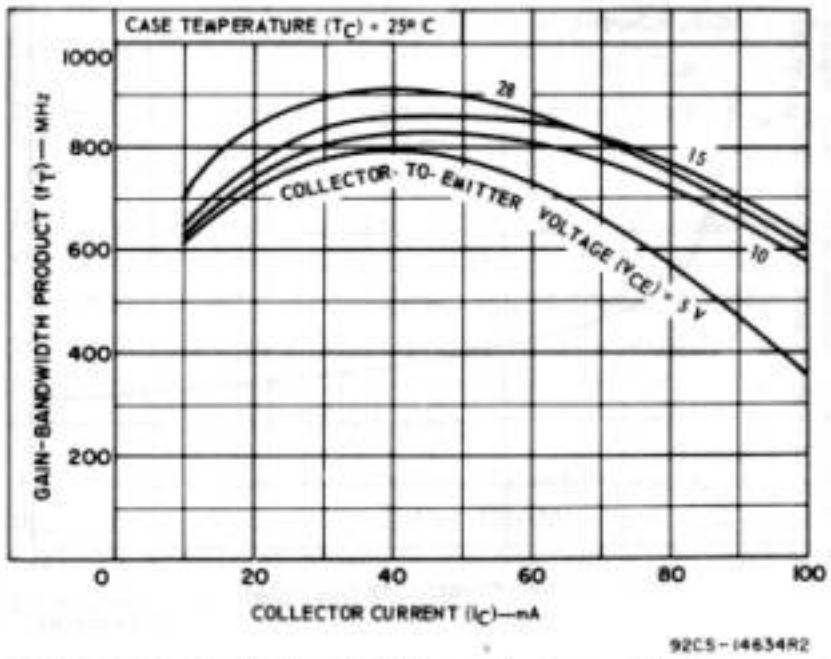


Fig.5—Typical gain-bandwidth product vs. collector current.

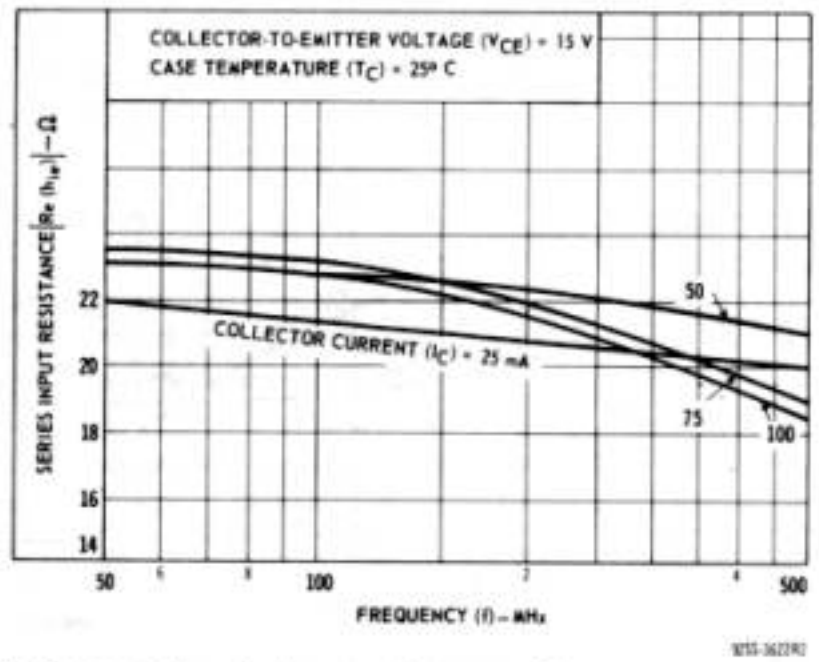


Fig.6—Typical series input resistance vs. frequency.

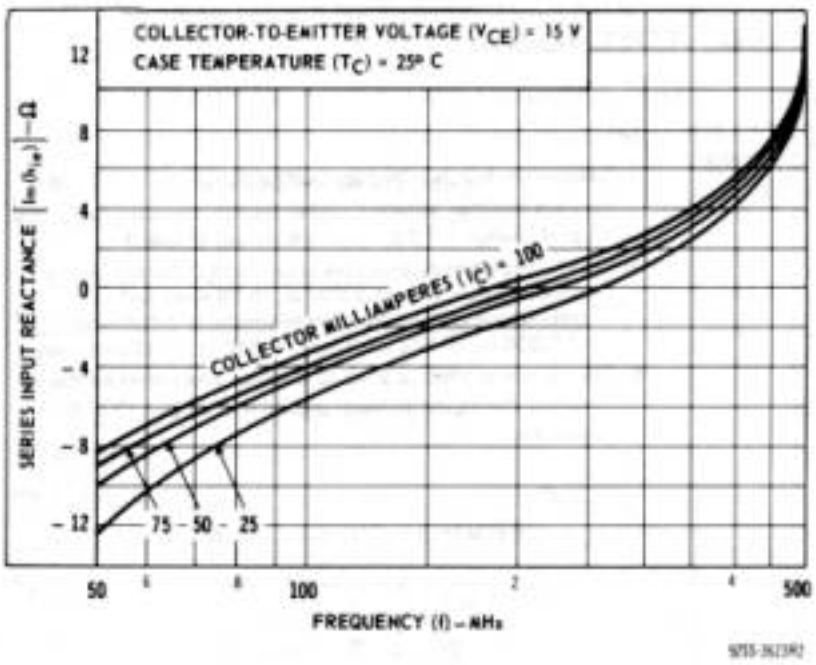


Fig.7—Typical series input reactance vs. frequency.

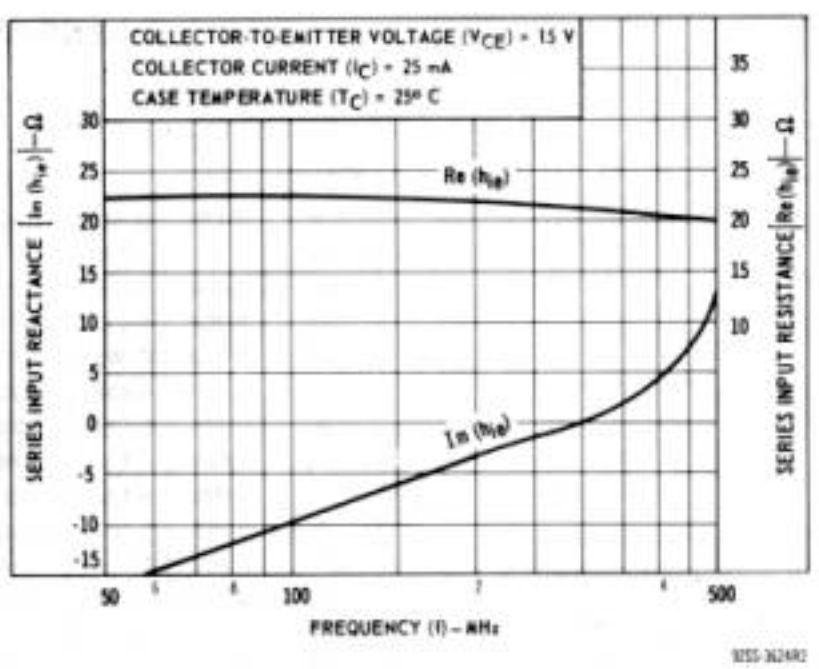


Fig.8—Typical series input resistance and reactance vs. frequency.

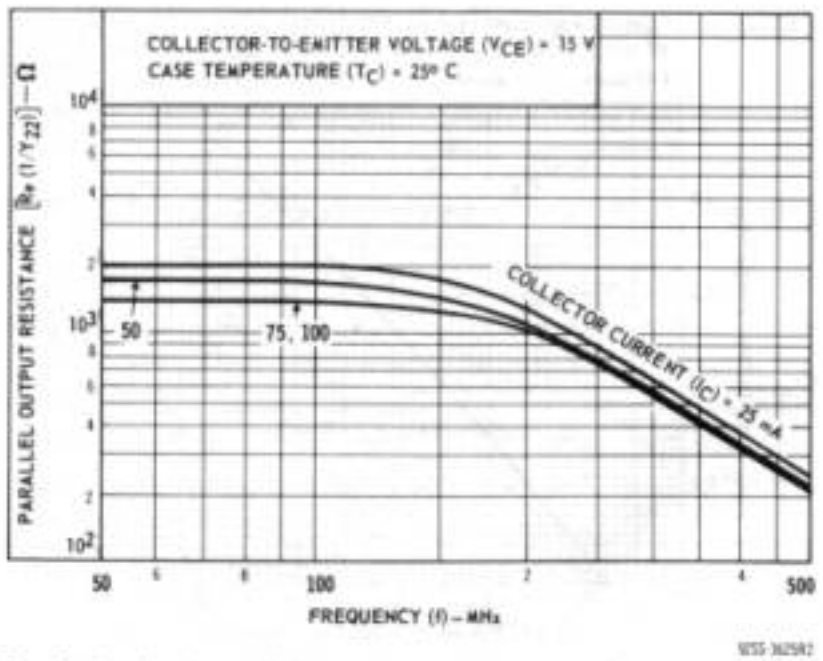


Fig.9—Typical parallel output resistance vs. frequency.

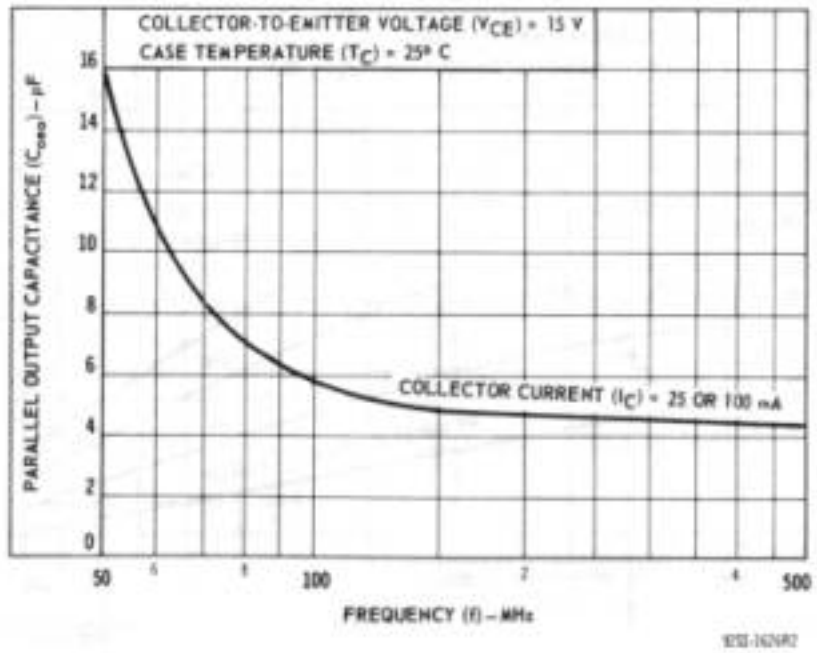


Fig.10—Typical parallel output capacitance vs. frequency.

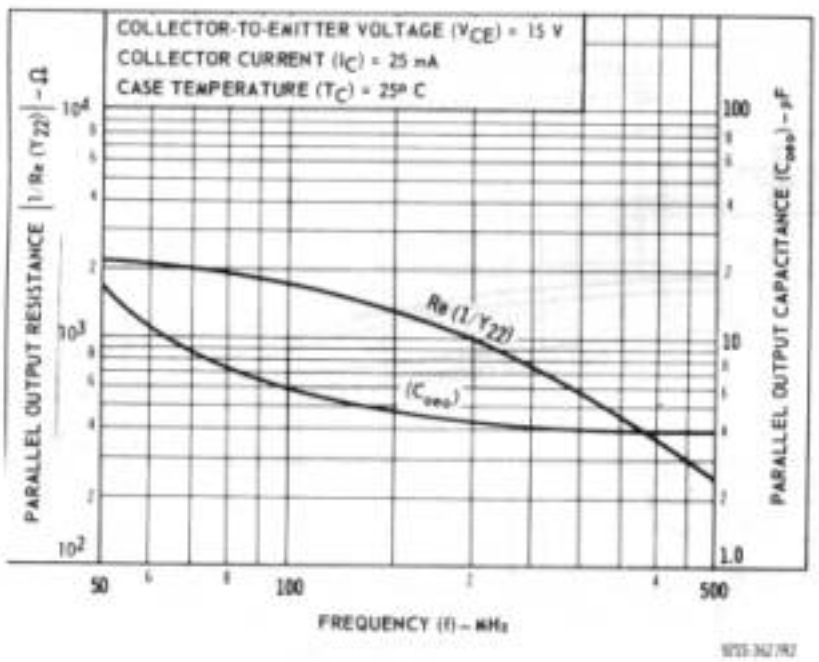


Fig.11—Typical parallel output resistance and capacitance vs. frequency.

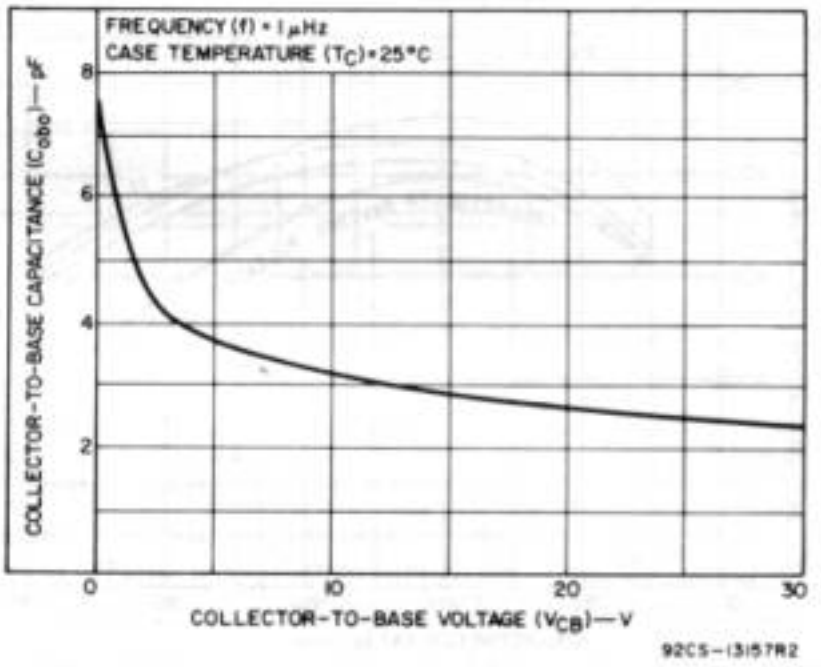
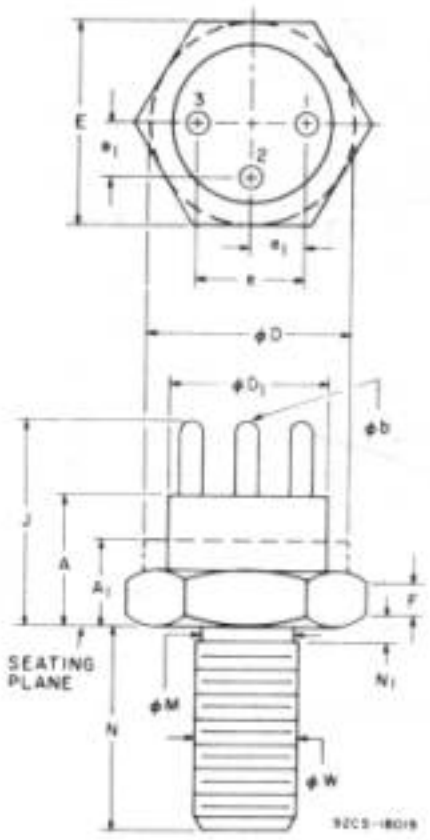


Fig.12—Typical variation of collector-to-base capacitance. with collector-to-base voltage.

DIMENSIONAL OUTLINE, JEDEC TO-60



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.215	0.320	5.46	8.13	
A_1	–	0.165	–	4.19	2
ϕb	0.030	0.046	0.762	1.17	4
ϕD	0.360	0.437	9.14	11.10	2
ϕD_1	0.320	0.360	8.13	9.14	
E	0.424	0.437	10.77	11.10	
e	0.185	0.215	4.70	5.46	
e_1	0.090	0.110	2.29	2.79	
F	0.090	0.135	2.29	3.43	1
J	0.355	0.480	9.02	12.19	
ϕM	0.163	0.189	4.14	4.80	
N	0.375	0.455	9.53	11.56	
N_1	–	0.078	–	1.98	
ϕW	0.1658	0.1697	4.212	4.310	3, 5

NOTES:

1. Dimension does not include sealing flanges
2. Package contour optional within dimensions specified
3. Pitch diameter – 10-32 UNF 2A thread (coated)
4. Pin spacing perimts insertion in any socket having a pin-circle diameter of 0.200 in. (5.08 mm) and contacts which will accommodate pins with a diameter of 0.030 in. (0.762 mm) min., 0.046 in. (1.17 mm) max.
5. The torque applied to a 10-32 hex nut assembled on the thread during installation should not exceed 12 inch-pounds.

TERMINAL CONNECTIONS

Pin No. 1 – Emitter
Pin No. 2 – Base
Pin No. 3 – Collector
Case–Isolated