

2N3902 & 2N5157



NPN High Power Silicon Transistors

Rev. V4

Features

- Available in JAN, JANTX, JANTXV per MIL-PRF-19500/371
- TO-3 (TO-204AA) Package
- Designed for Use in High Voltage Inverters, Converters, Switching Regulators and Line Operated Amplifiers



Electrical Characteristics ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Cutoff Current	$V_{CE} = 400 \text{ V dc}$, 2N3902 $V_{CE} = 500 \text{ V dc}$, 2N5157	I_{CEO}	$\mu\text{A dc}$	—	100 100
Collector - Emitter Cutoff Current	$V_{BE} = 1.5 \text{ V dc}$, $V_{CE} = 700 \text{ V dc}$	I_{CEX1}	$\mu\text{A dc}$	—	20
Collector - Emitter Cutoff Current	$V_{BE} = 5 \text{ V dc}$, 2N3902 $V_{BE} = 6 \text{ V dc}$, 2N5157	I_{EBO}	$\mu\text{A dc}$	—	200 200
Forward Current Transfer Ratio	$I_C = 0.5 \text{ A dc}$; $V_{CE} = 5 \text{ V dc}$ $I_C = 1.0 \text{ A dc}$; $V_{CE} = 5 \text{ V dc}$ $I_C = 2.5 \text{ A dc}$; $V_{CE} = 5 \text{ V dc}$ $I_C = 3.5 \text{ A dc}$; $V_{CE} = 5 \text{ V dc}$	h_{FE}	-	25 30 10 5	90
Collector - Emitter Saturation Voltage	$I_C = 1.0 \text{ A dc}$; $I_B = 0.1 \text{ A dc}$ $I_C = 3.5 \text{ A dc}$; $I_B = 0.7 \text{ A dc}$	$V_{CE(SAT)1}$ $V_{CE(SAT)2}$	V dc	—	0.8 2.5
Base - Emitter Saturation Voltage	$I_C = 1.0 \text{ A dc}$; $I_B = 0.1 \text{ A dc}$ $I_C = 3.5 \text{ A dc}$; $I_B = 0.7 \text{ A dc}$	$V_{BE(SAT)1}$ $V_{BE(SAT)2}$	V dc	—	1.5 2.0
Collector - Emitter Sustaining Voltage	$I_C = 100\text{mA dc}$ 2N3902 2N5157	$V_{CEO(SUS)}$	V dc	—	325 400
Collector - Emitter Cutoff Current	$T_A = +150^\circ\text{C}$ $V_{BE} = 1.5 \text{ V dc}$ $V_{CE} = 400 \text{ V dc}$, 2N3902 $V_{CE} = 500 \text{ V dc}$, 2N5157	I_{CEX2}	$\mu\text{A dc}$	—	300 300
Forward - Current Transfer Ratio	$T_A = -55^\circ\text{C}$ $V_{CE} = 5.0 \text{ V dc}$; $I_C = 1.0 \text{ A dc}$	h_{FE5}		10	—
Small-Signal Short-Circuit Forward Current Transfer Ratio	$I_C = 0.2 \text{ A dc}$; $V_{CE} = 10 \text{ Vdc}$; $f = 1 \text{ MHz}$	$ h_{fe} $	-	2.5	25
Output Capacitance	$V_{CB} = 10 \text{ Vdc}$; $I_E = 0$; $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{obo}	pF	—	250

(Continued next page)

2N3902 & 2N5157



NPN High Power Silicon Transistors

Rev. V4

Electrical Characteristics ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Switching Characteristics					
Turn-On Time	$V_{CC} = 125 \text{ Vdc}; I_C = 1.0 \text{ A dc}; I_{B1} = 0.1 \text{ A dc}$	t_{on}	μs	—	0.8
Turn-Off Time	$V_{CC} = 125 \text{ V dc}; I_C = 1.0 \text{ A dc}; I_{B1} = 0.1 \text{ A dc}; -I_{B2} = 0.50 \text{ A dc}$	t_{off}	μs	—	1.7
Safe Operating Area					
<p>DC Tests: $T_C = +25^\circ\text{C}$, 1 Cycle, $t = 1.0 \text{ s}$ (see Fig. 3 of MIL-PRF-19500/371)</p> <p>Test 1: $V_{CE} = 28.6 \text{ Vdc}, I_C = 3.5 \text{ A dc}$</p> <p>Test 2: $V_{CE} = 70 \text{ Vdc}, I_C = 1.43 \text{ A dc}$</p> <p>Test 3: $V_{CE} = 325 \text{ Vdc}, I_C = 55 \text{ mA dc}$, 2N3902 $V_{CE} = 400 \text{ Vdc}, I_C = 35 \text{ mA dc}$, 2N5157</p> <p>Switching Tests:</p> <p>Load Condition C (unclamped inductive load): $T_C = +25^\circ\text{C}$, duty cycle $<10\%$; $R_S = 0.1 \Omega$ (See Fig. 4 of MIL-PRF-19500/371)</p> <p>Test 1: $t_p =$ approximately 3 ms (vary to obtain I_C), $R_{BB1} = 20 \Omega$, $V_{BB1} = 10 \text{ Vdc}$; $R_{BB2} = 3 \text{ k}\Omega$, $V_{BB2} = 1.5 \text{ V dc}$, $V_{CC} = 50 \text{ Vdc}$, $I_C = 3.5 \text{ A dc}$, $L = 60 \text{ mH}$, $R = 3 \Omega$; $R_L < 14 \Omega$</p> <p>Test 2: $t_p =$ approximately 3 ms (vary to obtain I_C), $R_{BB1} = 100 \Omega$, $V_{BB1} = 10 \text{ Vdc}$; $R_{BB2} = 3 \text{ k}\Omega$, $V_{BB2} = 1.5 \text{ V dc}$, $I_C = 0.6 \text{ A dc}$, $V_{CC} = 50 \text{ Vdc}$, $L = 200 \text{ mH}$, $R = 8 \Omega$; $R_L < 83 \Omega$</p> <p>Load Condition (clamped inductive load): $T_C = +25^\circ\text{C}$, duty cycle $<10\%$ (See Fig. 5 of MIL-PRF-19500/371)</p> <p>Test 1: $t_p =$ approximately 30 ms (vary to obtain I_C), $R_S = 0.1 \Omega$, $R_{BB1} = 20 \Omega$, $V_{BB1} = 10 \text{ Vdc}$; $R_{BB2} = 100 \Omega$, $V_{BB2} = 1.5 \text{ Vdc}$, $V_{CC} = 50 \text{ Vdc}$, $I_C = 3.5 \text{ A dc}$, $L = 60 \text{ mH}$, $R = 3 \Omega$; $R_L < 0 \Omega$ (A suitable clamping circuit or diode can be used.) Clamp Voltage = 400 +0, -5 Vdc 2N3902 Clamp Voltage = 500 +0, -5 Vdc 2N5157 (Clamped voltage must be reached)</p>					

2N3902 & 2N5157



NPN High Power Silicon Transistors

Rev. V4

Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Ratings	Symbol	Value
Collector - Emitter Voltage 2N3902 2N5157	V_{CEO}	400 V dc 500 V dc
Emitter - Base Voltage 2N3902 2N5157	V_{EBO}	5 V dc 6 V dc
Collector - Base Voltage	V_{CBO}	700 V dc
Base Current	I_B	2.0 A dc
Collector Current	I_C	3.5 A dc
Total Power Dissipation	P_T	5 W
Total Power Dissipation $T_C = +25^\circ\text{C}$	$P_T^{(1)}$	125 W
Operating & Storage Temperature Range	T_J, T_{STG}	-65°C to $+200^\circ\text{C}$

Thermal Characteristics

Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Case ⁽²⁾	$R_{\theta JC}$	1.25°C/W

(1) See figures 4, 5 and 6 of MIL-PRF-19500/371 for temperature-power derating curves.

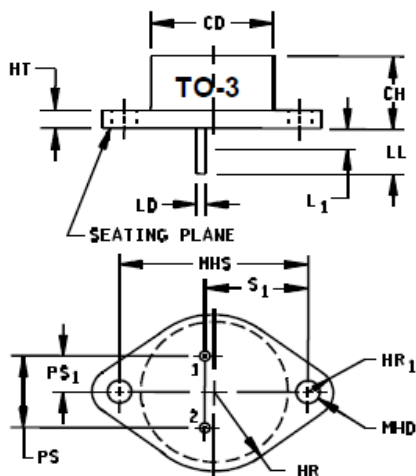
(2) For thermal impedance curves, see figures 7, 8 and 9 of MIL-PRF-19500/371.

2N3902 & 2N5157

NPN High Power Silicon Transistors

Rev. V4

Outline Drawing (TO-3)



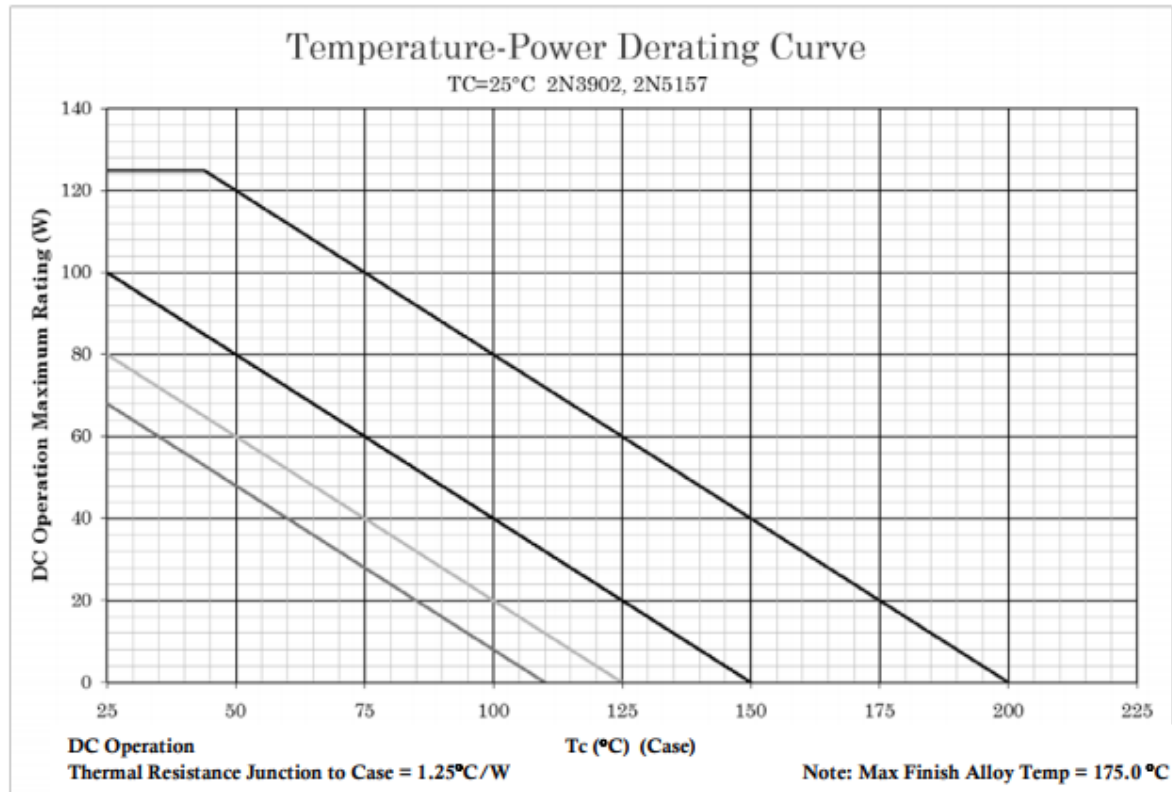
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.22	3
CH	.250	.328	6.35	8.33	
HR	.495	.525	12.57	13.34	
HR ₁	.131	.188	3.33	4.78	6
HT	.060	.135	1.52	3.43	
LD	.038	.043	0.97	1.09	4, 5, 9
LL	.312	.500	7.92	12.70	4, 5, 9
L ₁		.050		1.27	5, 9
MHD	.151	.161	3.84	4.09	7
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	
PS ₁	.205	.225	5.21	5.72	5
S ₁	.655	.675	16.64	17.15	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Body contour is optional within zone defined by CD.
4. These dimensions shall be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement shall be made at seating plane.
5. Both terminals.
6. At both ends.
7. Two holes.
8. Terminal 1 is the emitter, terminal 2 is base. The collector shall be electrically connected to the case.
9. LD applies between L₁ and LL. Lead diameter shall not exceed twice LD within L₁.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.
11. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.

* FIGURE 1. Physical dimensions, 2N3902, 2N5157 (modified TO-204AA, similar to TO-3).

Temperature-Power Derating Curve

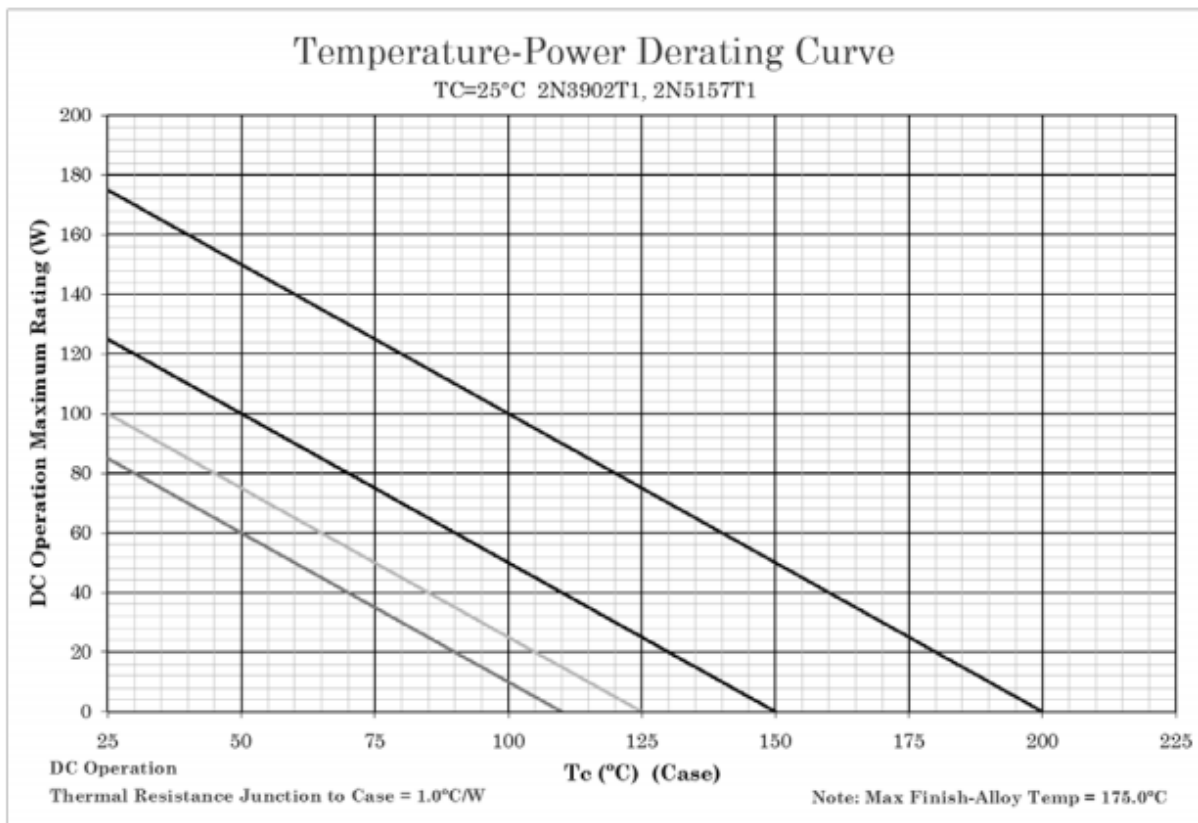


NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

FIGURE 4. Temperature-power derating graph (TO-3), 2N3902 and 2N5157.

Temperature-Power Derating Curve

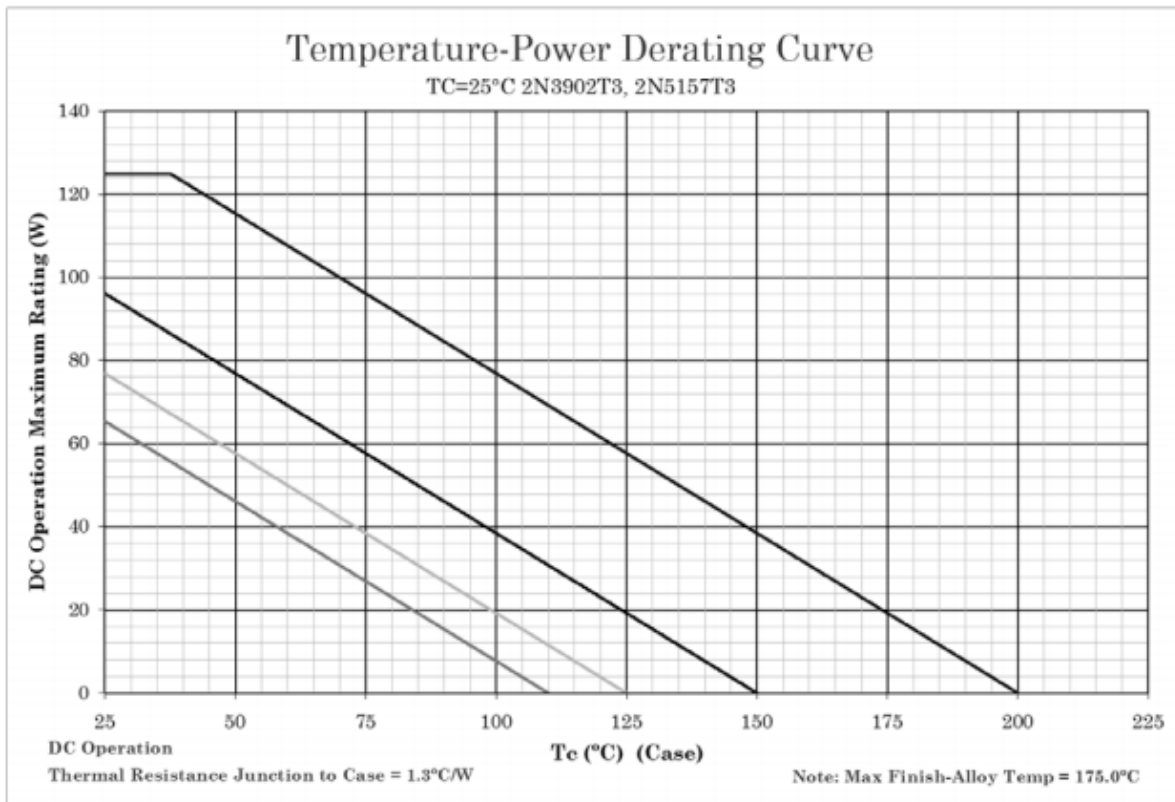


NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

FIGURE 5. Temperature-power derating graph (TO-254), 2N3902T1 and 2N5157T1.

Temperature-Power Derating Curve

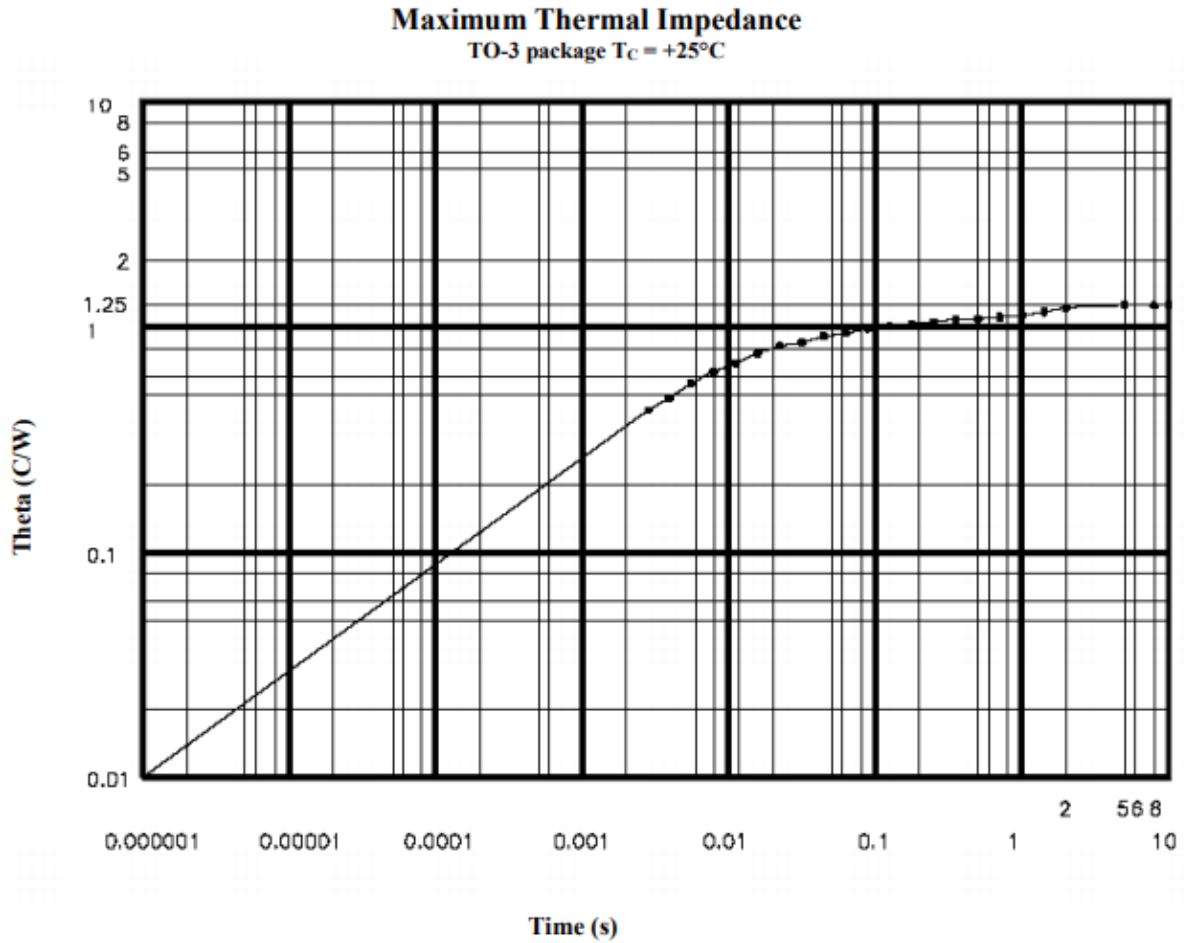


NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

FIGURE 6. Temperature-power derating graph (TO-257), 2N3902T3 and 2N5157T3.

Thermal Impedance Curve



$R_{\theta JC} = 1.25^\circ\text{C/W max.}$

FIGURE 7. Thermal impedance graph (2N3902 and 2N5157).

2N3902 & 2N5157



NPN High Power Silicon Transistors

Rev. V4

Thermal Impedance Curve

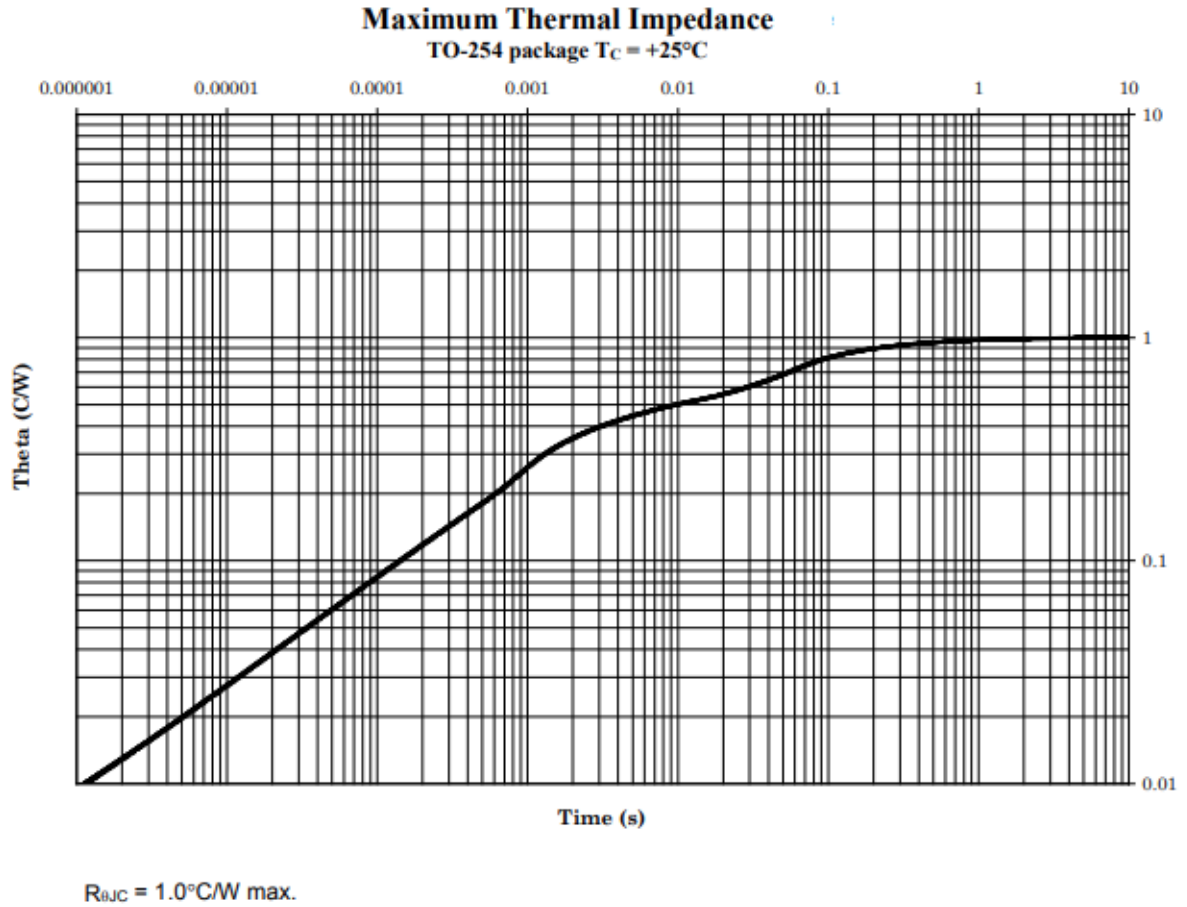
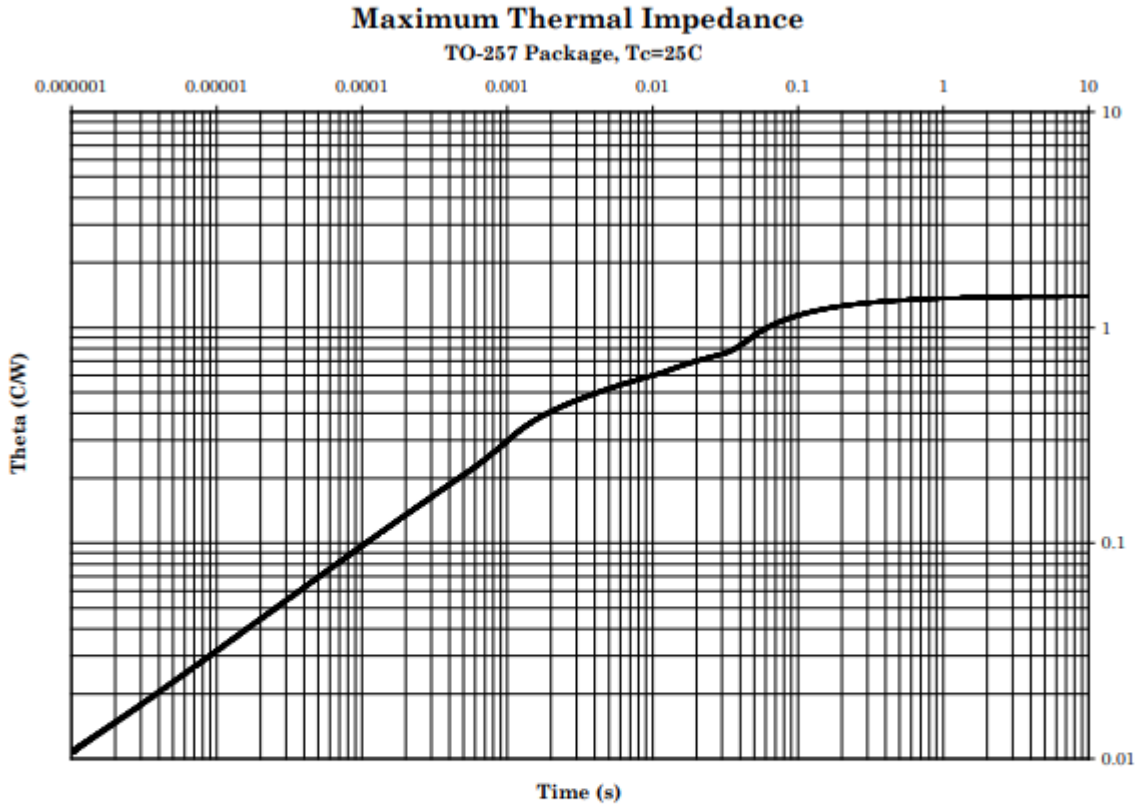


FIGURE 8. Thermal impedance graph (2N3902T1 and 2N5157T1).

Thermal Impedance Curve



$R_{\theta JC} = 1.3^{\circ}\text{C/W max.}$

FIGURE 9. Thermal impedance graph (2N3902T3, and 2N5157T3).

2N3902 & 2N5157



NPN High Power Silicon Transistors

Rev. V4

VPT COMPONENTS. ALL RIGHTS RESERVED.

Information in this document is provided in connection with VPT Components products. These materials are provided by VPT Components as a service to its customers and may be used for informational purposes only. Except as provided in VPT Components Terms and Conditions of Sale for such products or in any separate agreement related to this document, VPT Components assumes no liability whatsoever. VPT Components assumes no responsibility for errors or omissions in these materials. VPT Components may make changes to specifications and product descriptions at any time, without notice. VPT Components makes no commitment to update the information and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to its specifications and product descriptions. No license, express or implied, by estoppels or otherwise, to any intellectual property rights is granted by this document.

THESE MATERIALS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, RELATING TO SALE AND/OR USE OF VPT COMPONENTS PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, CONSEQUENTIAL OR INCIDENTAL DAMAGES, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. VPT COMPONENTS FURTHER DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. VPT COMPONENTS SHALL NOT BE LIABLE FOR ANY SPECIAL, INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS, WHICH MAY RESULT FROM THE USE OF THESE MATERIALS.

VPT Components products are not intended for use in medical, lifesaving or life sustaining applications. VPT Components customers using or selling VPT Components products for use in such applications do so at their own risk and agree to fully indemnify VPT Components for any damages resulting from such improper use or sale.