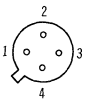
2N5265 thru 2N5270

(SILICON)

P-Channel junction depletion mode (Type A) field-effect transistors designed for general-purpose amplifier applications.

CASE 20(5)
(TO-72)



STYLE 5
PIN 1. SOURCE
2. GATE 1
3. DRAIN
4. CASE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	Vdc
Drain-Gate Voltage	V_{DG}	60	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	60	Vdc
Drain Current	I_D	20	mAdc
Gate Current-forward	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 2.0	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C
Operating Junction Temperature Range	T_J	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	60	-	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc)	2N5265, 2N5266	$V_{GS(off)}$	-	3.0	Vdc
	2N5267, 2N5268		-	6.0	
	2N5269, 2N5270		-	8.0	
Gate Reverse Current (V_{GS} = 30 Vdc, V_{DS} = 0)		I_{GSS}	-	2.0	nAdc
(V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 150°C)			-	2.0	μAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5265	I_{DSS}	0.5	1.0	mAdc
	2N5266		0.8	1.6	
	2N5267		1.5	3.0	
	2N5268		2.5	5.0	
	2N5269		4.0	8.0	
	2N5270		7.0	14	
Gate-Source Voltage		V_{GS}			Vdc
(V_{DS} = 15 Vdc, I_D = 0.05 mAdc)	2N5265		0.3	1.5	
(V_{DS} = 15 Vdc, I_D = 0.08 mAdc)	2N5266		0.4	2.0	
(V_{DS} = 15 Vdc, I_D = 0.15 mAdc)	2N5267		1.0	4.0	
(V_{DS} = 15 Vdc, I_D = 0.25 mAdc)	2N5268		1.0	4.0	
(V_{DS} = 15 Vdc, I_D = 0.4 mAdc)	2N5269		2.0	6.0	
(V_{DS} = 15 Vdc, I_D = 0.7 mAdc)	2N5270		2.0	6.0	
SMALL-SIGNAL CHARACTERISTICS					
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5265	$\|y_{fs}\|$	900	2700	μmhos
	2N5266		1000	3000	
	2N5267		1500	3500	
	2N5268		2000	4000	
	2N5269		2200	4500	
	2N5270		2500	5000	
Forward Transconductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5265	$Re(y_{fs})$	800	-	μmhos
	2N5266		900	-	
	2N5267		1400	-	
	2N5268		1700	-	
	2N5269		1900	-	
	2N5270		2100	-	
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\|y_{os}\|$	-	75	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	-	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	-	2.0	pF
Common-Source Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 M ohm, f = 100 Hz, BW = 1.0 Hz)		NF	-	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)		e_n	-	115	$nV/\sqrt{Hz}$

FIGURE 1–6 TRANSFER CHARACTERISTIC CURVES
FOR MIN/MAX I_{DSS} LIMITS

FIGURE 1

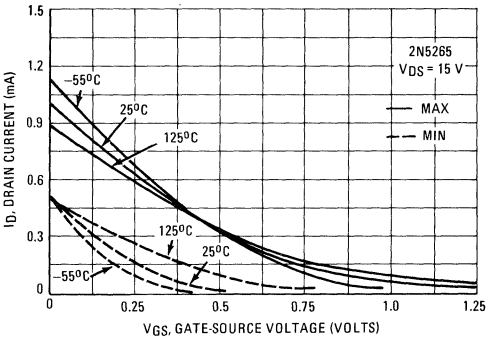


FIGURE 2

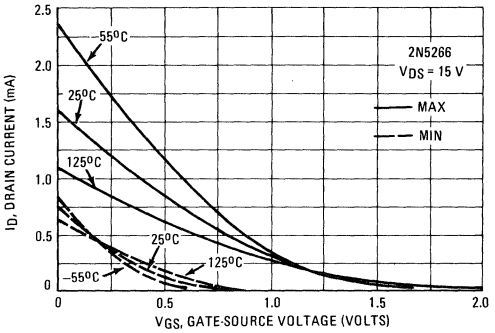


FIGURE 3

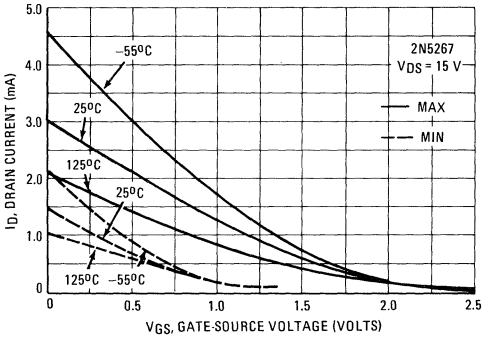


FIGURE 4

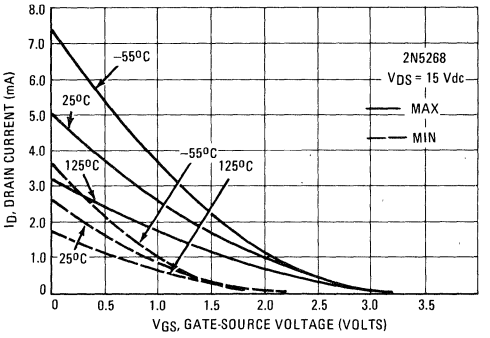


FIGURE 5

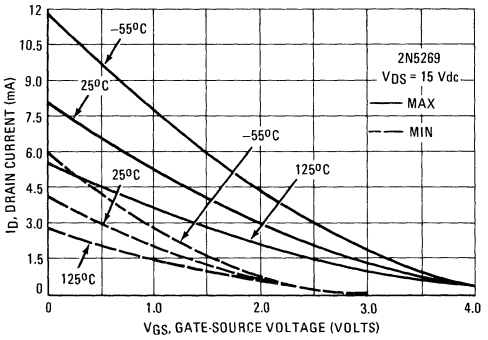
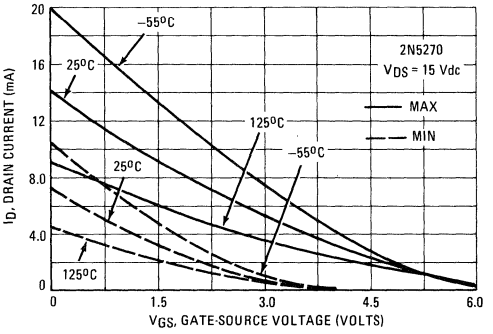


FIGURE 6



FIGURES 7-12 – TYPICAL AND MINIMUM FORWARD TRANSFER ADMITTANCE

FIGURE 7

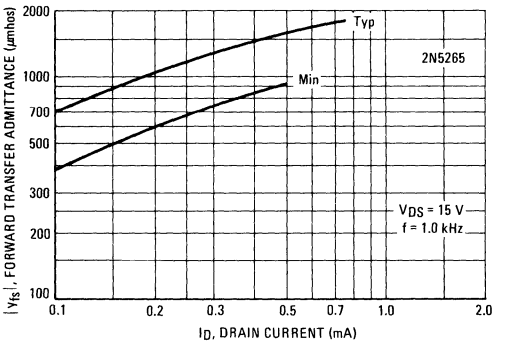


FIGURE 8

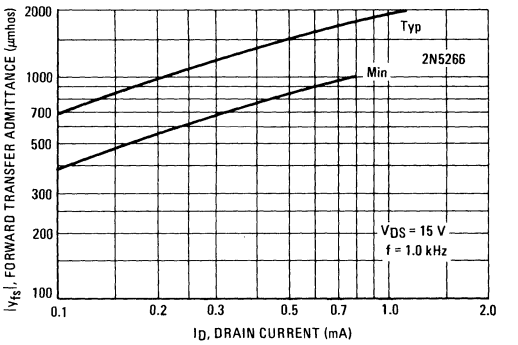


FIGURE 9

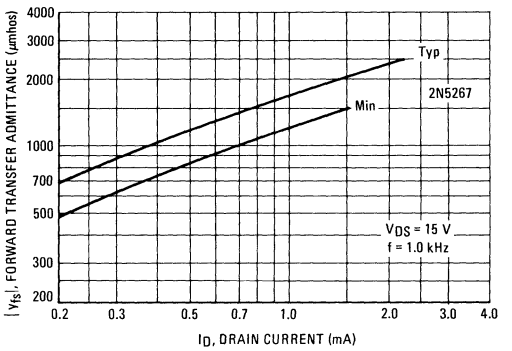


FIGURE 10

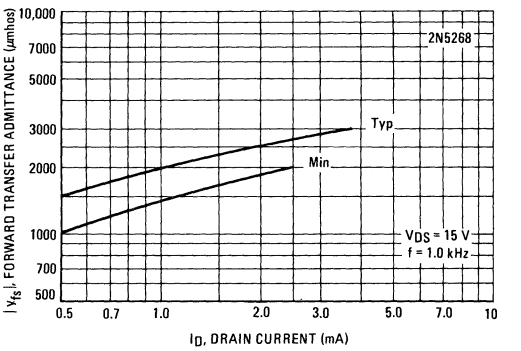


FIGURE 11

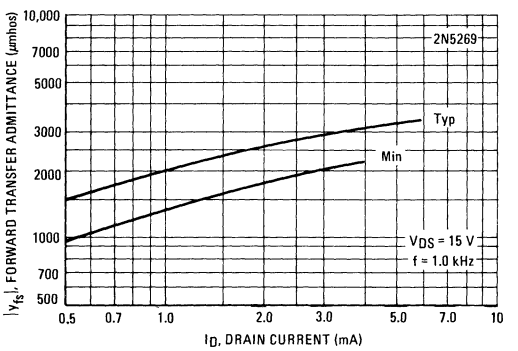
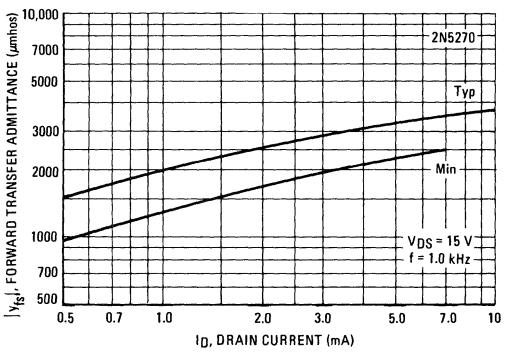


FIGURE 12



TYPICAL CURVES

FIGURE 13 – OUTPUT RESISTANCE versus DRAIN CURRENT

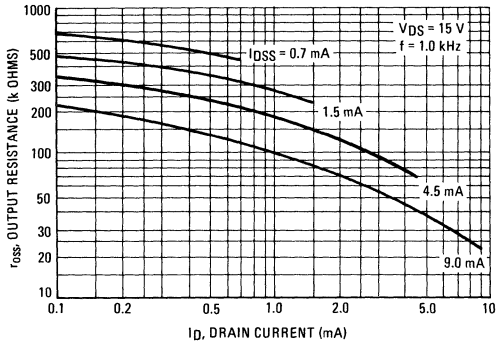


FIGURE 14 – CAPACITANCE versus DRAIN-SOURCE VOLTAGE

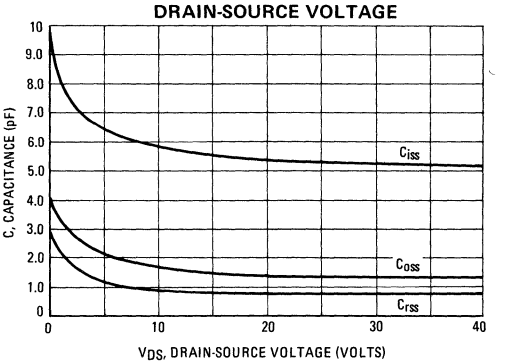


FIGURE 15 – NOISE FIGURE versus FREQUENCY

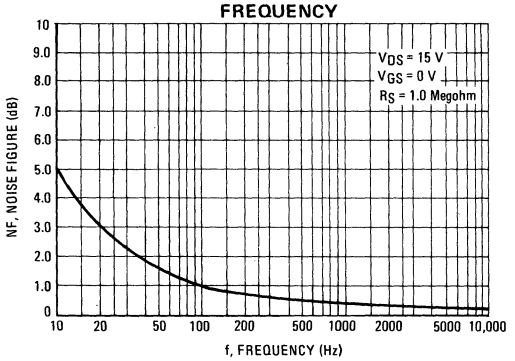


FIGURE 16 – NOISE FIGURE versus SOURCE RESISTANCE

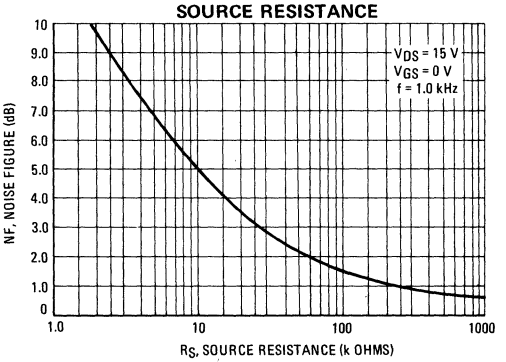


FIGURE 17 – DRAIN CURRENT TEMPERATURE COEFFICIENT versus DRAIN CURRENT

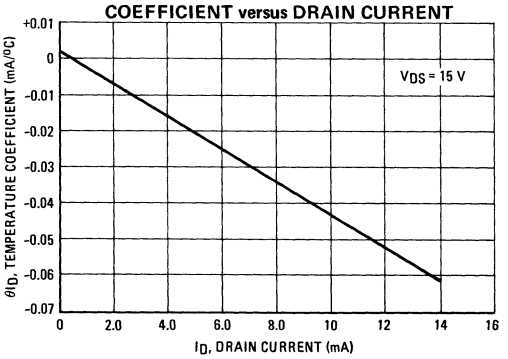


FIGURE 18 – FORWARD TRANSADMITTANCE COEFFICIENT versus DRAIN CURRENT

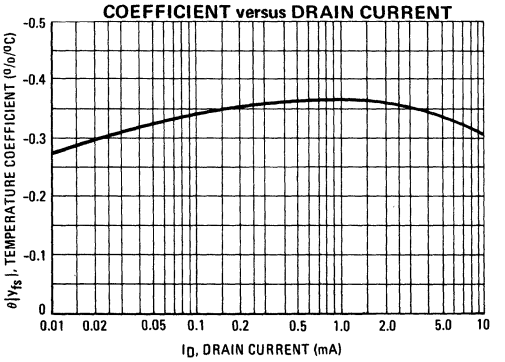
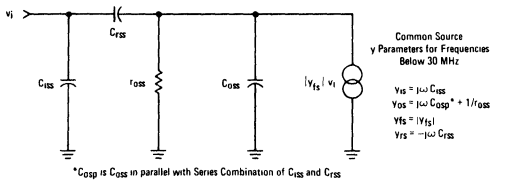


FIGURE 19 – EQUIVALENT LOW FREQUENCY CIRCUIT



BIAS NETWORK DESIGN FOR WORST CASE I_{DSS} VARIANCE

This Designers Data Sheet has been published to assist the circuit designer in optimizing his "worst case" design. The following example illustrates the use of the forward transfer characteristics curves (Figures 1 thru 6) in the design of a typical bias network.

Given: V_{DD} = -30 Vdc, I_D = 1.0 ± 0.25 mAdc from -55°C to +125°C

Procedure: The 2N5268 "worst case" bias conditions across the temperature range (from Figure 4) are reproduced in Figure A. The first step in the bias network design is to determine the value of the source resistance (R_S) necessary to hold the ± 0.25 mAdc I_D bias tolerance. To solve R_S, plot $I_{D(max)}$ and $I_{D(min)}$ on Figure A and calculate R_S, and V_G.

$$R_S = \frac{V_{GS(max)} - V_{GS(min)}}{I_{D(max)} - I_{D(min)}} = \frac{1.9\ \text{Vdc} - 0.8\ \text{Vdc}}{(1.25\ \text{mA} - 0.75\ \text{mA})} = 2.2\ \text{k Ohms}$$

$$V_G = \frac{I_{D(max)}\ V_{GS(min)} - I_{D(min)}\ V_{GS(max)}}{I_{D(max)} - I_{D(min)}}$$

$$= \frac{1.25 \times 0.80 - 0.75 \times 1.9}{0.5} = -0.9\ \text{Vdc}$$

In Figure B the maximum allowable value for R_1 will be determined by loading due to gate reverse current. Gate reverse current variations with temperature follow the pattern of all silicon devices, and, as a rule, we can assume that it will double with each 15°C temperature rise. Therefore, we can assume a maximum reverse current of approximately 0.5 μAdc at 125°C, based on the specified maximum 2.0 μAdc reverse at 150°C. The variation in V_G bias versus temperature will not be too great if we chose a value for R_1 which results in a bias network current (I_1 in Figure B) greater than 5 times the maximum reverse current. Assuming a value for R_1 of 9.1 Megohms, R_2 can be solved from the equation:

$$V_G = -0.9\ \text{Vdc} \approx \frac{-30\ R_2}{9.1 + R_2}\ \text{(Ignoring } I_G\text{)}$$

$$R_2 \approx 300\ \text{k Ohms}$$

Using the above values of R_1 and R_2, the variation in V_G can be computed for I_G = 0 to I_G = 0.5 μAdc. V_G will vary from 0.81 Vdc at I_G = 0.5 μAdc to 0.96 Vdc @ I_G = 0. This variation will have a minimal effect on I_D, as can be seen from Figure A by plotting load lines with a slope equal to $1/R_S$ from V_G = 0.81 Vdc and 0.96 Vdc respectively.

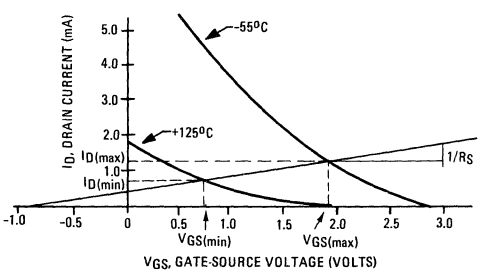


FIGURE A

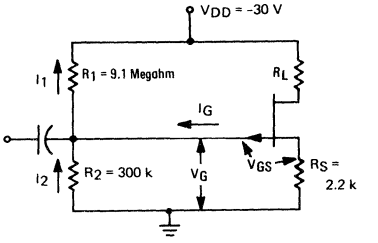


FIGURE B