

# 2N5415, S, UA

# 2N5416, S, UA

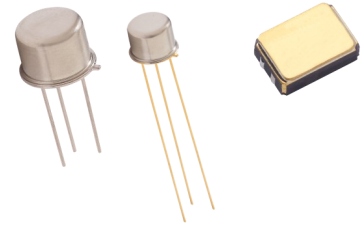


## PNP Low Power, High Voltage Silicon Transistor

Rev. V2

### Features

- Available in JAN, JANTX, JANTXV and JANS per MIL-PRF-19500/485
- TO-39, TO-5 and UA Package Types
- Suitable For Drivers in High-Voltage, Low Current Inverters, Switching and Series Regulators



### Electrical Characteristics ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Emitter - Base Cutoff Current	$V_{EB} = -6.0 \text{ V dc}$	$I_{EBO}$	$\mu\text{A dc}$	—	-20
Collector - Emitter Cutoff	$V_{CE} = -150 \text{ V dc}$ 2N5415, S, UA $V_{CE} = -250 \text{ V dc}$ 2N5416, S, UA	$I_{CEO1}$	$\mu\text{A dc}$		-50
Collector - Emitter Cutoff	$V_{CE} = -200 \text{ V dc}$ 2N5415, S, UA $V_{CE} = -300 \text{ V dc}$ 2N5416, S, UA	$I_{CEO2}$	$\text{mA dc}$		-1
Collector - Emitter Cutoff Current	$V_{BE} = -1.5 \text{ V dc}$ $V_{CE} = -200 \text{ V dc}$ 2N5415, S, UA $V_{CE} = -300 \text{ V dc}$ 2N5416, S, UA	$I_{CEX}$	$\mu\text{A dc}$	—	-50
Collector - Base Cutoff Current	$V_{CB} = -175 \text{ V dc}$ 2N5415, S, UA $V_{CB} = -280 \text{ V dc}$ 2N5416, S, UA	$I_{CBO1}$	$\mu\text{A dc}$	—	-50
Collector - Base Cutoff Current	$V_{CB} = -200 \text{ V dc}$ 2N5415, S, UA $V_{CB} = -350 \text{ V dc}$ 2N5416, S, UA	$I_{CBO2}$	$\mu\text{A dc}$	—	-500
Base - Emitter Voltage Saturation	$V_{CE} = -10 \text{ V dc}$ , $I_C = -50 \text{ mA dc}$	$V_{BE}$	$\text{V dc}$		-1.5
Collector - Emitter Voltage (saturated)	$I_C = -50 \text{ mA dc}$ , $I_B = -5 \text{ mA dc}$	$V_{CE(sat)}$	$\text{V dc}$		-2.0
Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V dc}$ , $I_C = -50 \text{ mA dc}$	$h_{FE1}$	-	30	120
	$V_{CE} = -10 \text{ V dc}$ , $I_C = -1 \text{ mA dc}$	$h_{FE2}$		15	

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### Electrical Characteristics (+25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Base Cutoff Current	$T_A = +150^\circ\text{C}$ $V_{CB} = -175\text{ V dc}$ 2N5415, S, UA $V_{CB} = -280\text{ V dc}$ 2N5416, S, UA	$I_{CBO3}$	mA dc		-1
Forward – Current Transfer Ratio	$T_A = -65^\circ\text{C}$ $V_{CE} = -10\text{ V dc}$ , $I_C = -50\text{ mA dc}$	$h_{FE3}$		15	
Parameter	Test Conditions	Symbol	Units	Min.	Max.
<b>Dynamic Characteristics</b>					
Small-Signal Short-Circuit Forward-Current Transfer Ratio	$V_{CE} = -10\text{ V dc}$ , $I_C = -10\text{ mA dc}$ , $f = 5\text{ MHz}$	$ h_{FE} $		3	15
Output Capacitance Output Capacitance	$V_{CB} = -10\text{ V dc}$ , $I_E = 0$ , $100\text{ kHz} \leq f \leq 1\text{ MHz}$	$C_{obo}$	pF	—	15
Small-Signal Short-Circuit Forward-Current Transfer Ratio	$V_{CE} = -10\text{ V dc}$ , $I_C = -5\text{ mA dc}$ , $f \leq 1\text{ kHz}$	$h_{fe}$		25	—
Input Capacitance (Output Open Circuited)	$V_{EB} = -5\text{ V dc}$ , $I_C = 0$ , $100\text{ kHz} \leq f \leq 1\text{ MHz}$	$C_{ibo}$	pF	—	75
<b>Switching Characteristics</b>					
Turn-On Time	$V_{CC} = -200\text{ V dc}$ , $I_C = -50\text{ mA dc}$ , $I_{B1} = -5\text{ mA dc}$	$t_{on}$	$\mu\text{s}$	—	1.0
Turn-Off Time	$V_{CC} = -200\text{ V dc}$ , $I_C = -50\text{ mA dc}$ , $I_{B1} = I_{B2} = -5\text{ mA dc}$	$t_{off}$	$\mu\text{s}$	—	10

### Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Ratings	Symbol	2N5415	2N5416
Collector - Emitter Voltage	$V_{CEO}$	-200 V dc	-300 V dc
Collector - Base Voltage	$V_{CBO}$	-200 V dc	-350 V dc
Emitter - Base Voltage	$V_{EBO}$	-6.0 V dc	
Collector Current	$I_C$	-1.0 A dc	
Junction & Storage Temperature Range	$T_J, T_{STG}$	-65°C to +200°C	

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## Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Thermal Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Ambient 2N5415, 2N5415S, 2N5415UA 2N5416, 2N5416S, 2N5416UA	$R_{\theta JA}$	234°C/W 234°C/W
Thermal Resistance, Junction to Case 2N5415, 2N5415S 2N5416, 2N5416S	$R_{\theta JC}$	17.5°C/W 17.5°C/W
Thermal Resistance, Junction to Solder Pad 2N5415UA, 2N5416UA	$R_{\theta JSP}$	80°C/W

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### Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Max. Value
$T_A = +25^\circ\text{C}$ 2N5415, 2N5415S, 2N5415UA 2N5416, 2N5416S, 2N5416UA	$P_T^{(1)}$	0.75 W 0.75 W
$T_C = +25^\circ\text{C}$ 2N5415, 2N5415S 2N5416, 2N5416S	$P_T^{(2)}$	10 W 10 W
$T_{SP} = +25^\circ\text{C}$ 2N5415UA, 2N5416UA	$P_T^{(3)}$	2.0 W

(1) Derate linearly 4.29 mW/°C for  $T_A > +25^\circ\text{C}$ .

(2) Derate linearly 57.2 mW/°C for  $T_C > +25^\circ\text{C}$ .

(3) Derate linearly 12.5 mW/°C for  $T_{SP} > +25^\circ\text{C}$

Electrical Measurements	Test Conditions	Symbol	Units	Min.	Max.
Breakdown Voltage, Collector-Emitter	$I_C = -50$ mA dc, $I_B = -5$ mA dc, $L = 25$ mH; $f = 30 - 60$ Hz 2N5415, S, UA 2N5416, S, UA	$V_{BR(CEO)}$	V dc	-200 -300	—

### Safe Operating Area

DC Tests:	$T_C = +25^\circ\text{C}$ ; 1 Cycle; $t = 0.4$ s
Test 1 (except UA):	$V_{CE} = -10$ V dc; $I_C = -1.0$ A dc
Test 2: (except UA)	$V_{CE} = -100$ V dc; $I_C = -100$ mA dc
Test 3: (except UA)	$V_{CE} = -200$ V dc; $I_C = -24$ mA dc (2N5415, S, only)
Test 4:	$V_{CE} = -300$ V dc; $I_C = -10$ mA dc (2N5416, S, only)
Test 1: UA only	$V_{CE} = -10$ V dc; $I_C = -0.3$ A dc
Test 2: UA only	$V_{CE} = -100$ V dc; $I_C = -30$ mA dc
Test 3:	$V_{CE} = -200$ V dc; $I_C = -12$ mA dc (2N5415UA only)
Test 4:	$V_{CE} = -300$ V dc; $I_C = -5$ mA dc (2N5416UA only)

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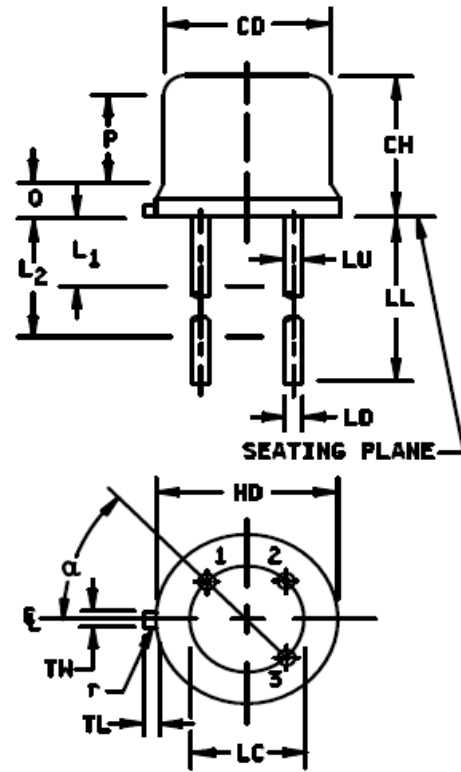


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### Outline Drawing (TO-5, TO-39)

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7, 8
LL	See notes				7, 8, 11, 12
LU	.016	.019	0.41	0.48	7, 8
L <sub>1</sub>		.050		1.27	7, 8
L <sub>2</sub>	.250		6.35		7, 8
P	.100		2.54		5
Q		.050		1.27	4
r		.010		0.25	10
TL	.029	.045	0.74	1.14	3
TW	.028	.034	0.71	0.86	2
α	45° TP		45° TP		6



#### NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TH shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between L<sub>2</sub> and LL minimum. Diameter is uncontrolled in L<sub>1</sub> and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. For transistor types 2N5415 and 2N5416, dimension LL shall be 1.5 inches (38.1 mm) minimum and 1.75 inches (44.4 mm) maximum.
12. For transistor types 2N5415S and 2N5416S, dimension LL shall be .5 inch (12.7 mm) minimum and .75 inch (19.0 mm) maximum.
13. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
14. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

FIGURE 1. Physical dimensions (similar to TO-5).

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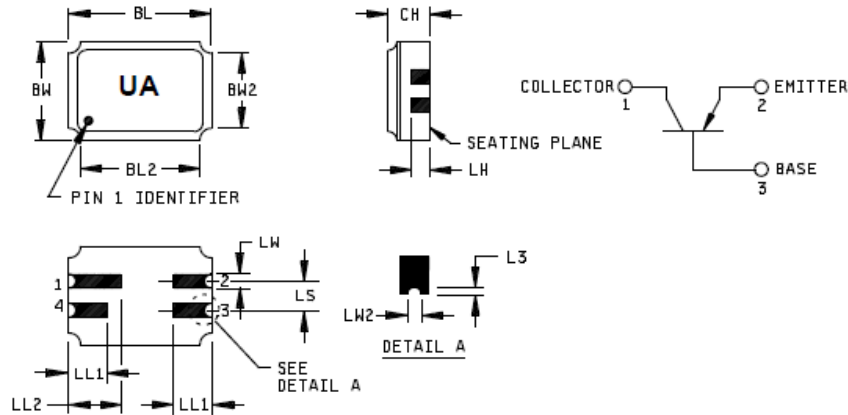
# 2N5416, S, UA



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### Outline Drawing (UA Package)



Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.91	3
L3	.003		0.08		5
LH	.029	.042	0.74	1.07	

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

Pin Number	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

#### NOTES:

- Dimensions are in inches.
- Millimeters are given for general information only.
- Dimension "CH" controls the overall package thickness. When a window lid is used, dimension "CH" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.016 mm).
- The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
- \* Dimensions "LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW2" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of this dimension may be made prior to solder dipping.
- The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
- In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.

\* FIGURE 2. Physical dimensions, surface mount (UA version).

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