2N5432-34 N-Channel JFETs

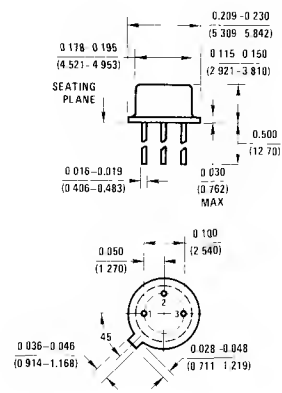
General Description

The 2N5432 thru 2N5434 series of N-channel JFETs is designed for analog switch applications requiring very low ON resistance.

Absolute Maximum Ratings (25°C)

Reverse Gate-Drain or Gate-Source Voltage	−25V
Gate Current	100 mA
Drain Current	400 mA
Total Device Dissipation at 25°C Free-Air Temperature, (Note 1)	300 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-52



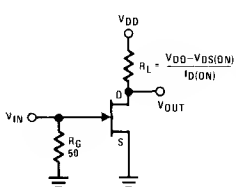
PIN	FET (07)
1	S
2	D
3	G

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5432 MIN	2N5432 MAX	2N5433 MIN	2N5433 MAX	2N5434 MIN	2N5434 MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−200		−200		−200	pA
			150°C		−200		−200		−200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−25		−25		−25		V
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 5V, V_{GS} = −10V			200		200		200	pA
			150°C		200		200		200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 5V, I_D = 3 nA		−4	−10	−3	−9	−1	−4	V
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 2)		150		100		30		mA
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0, I_D = 10 mA		2	5		7		10	Ω
$V_{DS(on)}$	Drain-Source ON Voltage				50		70		100	mV
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0	f = 1 kHz		5		7		10	Ω
C_{iss}	Common-Source Input Capacitance	V_{DS} = 0, V_{GS} = −10V	f = 1 MHz		30		30		30	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				15		15		15	
t_d	Turn ON Delay Time	V_{DD} = 1.5V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = −12V, $I_{D(on)}$ = 10 mA			4		4		4	ns
t_r	Rise Time				1		1		1	
t_{off}	Turn OFF Delay Time				6		6		6	
t_f	Fall Time				30		30		30	

Note 1: Derate linearly at the rate of 2.3 mW/°C.

Note 2: Pulse test required pulse width 300 μs, duty cycle ≤ 3%.



Input Pulse
Rise time = 0.25 ns
Fall time = 0.75 ns
Pulse width = 200 ns
Pulse rate = 550 pps

Sampling Scope
Rise time = 0.4 ns
Input resistance = 10M
Input Capacitance = 1.5 pF