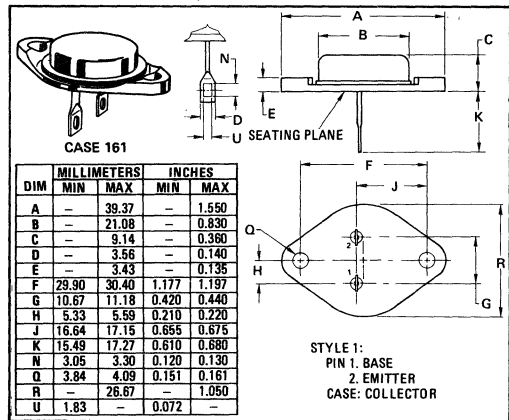
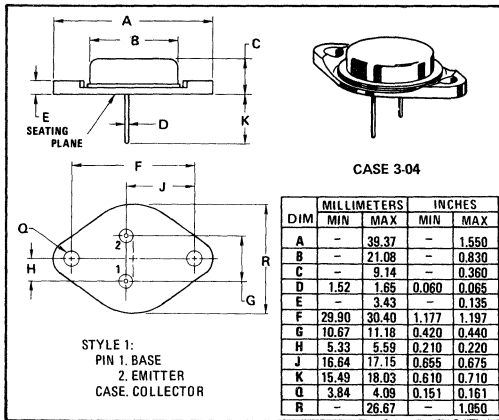


2N5435 (GERMANIUM)

thru

2N5440

PNP germanium power switching transistors designed for high-current, fast-switching applications requiring low saturation voltage and excellent safe operating area.



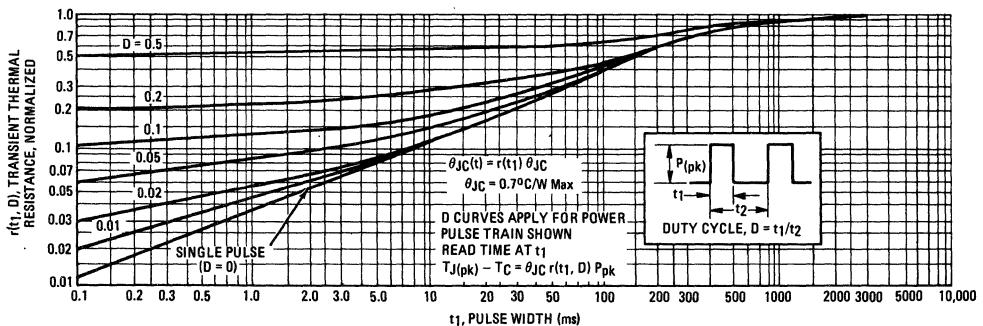
MAXIMUM RATINGS \*\*

Rating	Symbol	2N5435	2N5436	2N5437	Unit
		2N5438	2N5439	2N5440	
Collector-Emitter Voltage	$V_{CEO}$	60	90	120	Vdc
Collector-Base Voltage	$V_{CB}$	80	110	140	Vdc
Emitter-Base Voltage	$V_{EB}$	2.5			Vdc
Collector Current — Continuous	$I_C$	60			Adc
Base Current — Continuous	$I_B$	12			Adc
Total Device Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	$P_D$	120			Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +110			$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.7	$^\circ C/W$

FIGURE 1 — THERMAL RESPONSE



\*\* Maximum Ratings for MP5435 Series are the Same as the 2N5435 Series.

# 2N5435 thru 2N5440 (continued)

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted) \*\*

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Breakdown Voltage (I <sub>C</sub> = 0.1 Adc, I <sub>B</sub> = 0)	BV <sub>CEO</sub>	60 90 120	- - -	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 80 Vdc, V <sub>BE(off)</sub> = 0.2 Vdc)	I <sub>CEX</sub>	-	10	mAdc
(V <sub>CE</sub> = 110 Vdc, V <sub>BE(off)</sub> = 0.2 Vdc)		-	10	
(V <sub>CE</sub> = 140 Vdc, V <sub>BE(off)</sub> = 0.2 Vdc)		-	10	
(V <sub>CE</sub> = 80 Vdc, V <sub>BE(off)</sub> = 0.2 Vdc, T <sub>C</sub> = +85°C)		-	30	
(V <sub>CE</sub> = 110 Vdc, V <sub>BE(off)</sub> = 0.2 Vdc, T <sub>C</sub> = +85°C)		-	30	
(V <sub>CE</sub> = 140 Vdc, V <sub>BE(off)</sub> = 0.2 Vdc, T <sub>C</sub> = +85°C)		-	30	
Collector Cutoff Current (V <sub>CB</sub> = 2.0 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	-	200	μAdc
Emitter Cutoff Current (V <sub>BE</sub> = 2.5 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	-	500	mAdc

## ON CHARACTERISTICS

DC Current Gain* (I <sub>C</sub> = 25 Adc, V <sub>CE</sub> = 2.0 Vdc)	h <sub>FE</sub> *	20 40	60 120	
(I <sub>C</sub> = 60 Adc, V <sub>CE</sub> = 2.0 Vdc)		10 15	- -	
Collector-Emitter Saturation Voltage* (I <sub>C</sub> = 60 Adc, I <sub>B</sub> = 6.0 Adc)	V <sub>CE(sat)</sub> *	-	0.75 0.50	Vdc
Base-Emitter Saturation Voltage* (I <sub>C</sub> = 60 Adc, I <sub>B</sub> = 6.0 Adc)	V <sub>BE(sat)</sub> *	-	1.2 0.9	Vdc

## SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product (I <sub>C</sub> = 5.0 Adc, V <sub>CE</sub> = 5.0 Vdc, f = 100 kHz)	f <sub>T</sub>	350	-	kHz
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## SWITCHING CHARACTERISTICS

Rise Time	(I <sub>C</sub> = 25 Adc, I <sub>B1</sub> = 2.5 Adc, I <sub>B2</sub> = 2.5 Adc) (See Figure 4)	t <sub>r</sub>	-	12	μs
Storage Time		t <sub>s</sub>	-	10	μs
Fall Time		t <sub>f</sub>	-	8.0	μs

\*\*Electrical Characteristics for MP5435 series are the same as the 2N5435 series.

\* To avoid excessive heating of the collector junction, perform test with pulse method.

FIGURE 2 - POWER-TEMPERATURE DERATING CURVE

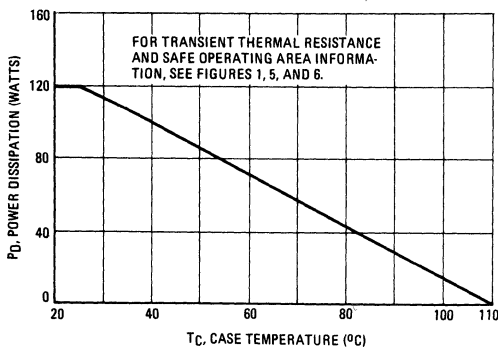


FIGURE 3 - SWITCHING TIMES

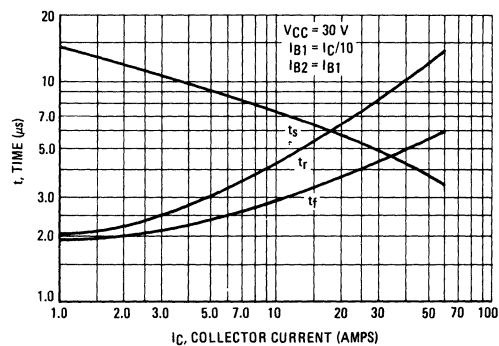


FIGURE 4 – SWITCHING TIME TEST CIRCUIT

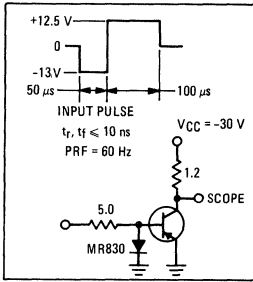
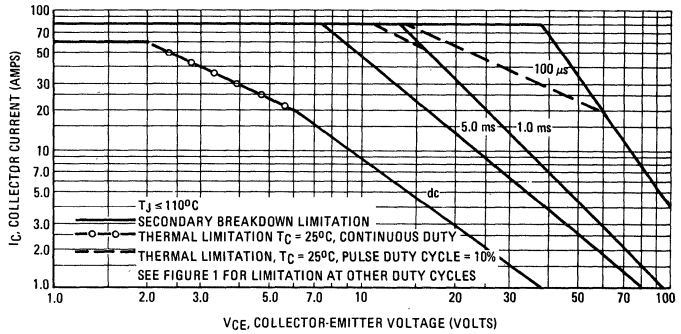


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 110^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Pulse curves are valid for duty cycles to 10% provided  $T_{J(pk)} < 110^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – CLAMPED INDUCTIVE SAFE OPERATING AREA

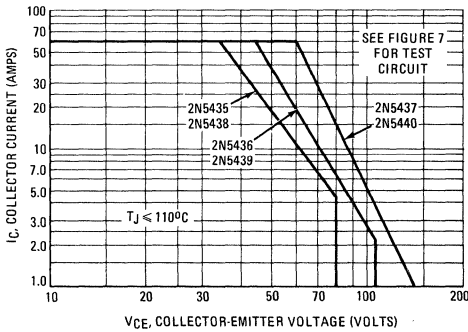


FIGURE 7 – CLAMPED INDUCTIVE SAFE OPERATING AREA TEST CIRCUIT

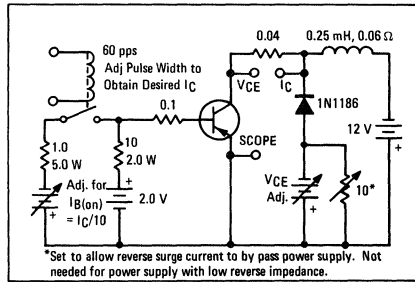


FIGURE 8 – DC CURRENT GAIN

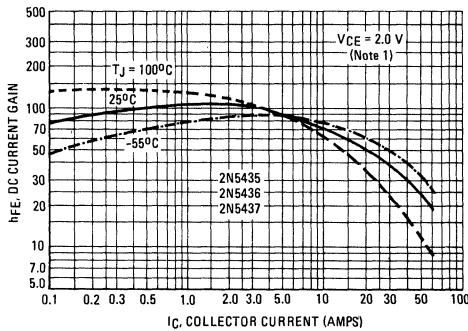
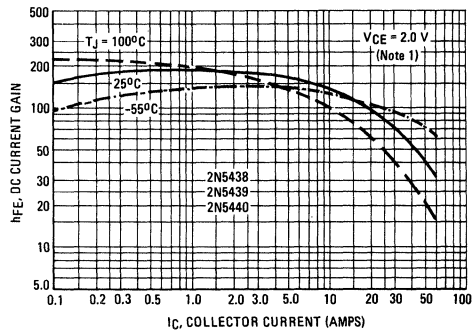


FIGURE 9 – DC CURRENT GAIN



NOTE 1: Data is obtained from pulse tests and adjusted to nullify the effect of  $I_C B Q_0$ .

FIGURE 10 – COLLECTOR SATURATION REGION

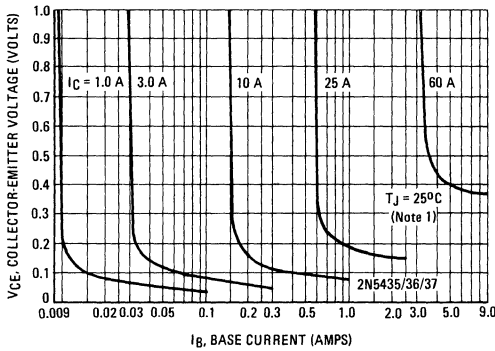


FIGURE 11 – COLLECTOR SATURATION REGION

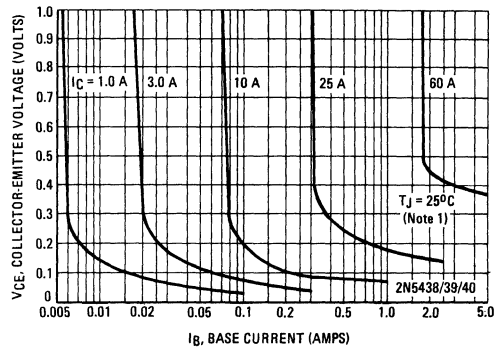


FIGURE 12 – EFFECTS OF BASE-EMITTER RESISTANCE

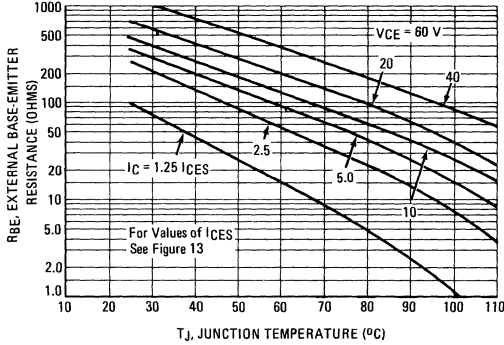


FIGURE 13 – COLLECTOR CUTOFF REGION

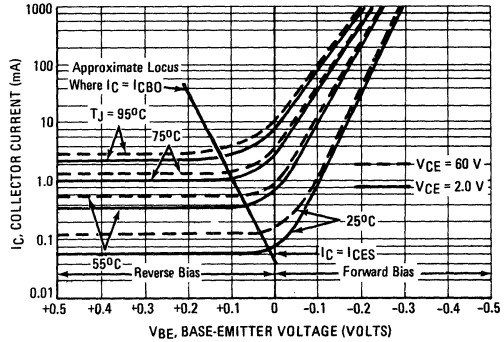


FIGURE 14 – "ON" VOLTAGES

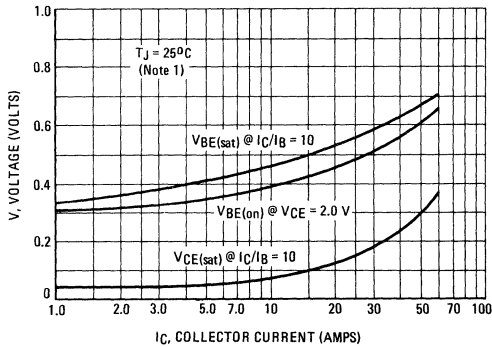


FIGURE 15 – TEMPERATURE COEFFICIENTS

