2N5460, 2N5461, 2N5462 P-Channel JFET

Features

- InterFET P0032F Geometry
- Typical Noise: 2.7 nV/√Hz
- Low Ciss: 3.2pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

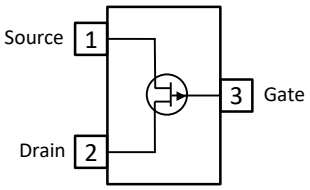
Applications

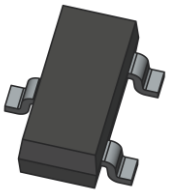
- Audio Amplifiers
- General Purpose Amplifiers

Description

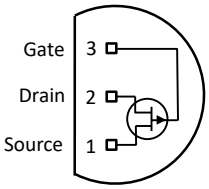
The 40V InterFET 2N5460, 2N5461, and 2N5462 JFET's are targeted for sensitive amplifier stages for mid-frequencies designs. Input capacitance is typically 3.2pF. The 2N5462 is target for higher gain applications with a typical Gfs of 3.5mS.

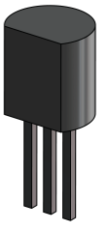
SOT23 Top View





TO-92 Bottom View





Product Summary

Parameters		2N5460 Min	2N5461 Min	2N5462 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	40	40	40	V
I_{DSS}	Drain to Source Saturation Current	-1	-2	-4	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	0.75	1	1.8	V
G_{FS}	Forward Transconductance	1000	1500	2000	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N5460; 2N5461; 2N5462	Through-Hole	TO-92	Bulk
SMP5460; SMP5461; SMP5462	Surface Mount	SOT23	Bulk
SMP5460TR; SMP5461TR; SMP5462TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N5460COT; 2N5461COT; 2N5462COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N5460CFT; 2N5461CFT; 2N5462CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	300	mW
P	Power Derating	1.7	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

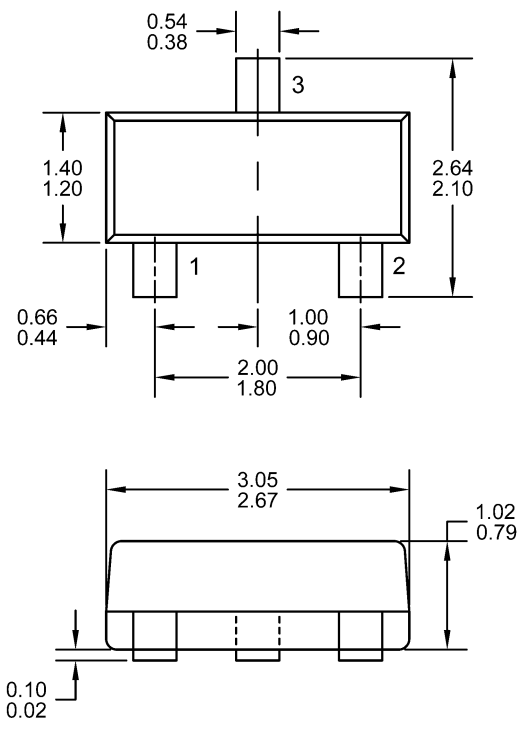
Parameters		Conditions	2N5460		2N5461		2N5462		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = 10µA	40		40		40		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = 20V, V_{DS} = 0V, T_A = 25°C		5		5		5	nA
		V_{GS} = 20V, V_{DS} = 0V, T_A = 100°C		1		1		1	µA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = -15V, I_D = -1µA	0.75	6	1	7.5	1.8	9	V
V_{GS}	Gate to Source Voltage	V_{DS} = -15V, I_D = -100µA	0.8	4.5					V
		V_{DS} = -15V, I_D = -200µA			0.8	4.5			
		V_{DS} = -15V, I_D = -400µA					1.5	6	
I_{DSS}	Drain to Source Saturation Current	V_{DS} = -15V, V_{GS} = 0V (Pulsed)	-1	-5	-2	-9	-4	-16	mA

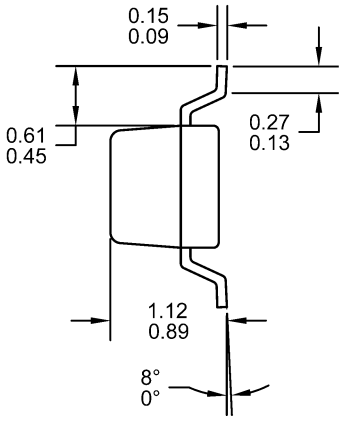
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	2N5460		2N5461		2N5462		Unit
			Min	Max	Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = -15V, V_{GS} = 0V, f = 1kHz	1000	4000	1500	5000	2000	6000	µS
G_{OS}	Output Conductance	V_{DS} = -15V, V_{GS} = 0V, f = 1kHz		75		75		75	µS
C_{iss}	Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1MHz		7		7		7	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1MHz		2		2		2	pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = -15V, V_{GS} = 0V, R_G = 1 MΩ, BW = 1Hz, f = 100Hz		115		115		115	nV/√Hz
NF	Noise Figure	V_{DS} = -15V, V_{GS} = 0V, f = 1kHz		2.5		2.5		2.5	dB

SOT23 (TO-236AB) Mechanical and Layout Data

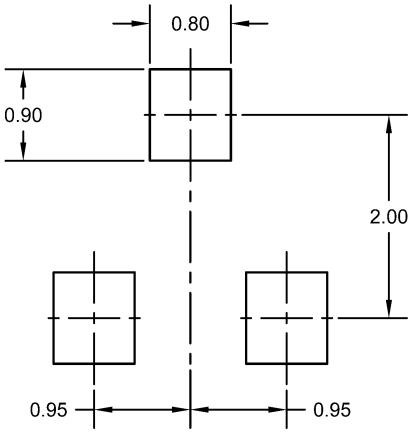
Package Outline Data





1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

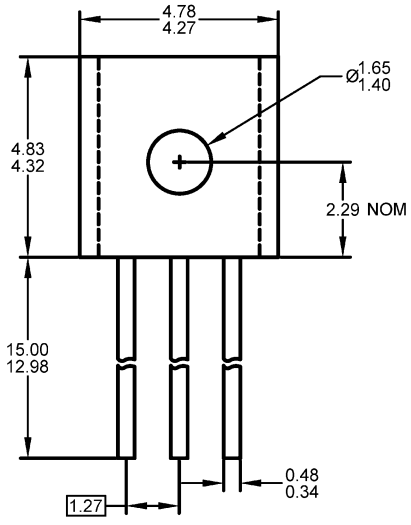
Suggested Pad Layout

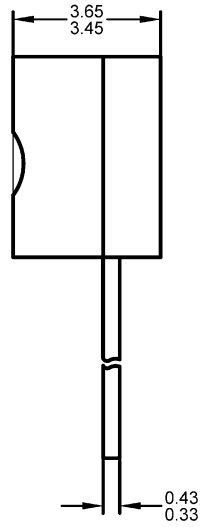


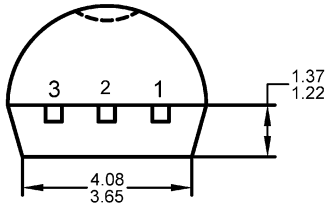
1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

TO-92 Mechanical and Layout Data

Package Outline Data

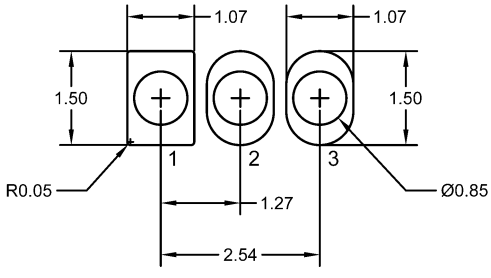






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.