

2N5471 (SILICON)

thru

2N5476

**P-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS**

Depletion mode Junction Field-Effect Transistors designed for general-purpose amplifier and switching applications.

- High Gate-Source Breakdown Voltage –  
 $V_{(BR)GSS} = 40 \text{ Vdc (Min) for All Types}$
- High DC Input Resistance –  
 $I_{GSS} = 100 \text{ pAdc (Max) @ } V_{GS} = 10 \text{ Vdc}$
- Low Reverse Transfer Capacitance –  
 $C_{RSS} = 1.0 \text{ pF (Max) @ } V_{DS} = -15 \text{ Vdc}$
- Tight  $I_{DSS}$  Range for Easier Circuit Design
- Drain and Source Interchangeable

**P-CHANNEL**

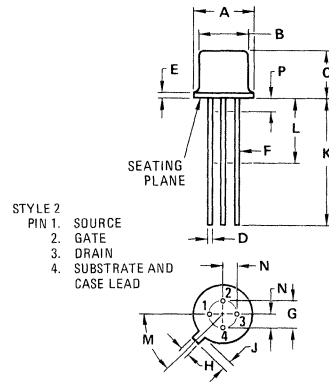
**JUNCTION FIELD-EFFECT TRANSISTORS**



**\*MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Gate Voltage	$V_{DG}$	40	Vdc
Reverse Gate-Source Voltage	$V_{GSR}$	40	Vdc
Forward Gate Current	$I_{GF}$	10	mAdc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 2.0	mW mW/ $^\circ\text{C}$
Operating Channel Temperature Range	$T_{channel}$	-65 to +175	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +200	$^\circ\text{C}$

\* Indicates JEDEC Registered Data.



STYLE 2  
PIN 1. SOURCE  
2. GATE  
3. DRAIN  
4. SUBSTRATE AND CASE LEAD

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.63	0.016	0.021
E	—	0.76	—	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45 $^\circ$ BSC		45 $^\circ$ BSC	
N	1.27 BSC		0.050 BSC	
P	—	1.27	—	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03  
TO-72

## 2N5471 thru 2N5476 (continued)

\*ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Gate-Source Breakdown Voltage ( $I_G = 10 \mu\text{A dc}$ , $V_{DS} = 0$ )	$V_{(BR)GSS}$	40	—	Vdc
Gate-Source Cutoff Voltage ( $V_{DS} = -15 \text{ Vdc}$ , $I_D = -10 \text{ nAdc}$ )	$V_{GS(off)}$	0.5 0.7 0.9 1.2 1.5 2.0	4.0 4.0 6.0 7.0 8.0 9.0	Vdc
Reverse Gate Current ( $V_{GS} = 10 \text{ Vdc}$ , $V_{DS} = 0$ ) ( $V_{GS} = 20 \text{ Vdc}$ , $V_{DS} = 0$ ) ( $V_{GS} = 20 \text{ Vdc}$ , $V_{DS} = 0$ , $T_A = 150^\circ\text{C}$ )	$I_{GSS}$	—	0.1	nAdc
		—	0.5	
		—	1.0	$\mu\text{Adc}$

<b>ON CHARACTERISTICS</b>				
Zero-Gate Voltage Drain Current (1) ( $V_{DS} = -15 \text{ Vdc}$ , $V_{GS} = 0$ )	$I_{DSS}$	0.02 0.05 0.10 0.20 0.40 0.80	0.06 0.12 0.25 0.50 1.0 2.0	mAdc
Gate-Source Voltage ( $V_{DS} = -15 \text{ Vdc}$ , $I_D = 2.0 \mu\text{Adc}$ ) ( $V_{DS} = -15 \text{ Vdc}$ , $I_D = 5.0 \mu\text{Adc}$ ) ( $V_{DS} = -15 \text{ Vdc}$ , $I_D = 10 \mu\text{Adc}$ ) ( $V_{DS} = -15 \text{ Vdc}$ , $I_D = 20 \mu\text{Adc}$ ) ( $V_{DS} = -15 \text{ Vdc}$ , $I_D = 40 \mu\text{Adc}$ ) ( $V_{DS} = -15 \text{ Vdc}$ , $I_D = 80 \mu\text{Adc}$ )	$V_{GS}$	0.5 0.7 0.9 1.2 1.5 2.0	3.0 3.5 4.5 6.0 7.5 8.0	Vdc

### SMALL-SIGNAL CHARACTERISTICS

Forward Transfer Admittance (1) ( $V_{DS} = -15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	$ Y_{fs} $	60 90 120 160 200 260	180 225 300 400 500 650	$\mu\text{mhos}$
Output Admittance (1) ( $V_{DS} = -15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	$ Y_{os} $	— — — — — —	1.0 1.0 2.5 2.5 5.0 10	$\mu\text{mhos}$
Input Capacitance ( $V_{DS} = -15 \text{ Vdc}$ , $V_{GS} = 0$ , $140 \text{ kHz} \leq f \leq 1.0 \text{ MHz}$ )	$C_{iss}$	—	5.0	pF
Reverse Transfer Capacitance ( $V_{DS} = -15 \text{ Vdc}$ , $V_{GS} = 0$ , $140 \text{ kHz} \leq f \leq 1.0 \text{ MHz}$ )	$C_{rss}$	—	1.0	pF
Common-Source Noise Figure ( $V_{DS} = -15 \text{ Vdc}$ , $V_{GS} = 0$ , $R_S = 1.0 \text{ Megohm}$ , $f = 1.0 \text{ kHz}$ , $BW = 1.0 \text{ Hz}$ )	NF	—	2.5	dB
Equivalent Short-Circuit Input Noise Voltage ( $V_{DS} = -15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ , $BW = 1.0 \text{ Hz}$ )	$e_n$	—	110	$\text{nV}/\sqrt{\text{Hz}}$

(1) Pulse Test: Pulse Width  $\leq 630 \text{ ms}$ , Duty Cycle  $\leq 2.0\%$ .

\*Indicates JEDEC Registered Data.

TYPICAL SMALL-SIGNAL CHARACTERISTICS

( $T_{channel} = 25^{\circ}C$ )

FIGURE 1 – FORWARD TRANSFER ADMITTANCE

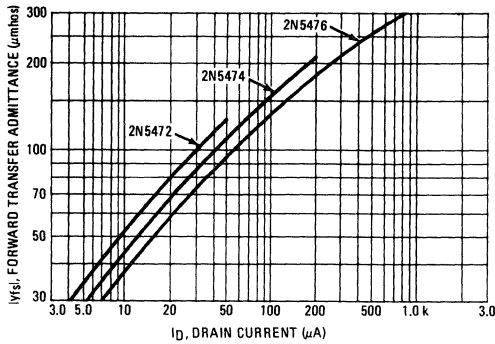
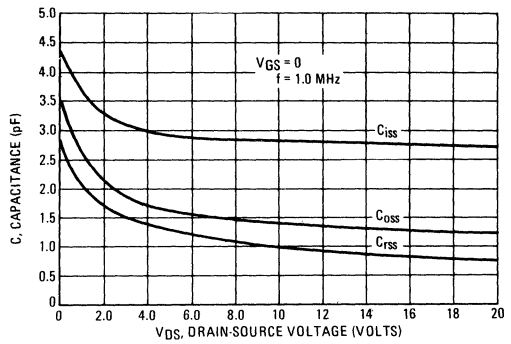


FIGURE 2 – CAPACITANCE



TYPICAL NOISE FIGURE

FIGURE 3 – EFFECTS OF FREQUENCY

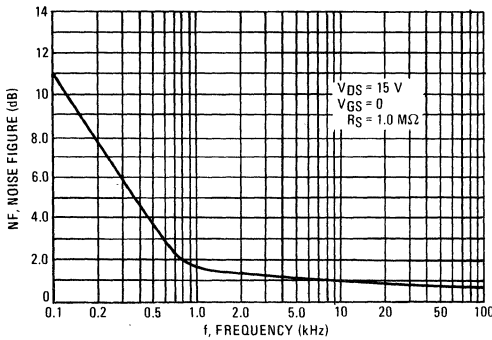


FIGURE 4 – EFFECTS OF SOURCE RESISTANCE

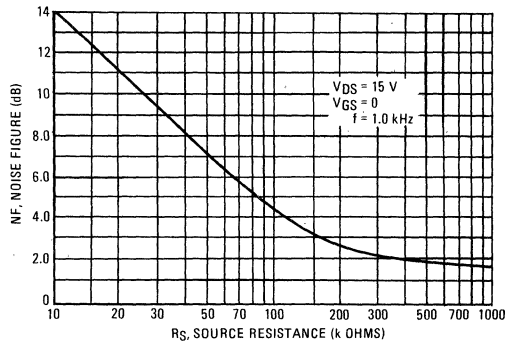
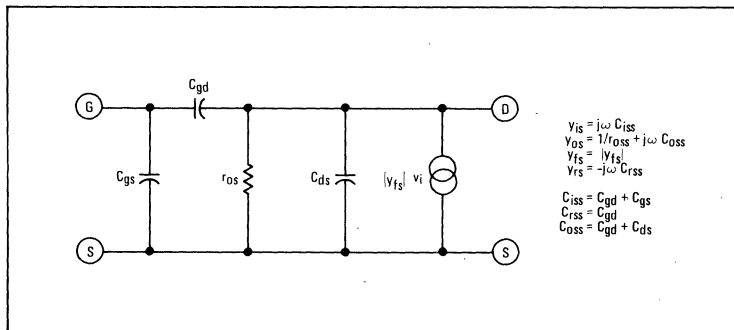
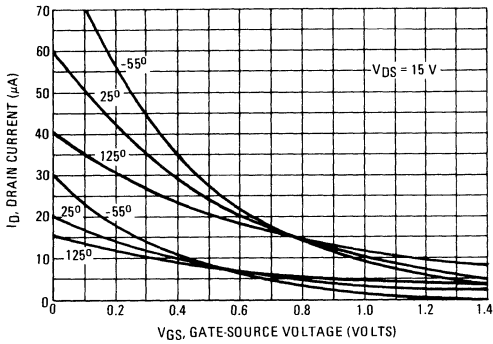


FIGURE 5 – LOW FREQUENCY CIRCUIT MODEL

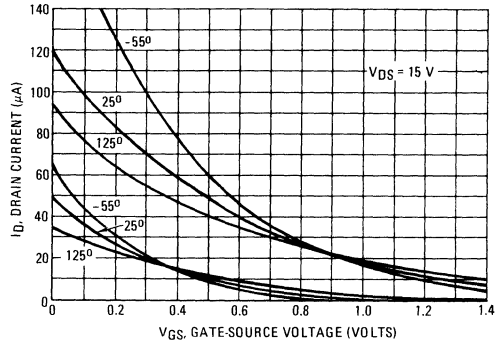


**TYPICAL LIMIT TRANSFER CHARACTERISTICS**  
(TEMPERATURES NOTED ARE  $T_{channel}$ )

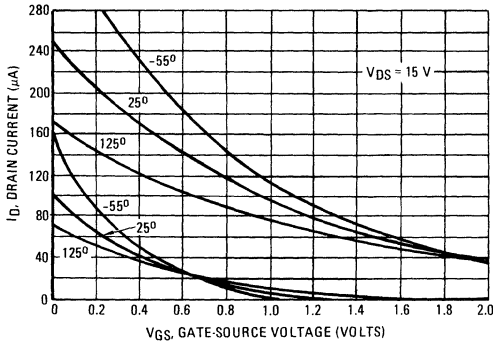
**FIGURE 6 – 2N5471**



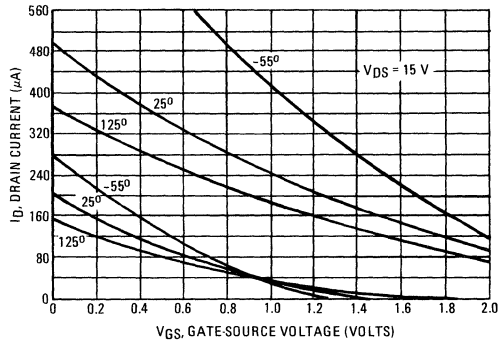
**FIGURE 7 – 2N5472**



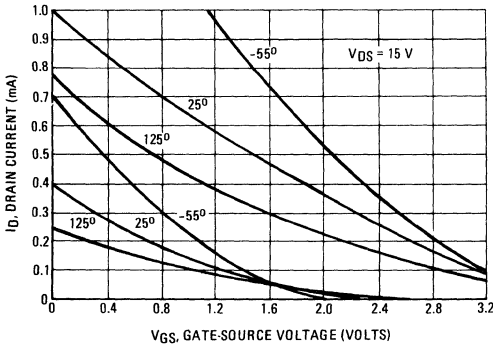
**FIGURE 8 – 2N5473**



**FIGURE 9 – 2N5474**



**FIGURE 10 – 2N5475**



**FIGURE 11 – 2N5476**

