2N5515-24 N-Channel Monolithic Dual JFETs

General Description

The 2N5515 thru 2N5524 series of N-channel monolithic dual JFETs is designed for low to medium frequency differential amplifiers requiring very low noise and high common-mode rejection.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−40V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 85°C (Derate 2 mW/°C)	250 mW
Total Device Dissipation, T_A = 85°C (Derate 3 mW/°C)	375 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

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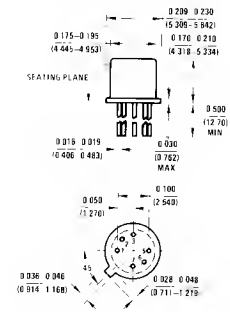

PIN	FET (12)
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−250	pA
			150°C		−250	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA		−0.7	−4	
V_{GS}	Gate-Source Voltage	V_{DG} = 20V, I_D = 200 μA		−0.2	−3.8	
I_G	Gate Operating Current				−100	pA
			125°C		−100	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 1)		0.5	7.5	mA
g_{fs}	Common Source Forward Transconductance	V_{DS} = 20V, V_{GS} = 0, (Note 1)	f = 1 kHz	1000	4000	μmho
g_{fs}	Common Source Forward Transconductance	V_{DG} = 20V, I_D = 200 μA, (Note 1)		500	1000	
g_{os}	Common-Source Output Conductance	V_{DS} = 20V, V_{GS} = 0			10	
g_{os}	Common-Source Output Conductance	V_{DG} = 20V, I_D = 200 μA			1	
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz		25	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				5	
e_n	Equivalent Input Noise Voltage	V_{DG} = 20V, I_D = 200 μA	f = 10 Hz, 2N5515–2N5519		30	$\frac{nV}{\sqrt{Hz}}$
			f = 10 Hz, 2N5520–2N5524		15	
			f = 1 kHz		10	

Matching Characteristics

PARAMETER		CONDITIONS		2N5515, 2N5520 MIN	2N5515, 2N5520 MAX	2N5516, 2N5521 MIN	2N5516, 2N5521 MAX	2N5517, 2N5522 MIN	2N5517, 2N5522 MAX	2N5518, 2N5523 MIN	2N5518, 2N5523 MAX	2N5519, 2N5524 MIN	2N5519, 2N5524 MAX	UNITS
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current	V_{DG} = 20V, I_D = 200 μA	125°C		10		10		10		10		10	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 20V, V_{GS} = 0, (Note 1)		0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage	V_{DG} = 20V, I_D = 200 μA			5		5		10		15		15	mV
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate Source Voltage Differential Drift, (Note 1)		T_A = 25°C, T_B = 125°C		5		10		20		40		80	μV/°C
			T_A = −55°C, T_B = 25°C		5		10		20		40		80	
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		f = 1 kHz		0.1		0.1		0.1		0.1		0.1	μmho
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio, (Note 1)			0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	
CMRR	Common-Mode Rejection Ratio, (Note 2)	V_{DD} = 10 to 20V, I_D = 200 μA		100		100		90						dB

Note 1: Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

Note 2: CMRR = 20 $\log_{10} \Delta V_{DD} / \Delta \lvert V_{GS1} - V_{GS2} \rvert$, ($\Delta V_{DD}$ = 10V).