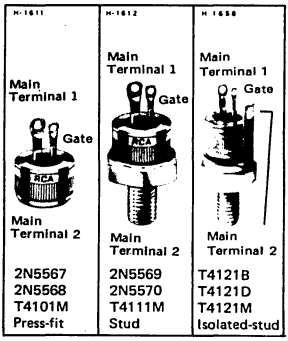
RCA
Solid State
Division

Thyristors
2N5567 – 2N5570
T4101 T4111 T4121 Series



10-A Silicon Triacs

Features:

- di/dt Capability = 150 A/μs
- Shorted-Emitter, Center-Gate Design
- Low Switching Losses
- Low On-State Voltage at High Current Levels
- Low Thermal Resistance

Package \ Voltage	200 V Types	400 V Types	600 V Types
Press-Fit (T4101 Series)	2N5567	2N5568	T4101M (40795)
Stud (T4111 Series)	2N5569	2N5570	T4111M (40796)
Isolated-Stud (T4121 Series)	T4121B (40799)	T4121D (40800)	T4121M (40801)

Numbers in parentheses (e.g. 40799) are former RCA type numbers.

These RCA triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate triggering voltages.

These triacs are intended for control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching systems.

MAXIMUM RATINGS, *Absolute-Maximum Values:*
For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

		2N5567 2N5569 T4121B	2N5568 2N5570 T4121D	T4101M T4111M T4121M	
***REPETITIVE PEAK OFF-STATE VOLTAGE:●**					
Gate open, T_J = −65 to 100° C	V_{DROM}	200	400	600	V
***RMS ON-STATE CURRENT (Conduction angle = 360°):**					
Case temperature (T_C) = 85° C	$I_{T(RMS)}$	10			A
For other conditions		See *Fig. 3*			
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}				
For one cycle of applied principal voltage, T_C = 85° C					
* 60 Hz (sinusoidal)		100			A
50 Hz (sinusoidal)		85			A
For more than one cycle of applied principal voltage		See *Fig. 4*			
RATE-OF-CHANGE OF ON-STATE CURRENT:					
V_{DM}= V_{DROM}, I_{GT} = 160 mA, t_r = 0.1 μs (See *Fig. 13)*	di/dt	150			A/μs
FUSING CURRENT (for Triac Protection):					
T_J = −65 to 100°C, t = 1.25 to 10 ms	I^2t	50			A^2s
PEAK GATE-TRIGGER CURRENT:■					
For 1 μs max.,See *Fig. 7*	I_{GTM}	4			A
***GATE POWER DISSIPATION:**					
PEAK (For 1 μs max., $I_{GTM} \leq 4$ A, See *Fig. 7)*	P_{GM}	16			W
AVERAGE	$P_{G(AV)}$	0.5			W
***TEMPERATURE RANGE:▲**					
Storage	T_{stg}	−65 to 150			°C
Operating (Case)	T_C	−65 to 100			°C
***TERMINAL TEMPERATURE (During soldering):**					
For 10 s max. (terminals and case)	T_T	225			°C
STUD TORQUE:	τ_s				
Recommended		35			in-lb
Maximum (DO NOT EXCEED)		50			in-lb

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.
● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.
▲ For temperature measurement reference point, see Dimensional Outline.

ELECTRICAL CHARACTERISTICS

At Maximum Ratings and at Indicated Case Temperature (T_C) Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Peak Off-State Current:♦ Gate open, T_J = 100° C, V_{DROM} = Max. rated value	I_{DROM}	–	0.1	2*	mA
Maximum On-State Voltage:♦ For i_T = 14 A (peak), T_C = 25° C	V_{TM}	–	1.35	1.65*	V
DC Holding Current:♦ Gate open, Initial principal current = 500 mA (DC), v_D = 12V:					
T_C = 25° C	I_{HO}	–	15	30	mA
T_C = −65° C		–	75	200*	
For other case temperatures			See *Fig. 6*		
Critical Rate-of-Rise of Commutation Voltage:♦ For v_D = V_{DROM}, $I_{T(RMS)}$ = 10 A, commutating di/dt = 5.4 A/ms, gate unenergized, T_C = 85° C (See *Fig. 14*)	dv/dt	2*	5	–	V/μs
Critical Rate-of-Rise of Off-State Voltage:♦ For v_D = V_{DROM}, exponential voltage rise, gate open, T_C = 100° C:					
2N5567, 2N5569, T4121B	dv/dt	30*	150	–	V/μs
2N5568, 2N5570, T4121D		20*	100	–	
T4101M, T4111M, T4121M		10	75	–	
DC Gate-Trigger Current:♦♦ For v_D = 12 V (DC), R_L = 30 Ω, T_C = 25° C — Mode / V_{MT2} / V_G	I_{GT}				mA
I^+ positive positive		–	10	25	
III^- negative negative		–	10	25	
I^- positive negative		–	20	40	
III^+ negative positive		–	20	40	
For v_D = 12 V (DC), R_L = 30 Ω, T_C = −65° C — Mode / V_{MT2} / V_G					
I^+ positive positive		–	45	100*	
III^- negative negative		–	45	100*	
I^- positive negative		–	80	150*	
III^+ negative positive		–	80	150*	
For other case temperatures			See *Figs. 8 & 9*		
DC Gate-Trigger Voltage:♦♦ For v_D = 12 V(DC), R_L = 30 Ω					
T_C = 25° C	V_{GT}		1	2.5	V
T_C = −65° C			2	4*	
For other case temperatures			See *Fig. 10*		
For v_D = V_{DROM}, R_L = 125 Ω, T_C = 100° C		0.2	–	–	
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For v_D = V_{DROM}, I_{GT} = 160 mA, t_r = 0.1 μs, i_T = 15 A (peak), T_C = 25° C (See *Figs. 11 & 15*)	t_{gt}	–	1.6	2.5	μs
Thermal Resistance: **Junction-to-Case:** Steady-State	$\theta_{J\text{-}C}$	–	–	1*	°C/W
Transient			See *Fig. 12*		
Junction-to-Isolated Hex (Stud, see Dim. Outline): Steady-State	$\theta_{J\text{-}IH}$	–	–	1.1	

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.

♦ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

♦ For either polarity of gate voltage (V_G) with reference to main terminal 1.

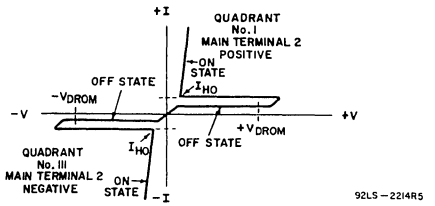


Fig. 1 – Principal voltage-current characteristic.

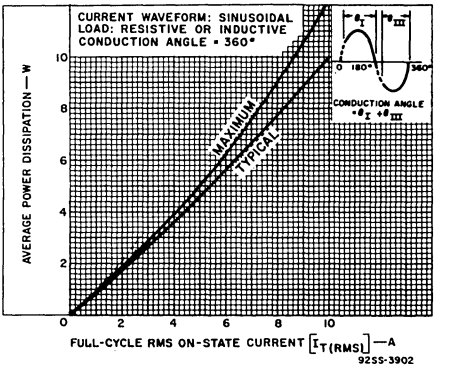


Fig. 2 – Power dissipation vs. on-state current.

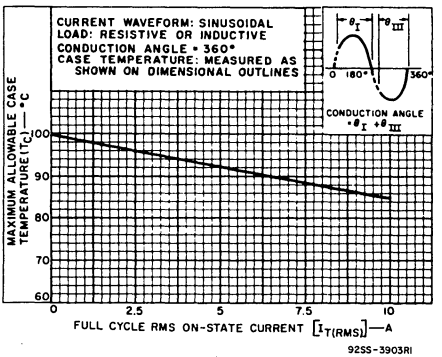


Fig. 3 – Maximum allowable case temperature vs. on-state current.

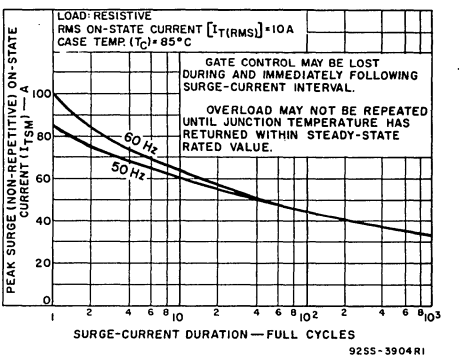


Fig. 4 – Peak surge on-state current vs. surge current duration.

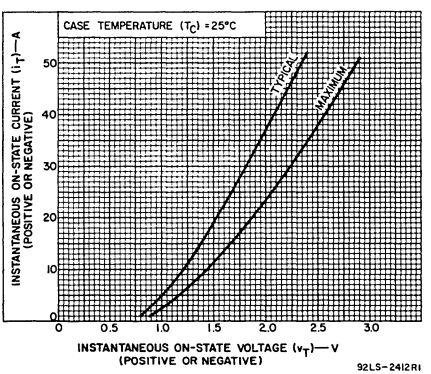


Fig. 5 – On-state current vs. on-state voltage.

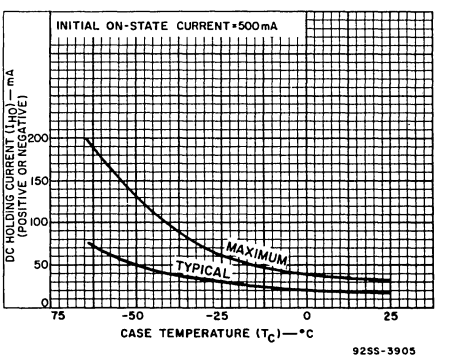


Fig. 6 – DC holding current vs. case temperature.

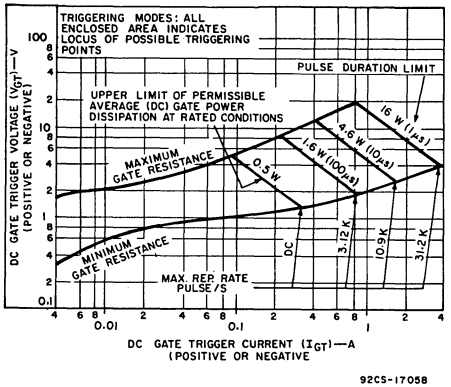


Fig. 7 – Gate trigger characteristics and limiting conditions for determination of permissible gate trigger pulses.

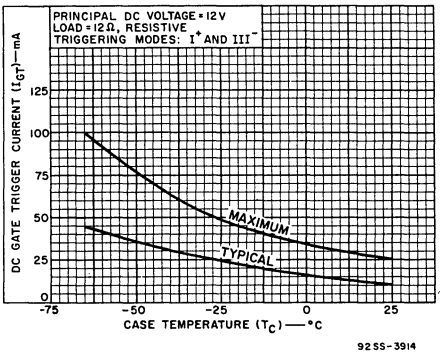


Fig. 8 – DC gate-trigger current vs. case temperature (1^+ & III^- modes).

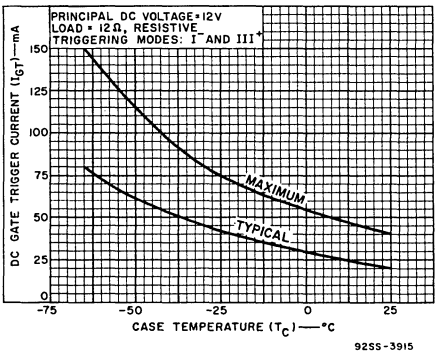


Fig. 9 – DC gate-trigger current vs. case temperature (1^- & III^+ modes).

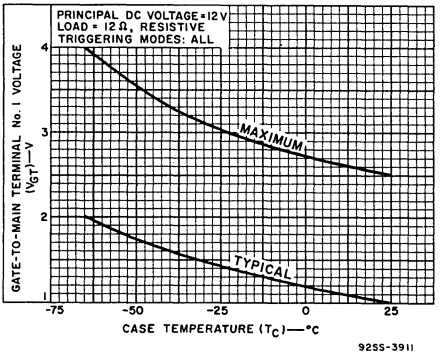


Fig. 10 – DC gate-trigger voltage vs. case temperature.

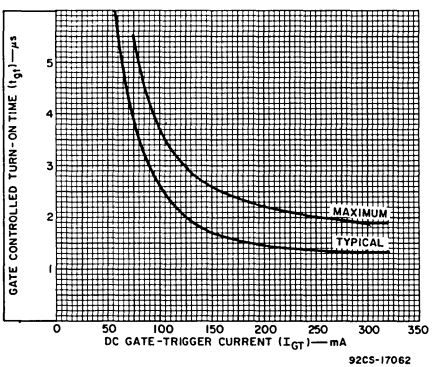


Fig. 11 – Turn-on time vs. gate trigger current.

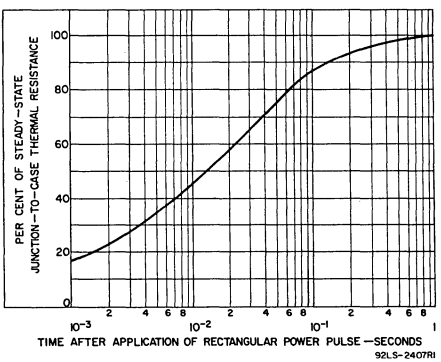


Fig. 12 – Transient junction-to-case thermal resistance vs. time.

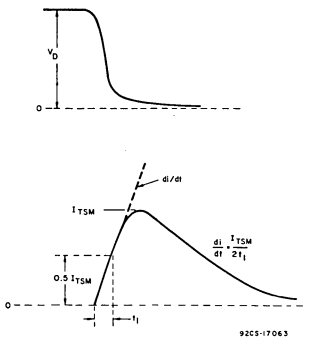


Fig. 13 – Rate-of-change of on-state current with time (defining di/dt).

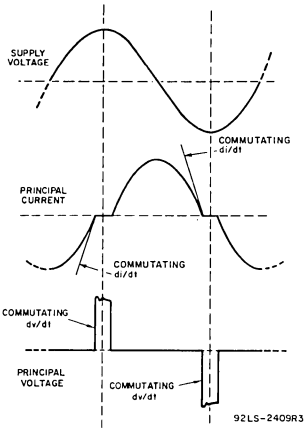


Fig. 14—Relationship between supply voltage and prinicpal current (inductive load) showing reference points for definition of commutating voltage (dv/dt).

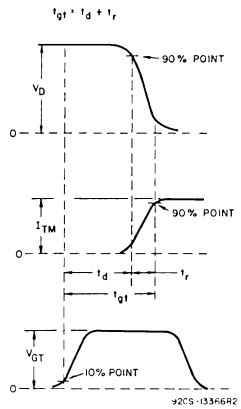


Fig. 15—Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).

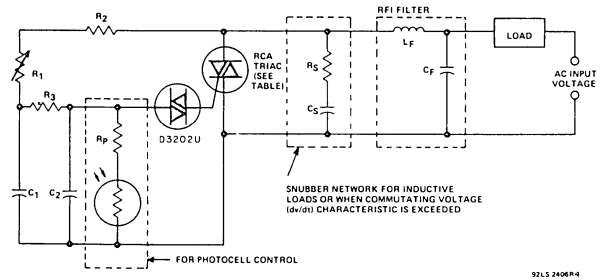


Fig. 16 – Typical phase-control circuit for lamp dimming, heat control, and universal-motor speed control.

AC INPUT VOLTAGE		120V 60Hz	240V 60Hz	240V 50Hz
C_1		0.1μF 200V	0.1μF 400V	0.1μF 400V
C_2		0.1μF 100V	0.1μF 100V	0.1μF 100V
R_1		100KΩ 1/2W	200KΩ 1W	250KΩ 1W
R_2		2.2KΩ 1/2W	3.3KΩ 1/2W	3.3KΩ 1/2W
R_3		15KΩ 1/2W	15KΩ 1/2W	15KΩ 1/2W
PHOTOCELL CONTROL	R_P	1.2KΩ 2W	1.2KΩ 2W	1.2KΩ 2W
SNUBBER NETWORK	C_S	0.1 μF 200V	0.1μF 400V	0.1μF 400V
	R_S	100Ω 1/2W	100Ω 1/2W	100Ω 1/2W
RFI FILTER	C_F*	0.1μF 200V	0.1μF 400V	0.1μF 400V
	L_F*	100μH	200μH	200μH
RCA TRIACS		2N5567 2N5569 T4121B	2N5568 2N5570 T4121D	2N5568 2N5570 T4121D

*Typical values for lamp dimming circuits.

WARNING:
The RCA isolated-stud package thyristors should be handled with care. The ceramic portion of these thyristors contains BERYLLIUM OXIDE as a major ingredient. Do not crush, grind, or abrade these portions of the thyristors because the dust resulting from such action may be hazardous if inhaled.

TERMINAL CONNECTIONS

No.1–Gate
No.2–Main Terminal 1
No.3–Main Terminal 2