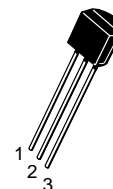
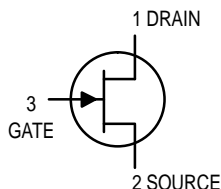


JFETs Switching

N-Channel — Depletion

2N5640



CASE 29-04, STYLE 5
TO-92 (TO-226AA)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Reverse Gate-Source Voltage	V_{GSR}	30	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	350 2.8	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	357	°C/W
Junction Temperature Range	T_J	-65 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage ($I_G = 10 \mu\text{Adc}$, $V_{DS} = 0$)	$V_{(BR)GSS}$	30	—	Vdc
Gate Reverse Current ($V_{GS} = -15 \text{ Vdc}$, $V_{DS} = 0$) ($V_{GS} = -15 \text{ Vdc}$, $V_{DS} = 0$, $T_A = 100^\circ\text{C}$)	I_{GSS}	—	1.0 1.0	nAdc μAdc
Drain Cutoff Current ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = -6.0 \text{ Vdc}$) ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = -6.0 \text{ Vdc}$, $T_A = 100^\circ\text{C}$)	$I_{D(off)}$	—	1.0 1.0	nAdc μAdc
ON CHARACTERISTICS				
Zero-Gate-Voltage Drain Current ⁽¹⁾ ($V_{DS} = 20 \text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}	5.0	—	mAdc
Drain-Source On-Voltage ($I_D = 3.0 \text{ mAdc}$, $V_{GS} = 0$)	$V_{DS(on)}$	—	0.5	Vdc
Static Drain-Source On Resistance ($I_D = 1.0 \text{ mAdc}$, $V_{GS} = 0$)	$r_{DS(on)}$	—	100	Ohms

1. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 3.0\%$.

2N5640**ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
SMALL-SIGNAL CHARACTERISTICS				
Static Drain-Source "ON" Resistance ($V_{GS} = 0, I_D = 0, f = 1.0 \text{ kHz}$)	$r_{ds(on)}$	—	100	Ohms
Input Capacitance ($V_{DS} = 0, V_{GS} = -12 \text{ Vdc}, f = 1.0 \text{ MHz}$)	C_{iss}	—	10	pF
Reverse Transfer Capacitance ($V_{DS} = 0, V_{GS} = -12 \text{ Vdc}, f = 1.0 \text{ MHz}$)	C_{rss}	—	4.0	pF

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$V_{DD} = 10 \text{ Vdc},$ $V_{GS(on)} = 0,$ $V_{GS(off)} = -10 \text{ Vdc},$ $R_G' = 50 \Omega$	$I_{D(on)} = 3.0 \text{ mAdc}$	$t_{d(on)}$	—	8.0	ns
Rise Time		$I_{D(on)} = 3.0 \text{ mAdc}$	t_r	—	10	ns
Turn-Off Delay Time		$I_{D(on)} = 3.0 \text{ mAdc}$	$t_{d(off)}$	—	15	ns
Fall Time		$I_{D(on)} = 3.0 \text{ mAdc}$	t_f	—	30	ns

TYPICAL SWITCHING CHARACTERISTICS

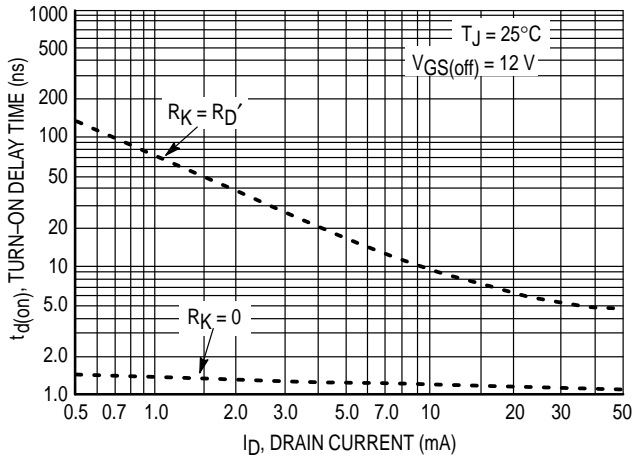


Figure 1. Turn-On Delay Time

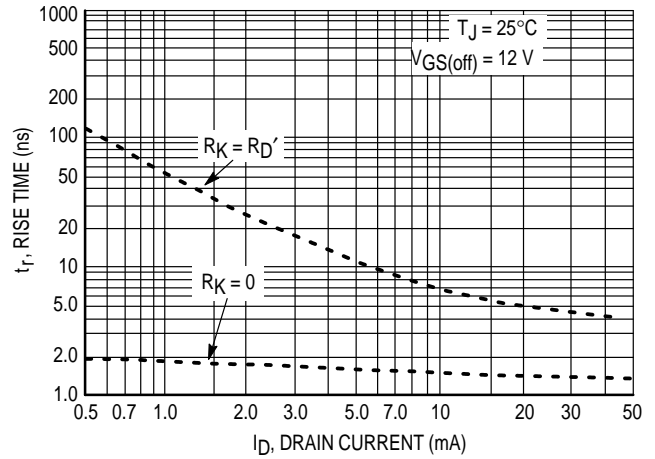


Figure 2. Rise Time

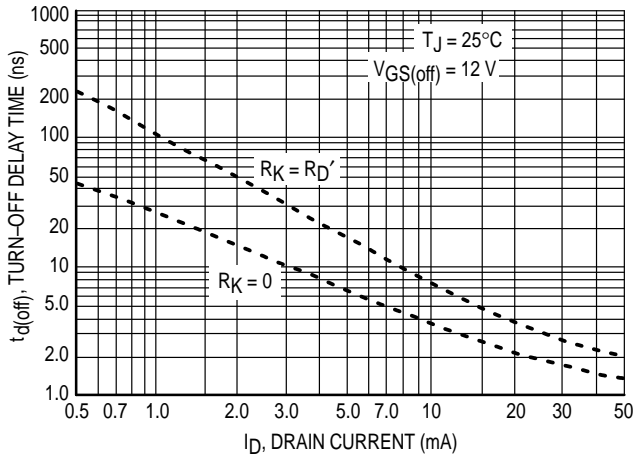


Figure 3. Turn-Off Delay Time

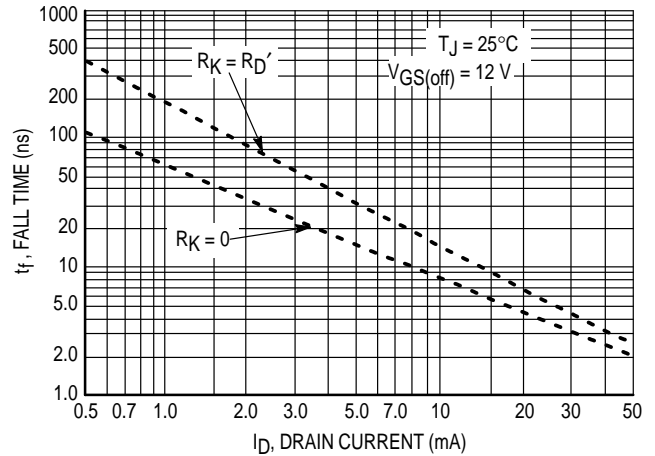


Figure 4. Fall Time

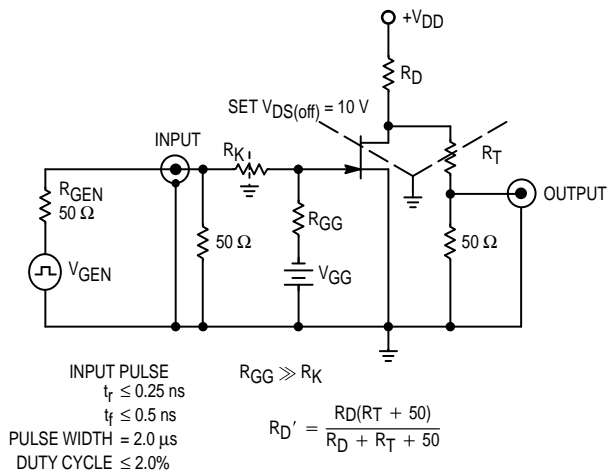


Figure 5. Switching Time Test Circuit

NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain-Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{RSS}) or Gate-Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn-on interval, Gate-Source Capacitance (C_{GS}) discharges through the series combination of R_{GEN} and R_K . C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain-Source Resistance (r_{DS}). During the turn-off, this charge flow is reversed.

Predicting turn-on time is somewhat difficult as the channel resistance r_{DS} is a function of the gate-source voltage. While C_{GS} discharges, V_{GS} approaches zero and r_{DS} decreases. Since C_{gd} discharges through r_{DS} , turn-on time is non-linear. During turn-off, the situation is reversed with r_{DS} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to R_D , which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

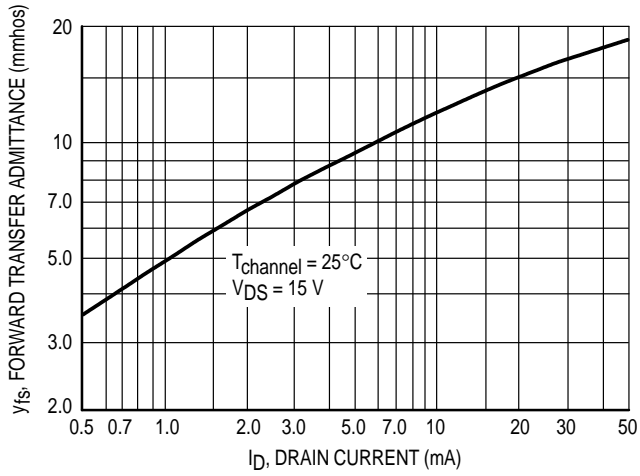


Figure 6. Typical Forward Transfer Admittance

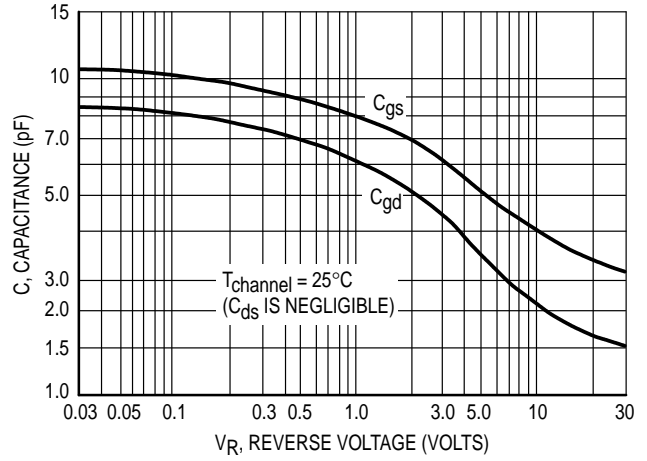


Figure 7. Typical Capacitance

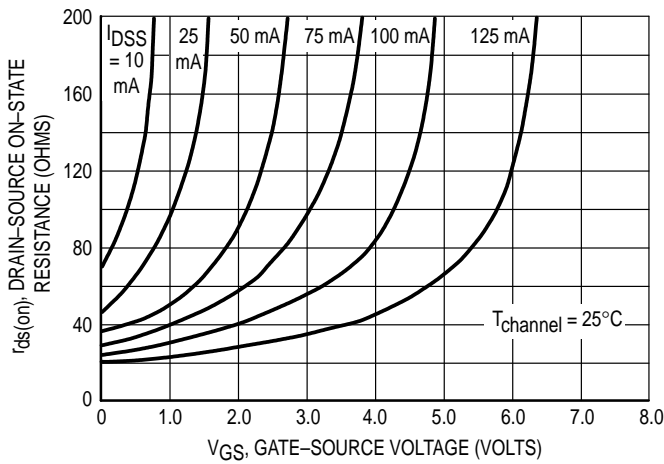


Figure 8. Effect of Gate-Source Voltage On Drain-Source Resistance

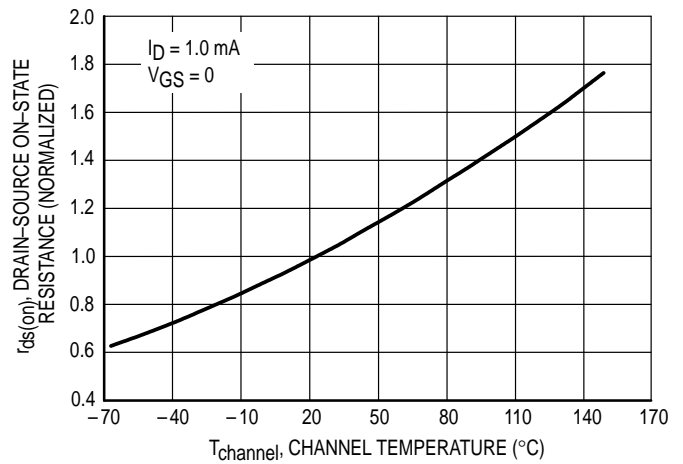


Figure 9. Effect of Temperature On Drain-Source On-State Resistance

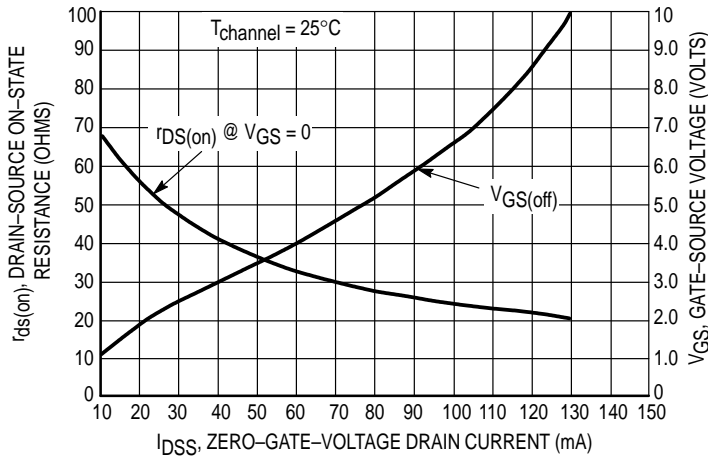
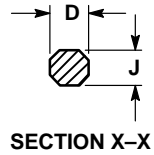
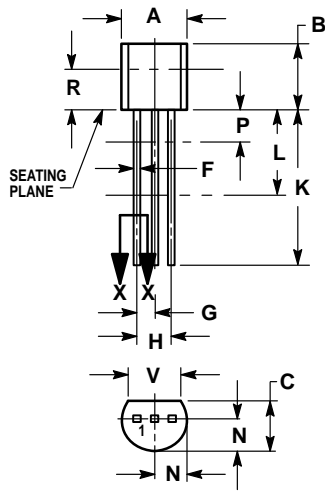


Figure 10. Effect of I_{DSS} On Drain-Source Resistance and Gate-Source Voltage

NOTE 2

The Zero-Gate-Voltage Drain Current (I_{DSS}), is the principle determinant of other J-FET characteristics. Figure 10 shows the relationship of Gate-Source Off Voltage ($V_{GS(off)}$) and Drain-Source On Resistance ($r_{ds(on)}$) to I_{DSS} . Most of the devices will be within $\pm 10\%$ of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

PACKAGE DIMENSIONS



SECTION X-X

**CASE 029-04
(TO-226AA)
ISSUE AD**


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K. MINIMUM LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

STYLE 5:

- PIN 1. DRAIN
2. SOURCE
3. GATE

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