

2N5668 (SILICON)

2N5669

2N5670

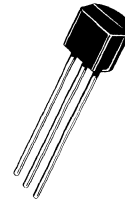
SILICON N-CHANNEL  
JUNCTION FIELD-EFFECT TRANSISTORS

Depletion Mode (Type A) Junction Field-Effect Transistors designed for VHF amplifier and mixer applications.

- Low Cross Modulation and Intermodulation Distortion
- Drain and Source Interchangeable
- Low 100-MHz Noise Figure – NF = 2.5 dB (Max)
- Low Reverse Transfer and Input Capacitances –  $C_{rss} = 1.0$  pF (Typ);  $C_{iss} = 4.7$  pF (Typ)
- High Maximum Stable Gain Due to Drain and Gate Lead Separation

N-CHANNEL  
JUNCTION FIELD-EFFECT  
TRANSISTORS

(Type A)

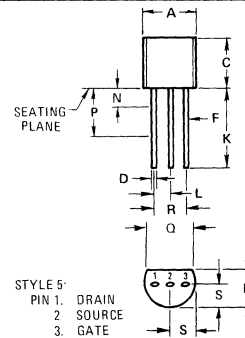


\*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	25	Vdc
*Drain-Gate Voltage	$V_{DG}$	25	Vdc
*Reverse Gate-Source Voltage	$V_{GSR}$	25	Vdc
*Forward Gate Current	$I_{GF}$	10	mA <sub>dc</sub>
Drain Current	$I_D$	20	mA <sub>dc</sub>
*Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D^{(1)}$	310 2.82	mW mW/ $^\circ\text{C}$
*Storage Temperature Range	$T_{stg}^{(1)}$	-65 to +150	$^\circ\text{C}$

\*Indicates JEDEC Registered Data.

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows:  $P_D = 1.0$  W @  $T_C = 25^\circ\text{C}$ , Derate above  $25^\circ\text{C} - 8.0$  mW/ $^\circ\text{C}$ ,  $T_J = -65$  to  $+150^\circ\text{C}$ ,  $\theta_{JC} = 125^\circ\text{C}/\text{W}$ .



STYLE 5:  
PIN 1. DRAIN  
2. SOURCE  
3. GATE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	—	0.500	—
L	1.150	1.390	0.045	0.055
N	—	1.270	—	0.050
P	6.350	—	0.250	—
Q	3.430	—	0.135	—
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02  
TO-92

# 2N5668, 2N5669, 2N5670 (continued)

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
<b>*OFF CHARACTERISTICS</b>						
Gate-Source Breakdown Voltage ( $I_G = 10 \mu\text{A dc}$ , $V_{DS} = 0$ )	$V_{(BR)GSS}$	25	—	—	Vdc	
Gate-Source Cutoff Voltage ( $V_{DS} = 15 \text{ Vdc}$ , $I_D = 10 \text{ nAdc}$ )	$V_{GS(off)}$	2N5668 2N5669 2N5670	0.2 1.0 2.0	— — —	4.0 6.0 8.0	Vdc
Gate Reverse Current ( $V_{GS} = -15 \text{ Vdc}$ , $V_{DS} = 0$ ) ( $V_{GS} = -15 \text{ Vdc}$ , $V_{DS} = 0$ , $T_A = 100^\circ\text{C}$ )	$I_{GSS}$	—	—	2.0	nAdc $\mu\text{Adc}$	

**\*ON CHARACTERISTICS**

Zero-Gate Voltage Drain Current (Note 1) ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ )	$I_{DSS}$	2N5668 2N5669 2N5670	1.0 4.0 8.0	— — —	5.0 10 20	mAdc
--	-----------	----------------------------	-------------------	-------------	-----------------	------

**SMALL-SIGNAL CHARACTERISTICS**

*Forward Transadmittance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	$ y_{fs} $	2N5668 2N5669 2N5670	1500 2000 3000	— — —	6500 6500 7500	$\mu\text{mhos}$
*Forward Transconductance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 100 \text{ MHz}$ )	$\text{Re}(y_{fs})$	2N5668 2N5669 2N5670	1000 1600 2500	— — —	— — —	$\mu\text{mhos}$
*Output Admittance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	$ y_{os} $	2N5668 2N5669 2N5670	— — —	— — —	20 50 75	$\mu\text{mhos}$
*Output Conductance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 100 \text{ MHz}$ )	$\text{Re}(y_{os})$	2N5668 2N5669 2N5670	— — —	10 25 35	50 100 150	$\mu\text{mhos}$
*Input Conductance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 100 \text{ MHz}$ )	$\text{Re}(y_{is})$	—	—	125	800	$\mu\text{mhos}$
*Input Capacitance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	$C_{iss}$	—	—	4.7	7.0	pF
*Reverse Transfer Capacitance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	$C_{rss}$	—	—	1.0	3.0	pF
Output Capacitance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	$C_{oss}$	—	—	1.4	4.0	pF
*Common Source Noise Figure (Figure 1) ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 100 \text{ MHz}$ , at $R_G = 1.0 \text{ k ohm}$ )	NF	—	—	—	2.5	dB
Power Gain (Figure 1) ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 100 \text{ MHz}$ )	$G_{ps}$	—	—	—	16	dB

\*Indicates JEDEC Registered Data, excluding typical values.  
Note 1: Pulse Test: Pulse Width = 100 ms, Duty Cycle  $\leq 10\%$ .

**FIGURE 1 – 100 MHz, POWER GAIN AND NOISE FIGURE TEST CIRCUIT**

