2N5716 (SILICON)
2N5717
2N5718

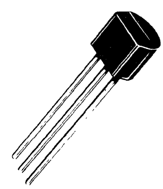
SILICON LOW NOISE N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

Depletion Mode Junction Field-Effect Transistors designed for audio amplifiers in low-power or battery operated applications.

- Low Zero-Gate-Voltage Drain Current @ V_{DS} = 15 Vdc –
  I_{DSS} = 50 μAdc to 250 μAdc – 2N5716
  200 μAdc to 1.0 mAdc – 2N5717
  800 μAdc to 4.0 mAdc – 2N5718
- High Forward Transadmittance @ V_{DS} = 15 Vdc, f = 1.0 kHz –
  $|y_{fs}|$ = 350 μmhos (Typ) @ I_D = 50 μAdc – 2N5716
  550 μmhos (Typ) @ I_D = 200 μAdc – 2N5717
  900 μmhos (Typ) @ I_D = 800 μAdc – 2N5718
- Low Noise Voltage –
  $e_n = 75\ nV/\sqrt{Hz}$ (Max) @ f = 1.0 kHz
- Drain and Source Interchangeable

LOW NOISE N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

$e_n = 75\ nV/\sqrt{Hz}$



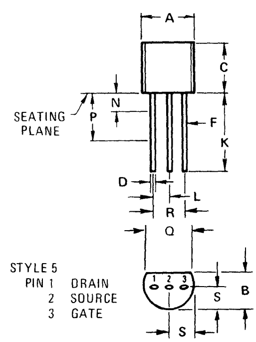
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	40	Vdc
Reverse Gate-Source Voltage	V_{GSR}	40	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Operating Channel Temperature	$T_{channel}$	150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.

MECHANICAL CHARACTERISTICS:

Maximum Lead Temperature for Soldering:
240°C, not less than 1/16" from case for 10 s.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Gate-Drain Breakdown Voltage (I_D = 1.0 μAdc, I_S = 0)		$V_{(BR)GSS}$	40	–	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 nAdc)	2N5716	$V_{GS(off)}$	0.2	3.0	Vdc
	2N5717		0.5	5.0	
	2N5718		1.0	8.0	
Gate Reverse Current		I_{GSS}			
(V_{GS} = 20 Vdc, V_{DS} = 0)			–	1.0	nAdc
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C)			–	1.0	μAdc
***ON CHARACTERISTICS**					
Zero-Gate Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5716	I_{DSS}	0.05	0.25	mAdc
	2N5717		0.2	1.0	
	2N5718		0.8	4.0	
SMALL-SIGNAL CHARACTERISTICS					
*Forward Transadmittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5716	$\|y_{fs}\|$	200	1000	μmhos
	2N5717		400	1600	
	2N5718		500	2000	
*Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		$\|y_{os}\|$	–	25	μmhos
*Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	5.0	pF
*Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	pF
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz, BW = 1.0 Hz)		e_n	–	75	nV/√Hz

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤630 ms, Duty Cycle ≤ 10%

TYPICAL SMALL-SIGNAL CHARACTERISTICS

FIGURE 1 – FORWARD TRANSFER ADMITTANCE

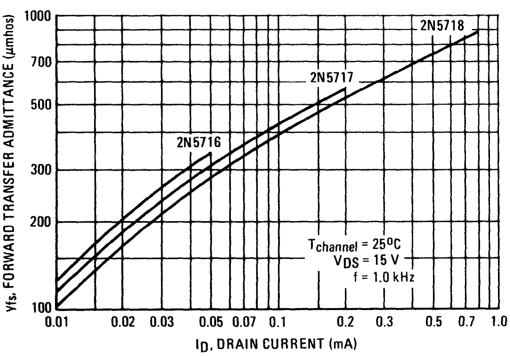
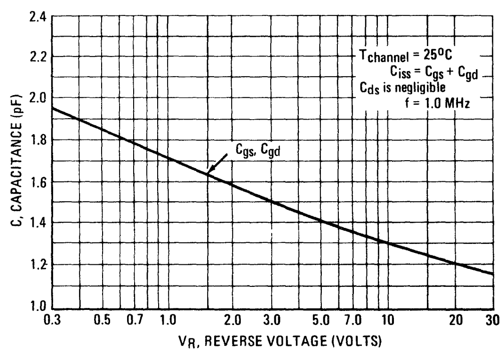
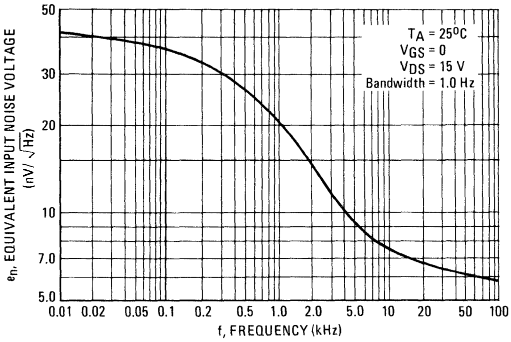


FIGURE 2 – CAPACITANCE



NOISE DATA

FIGURE 3 – TYPICAL NOISE VOLTAGE



In a junction field-effect transistor, the current flow is due to carrier drift, therefore total noise at the input may be expressed as

$$V_T = \left[e^2_n + 4\,K\,T\,R_S \right]^{1/2}$$

where V_T = total noise voltage at the FET input (volts/$\sqrt{Hz}$)
e_n = noise voltage of the FET referred to the input (Figure 3).
K = Boltzman's constant (1.38 x 10^{-23} j/°K)
T = temperature of the source resistance (°K)
R_S = source resistance (ohms)

Example:
Find the total noise at the input of a 2N5716 FET with a source impedance of 10 kilohms at a frequency of 1.0 kHz and at a temperature of 25°C.

Read e_n = 20.5 nV/$\sqrt{Hz}$ from Figure 3. (Note that this is for a one cycle bandwidth).

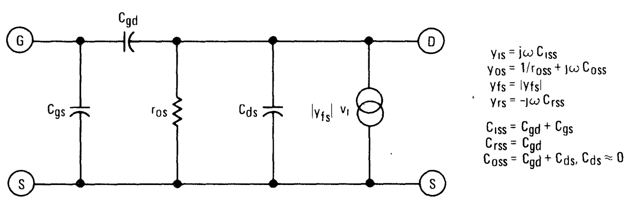
$$V_T = [(20.5 \times 10^{-9})^2 + (4)(1.38 \times 10^{-23}(300)(1 \times 10^4)]^{1/2}$$
$$= 24.2\ nV/\sqrt{Hz}$$

Noise over a frequency band can be handled in one of two ways depending upon whether FET noise is constant or variable over the bandwidth of interest.

1. For constant FET noise, multiply V_T by the square root of bandwidth, i.e., $V'_T = V_T \bullet \Delta f^{1/2}$
2. For variable FET noise, plot V'_T (where Δf = 1.0 Hz) versus frequency over the bandwidth and integrate the result.

Total noise voltage at the output of the FET stage can be found by multiplying V_T by the voltage gain of the stage.

FIGURE 4 – LOW FREQUENCY CIRCUIT MODEL



TYPICAL LIMIT TRANSFER CHARACTERISTICS

(Temperatures Noted are $T_{channel}$)

FIGURE 5 – 2N5716

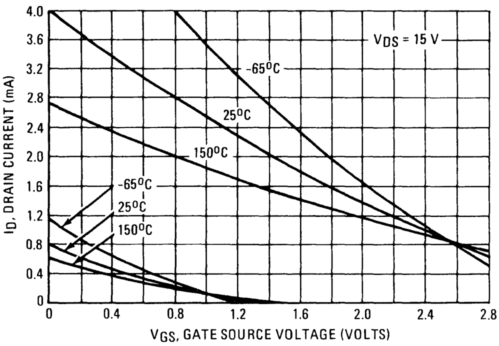


FIGURE 6 – 2N5717

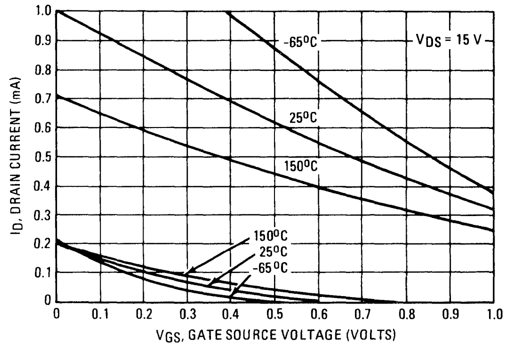


FIGURE 7 – 2N5718

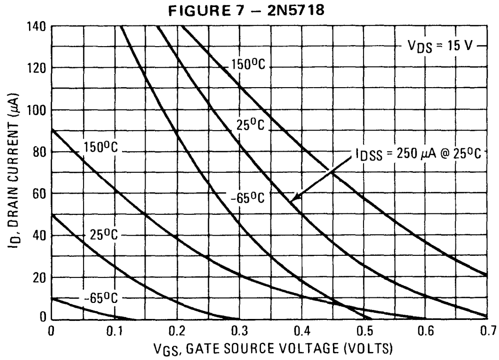
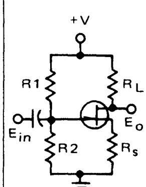
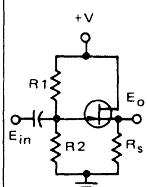
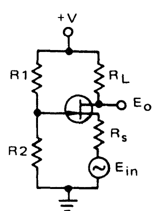


FIGURE 8 – AMPLIFIER EQUATIONS

Circuit Characteristic	Common Source	Source Follower	Common Gate
			
Voltage Gain	$A_v \approx \frac{-R_L}{\frac{1}{gm} + R_s}$	$A_v \approx \frac{R_s}{\frac{1}{gm} + R_s}$	$A_v \approx \frac{R_L}{\frac{1}{gm} + R_s}$
Input Impedance	$Z_{in} \approx R1 \| R2$	$Z_{in} \approx R1 \| R2$	$Z_{in} \approx R_s + \frac{1}{gm}$
Output Impedance	$Z_o \approx R_L$	$Z_o \approx R_s \| \frac{1}{gm}$	$Z_o \approx R_L$

2N5745 (SILICON)

For Specifications, See 2N4398, Volume I.