2N5745
(See 2N4398)

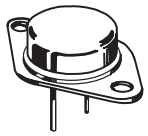
2N5758

High-Voltage High-Power Silicon Transistors

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- DC Current Gain @ I_C = 3.0 Adc —
  h_{FE} = 25 (Min)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 3.0 Adc

6 AMPERE
POWER TRANSISTOR
NPN SILICON
100 – 140 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N5758	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	6.0 10	Adc
Base Current	I_B	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857	Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

(1) Indicates JEDEC Registered Data.

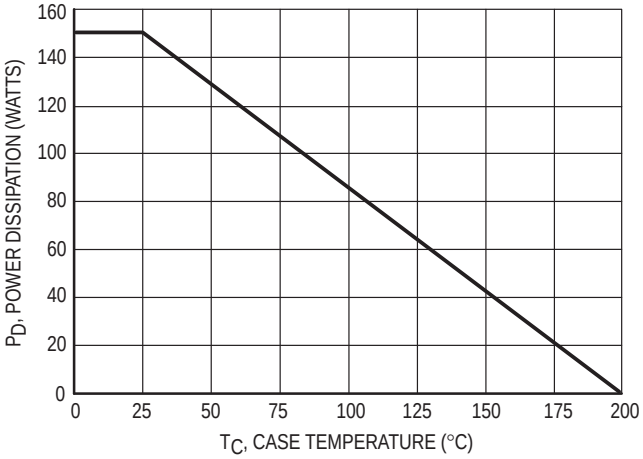


Figure 1. Power Derating

Safe area limits are indicated by Figure 5. Both limits are applicable and must be observed.

REV 7

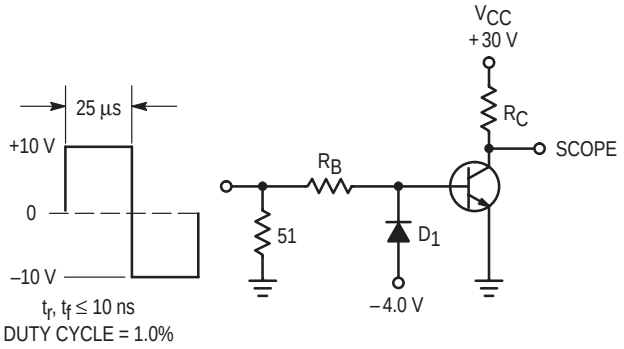
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	—	1.0	mAdc
Emitter–Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	 25 5.0	 100 —	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc) (I_C = 6.0 Adc, I_B = 1.2 Adc)	$V_{CE(sat)}$	 — —	 1.0 2.0	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)	f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	300	pF
Small–Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	15	—	—

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$.



*For PNP test circuit, reverse all polarities and D1.

Figure 2. Switching Time Test Circuit

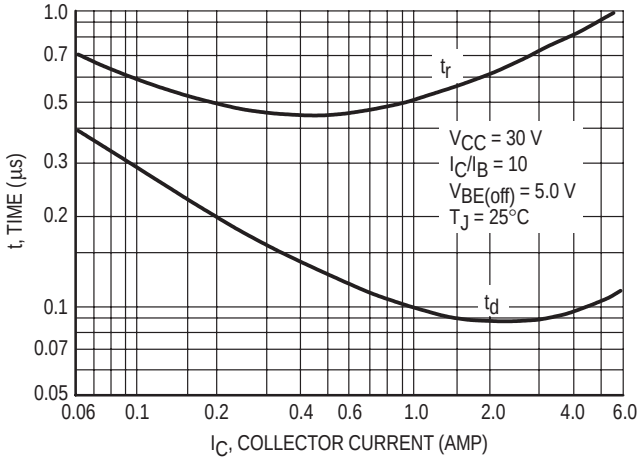


Figure 3. Turn–On Time

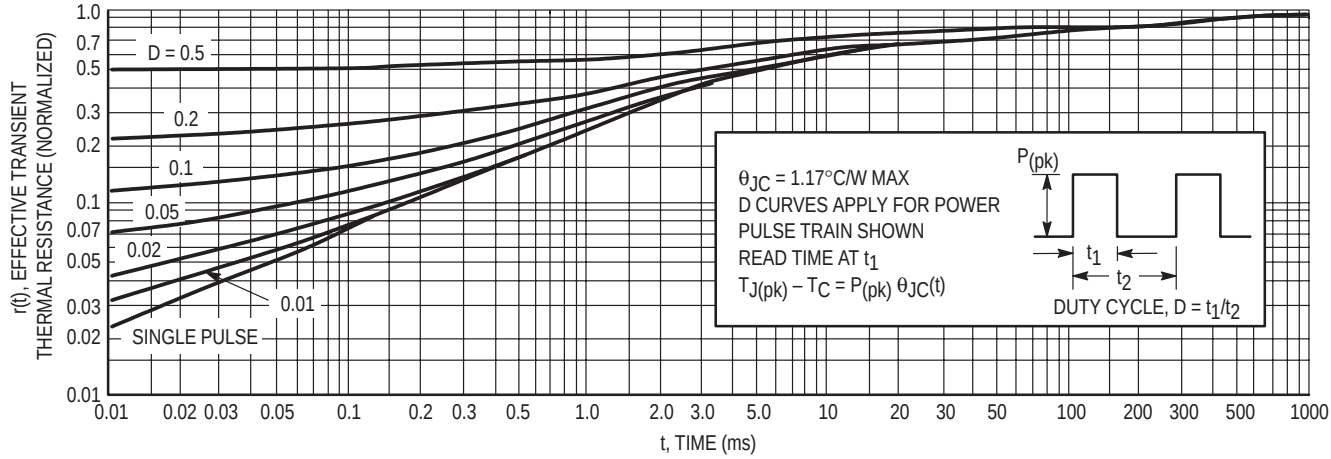


Figure 4. Thermal Response

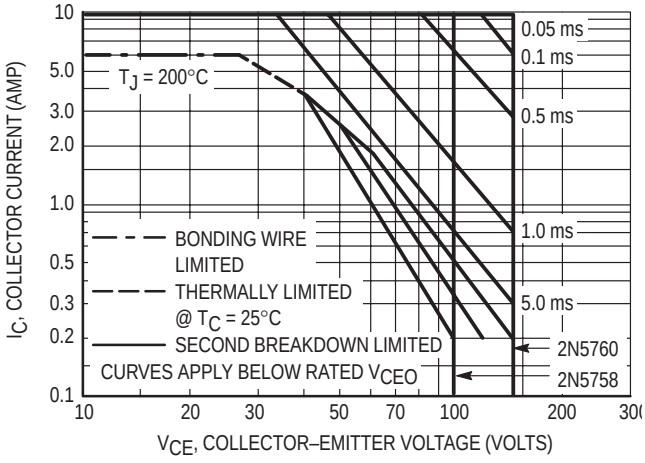


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

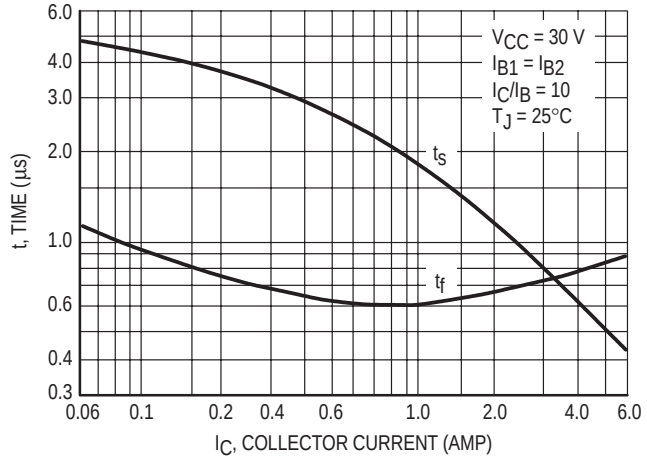


Figure 6. Turn–Off Time

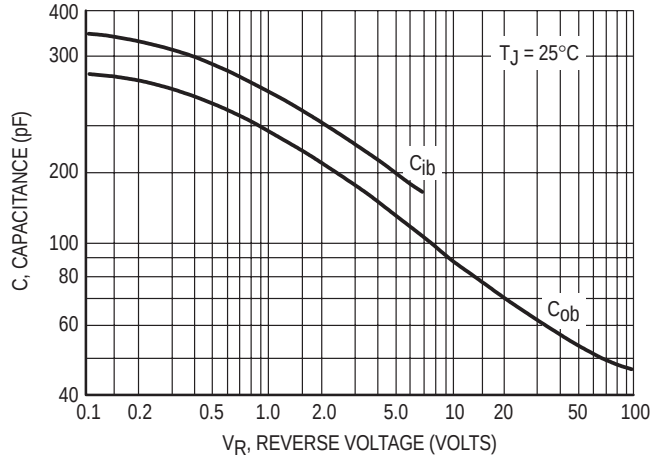


Figure 7. Capacitance

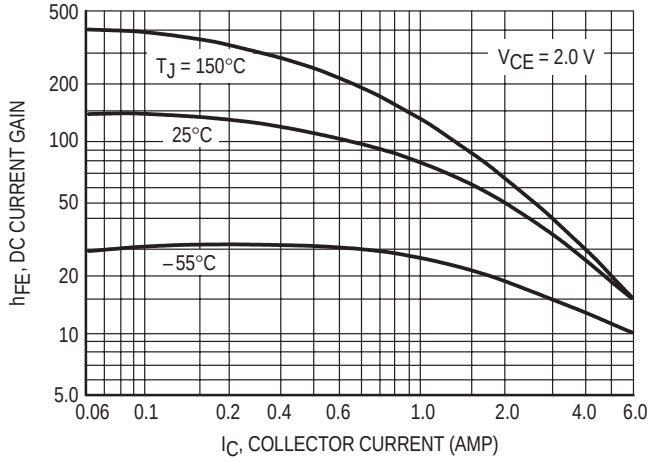


Figure 8. DC Current Gain