2N4957
2N4958
2N4959
2N5829

2N4957
JAN, JTX, JTXV AVAILABLE
CASE 20-03, STYLE 10
TO-72 (TO-206AF)

HIGH FREQUENCY TRANSISTOR

PNP SILICON

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	30	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		$V_{(BR)CBO}$	30	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	3.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0) (V_{CB} = 10 Vdc, I_E = 0, T_A = 150°C)		I_{CBO}	 — —	 — —	 0.1 100	μAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)		h_{FE}	20	40	150	—
SMALL SIGNAL CHARACTERISTICS						
Current-Gain — Bandwidth Product(1) (I_E = 2.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	 2N4957, 2N5829 2N4958, 2N4959	f_T	 1200 1000	 1600 1500	 2500 2500	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	—	0.4	0.8	pF
Small Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	200	—
Collector Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 10 Vdc, f = 63.6 MHz)		$r_b'C_c$	1.0	—	8.0	ps
Noise Figure (Figure 1) (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 450 MHz)	 2N5829 2N4957 2N4958 2N4959	NF	 — — — —	 2.3 2.6 2.9 3.2	 2.5 3.0 3.3 3.8	dB
FUNCTIONAL TEST						
Common-Emitter Amplifier Power Gain (Figure 1) (V_{CE} = 10 Vdc, I_C = 2.0 mAdc, f = 450 MHz)	 2N4957, 2N5829 2N4958 2N4959	G_{pe}	 17 16 15	 — — —	 25 25 25	dB

(1) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – NOISE FIGURE AND POWER GAIN TEST CIRCUIT

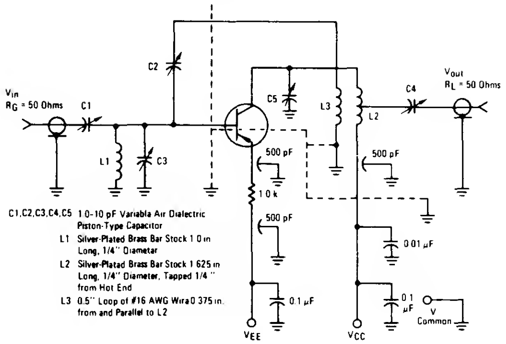


FIGURE 2 – UNILATERALIZED POWER GAIN versus FREQUENCY

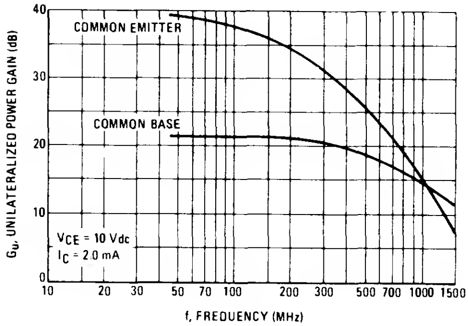


FIGURE 3 – NOISE FIGURE versus FREQUENCY

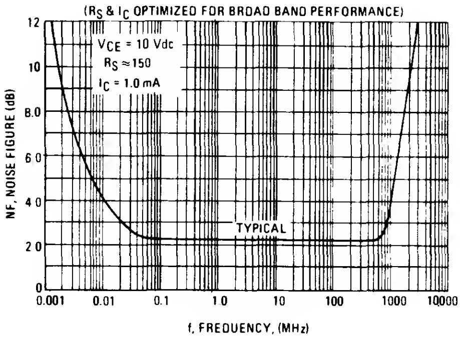


FIGURE 4 – NOISE FIGURE AND POWER GAIN versus COLLECTOR CURRENT

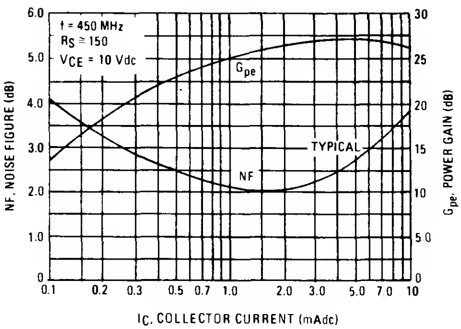


FIGURE 5 – CONTOURS OF NOISE FIGURE versus SOURCE RESISTANCE AND COLLECTOR CURRENT

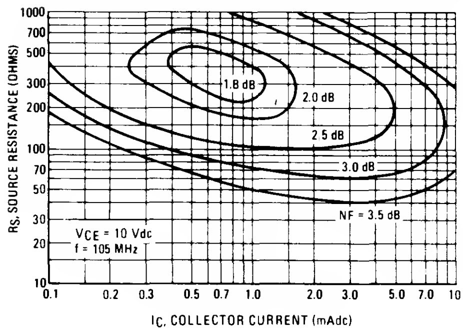
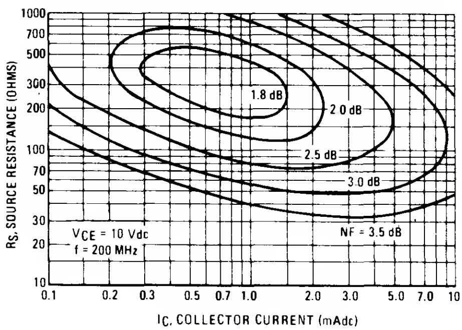


FIGURE 6 – CONTOURS OF NOISE FIGURE versus SOURCE RESISTANCE AND COLLECTOR CURRENT



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COMMON EMITTER CIRCUIT DESIGN DATA

(V_{CE} = 10 Vdc, I_C = 2.0 mAdc)

FIGURE 7 – TRANSDUCER GAIN versus FREQUENCY

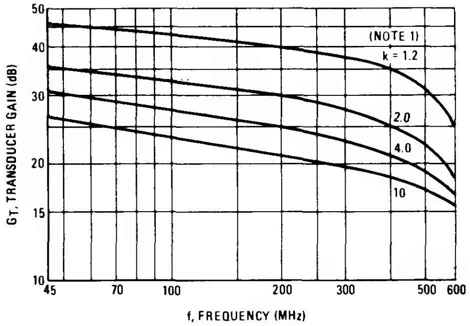


FIGURE 8 – LINVILL STABILITY FACTOR versus FREQUENCY

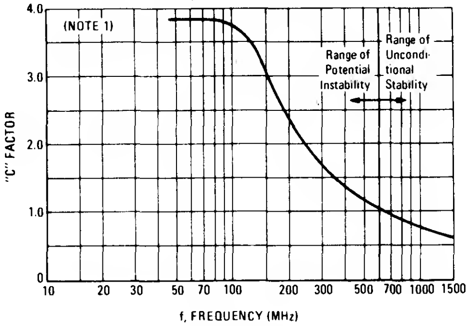


FIGURE 9 – LOAD ADMITTANCE versus FREQUENCY (REAL)

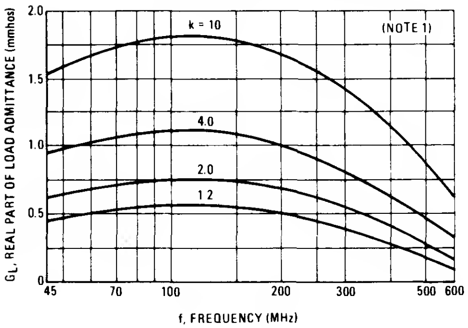


FIGURE 10 – LOAD ADMITTANCE versus FREQUENCY (IMAGINARY)

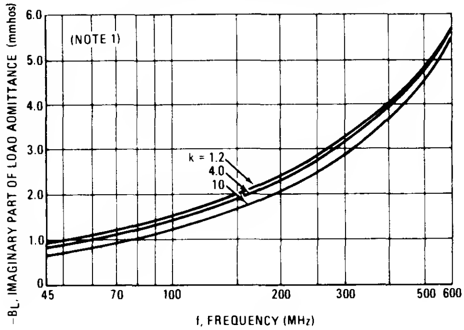


FIGURE 11 – SOURCE ADMITTANCE versus FREQUENCY (REAL)

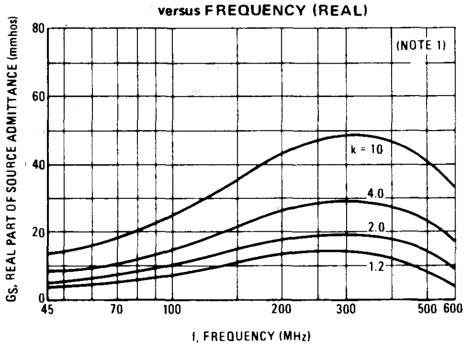
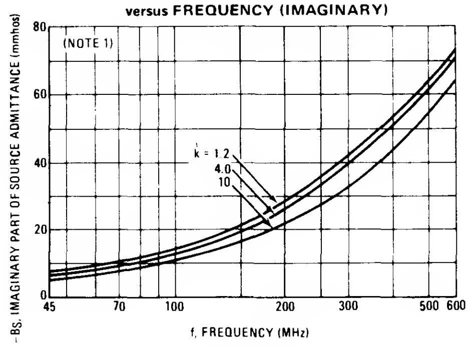


FIGURE 12 – SOURCE ADMITTANCE versus FREQUENCY (IMAGINARY)



NOTE 1

Figures 7 through 18 are included to assist the circuit designer in determining the stability of his particular circuit. Two stability criteria are given in these figures.

The Linvill "C" factor* is a measure of transistor stability when the input and output are terminated in the worst case (open circuit) condition. When "C" is less than 1.0, the circuit is unconditionally stable. When "C" is greater than 1.0, the circuit is potentially unstable.

The Stern "K" factor† has been defined to determine the stability of a practical amplifier terminated in finite load and source admittances. If "K" is greater than 1.0, the circuit will be stable. If less than 1.0, the circuit will be unstable. For further details, see Application Note AN 215A.

* "Transistors and Active Circuits," Linvill and Gibbons, McGraw Hill, 1961

† "Stability and Power Gain of Tuned Transistor Amplifiers," Arthur P. Stern, Proc I.R.E., March 1967

COMMON BASE CIRCUIT DESIGN DATA

(V_{CB} = 10 Vdc, I_C = 2.0 mAdc)

FIGURE 13 – TRANSDUCER GAIN versus FREQUENCY

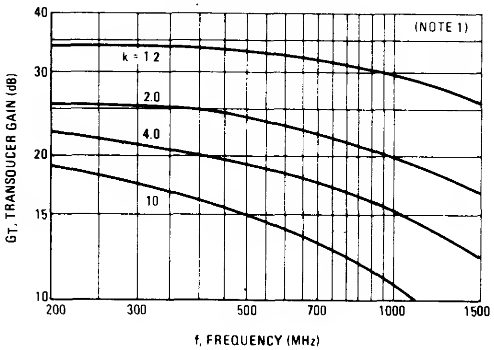


FIGURE 14 – LINVILL STABILITY FACTOR versus FREQUENCY

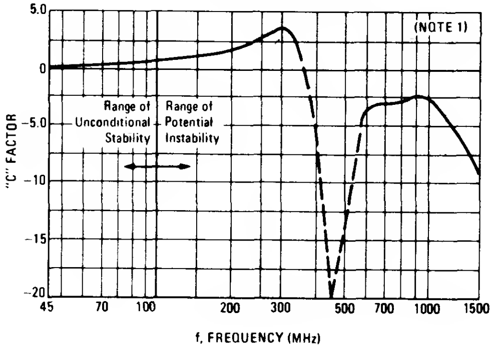


FIGURE 15 – LOAD ADMITTANCE versus FREQUENCY (REAL)

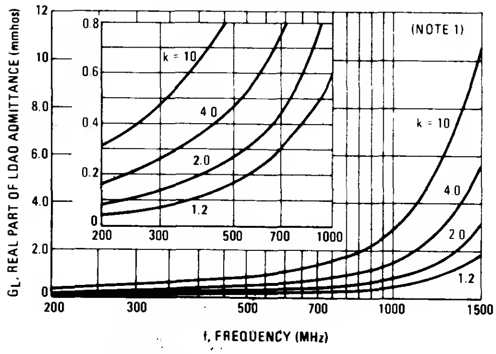


FIGURE 16 – LOAD ADMITTANCE versus FREQUENCY (IMAGINARY)

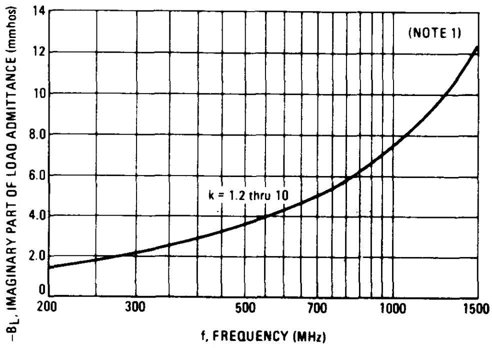


FIGURE 17 – SOURCE ADMITTANCE versus FREQUENCY (REAL)

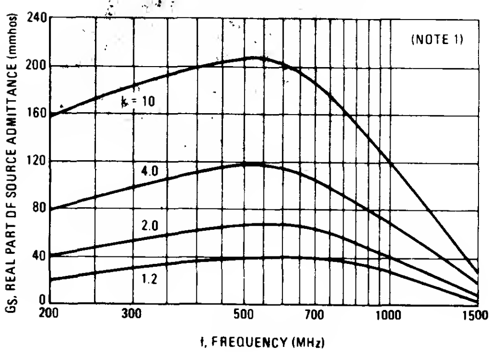


FIGURE 18 – SOURCE ADMITTANCE versus FREQUENCY (IMAGINARY)

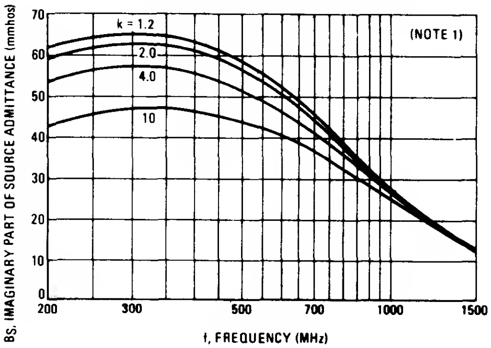


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FIGURE 19 – SMALL-SIGNAL CURRENT GAIN versus FREQUENCY

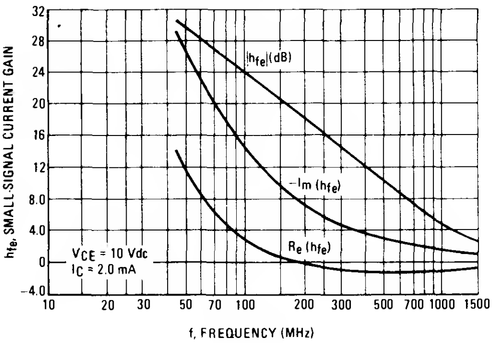


FIGURE 20 – POLAR h_{fe}

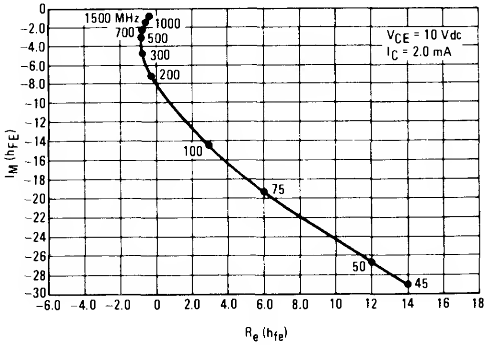


FIGURE 21 – f_T versus COLLECTOR CURRENT

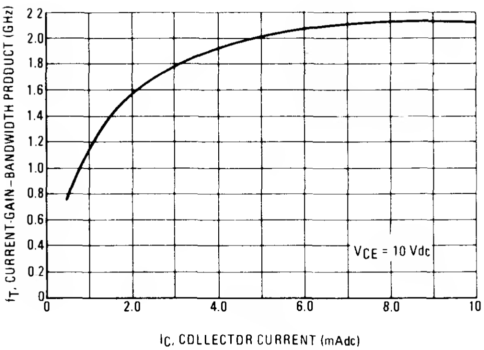


FIGURE 22 – DC CURRENT GAIN

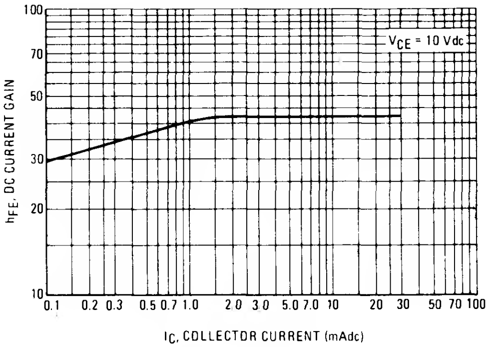


FIGURE 23 – CAPACITANCE

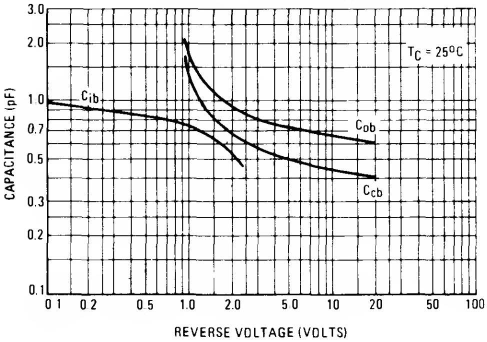
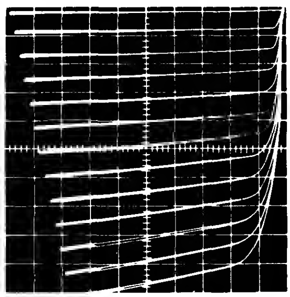


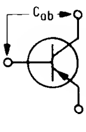
FIGURE 24 – COLLECTOR CHARACTERISTICS

VERTICAL SCALE
I_C = 1.0 mA/DIV

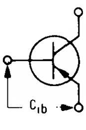
I_b = 0.02 mA/STEP



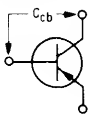
HORIZONTAL SCALE – V_{CE} = 1.0 V/DIV



Apply reverse bias between collector and base and measure capacitance between these terminals. Emitter is open



Apply reverse bias between emitter and base and measure capacitance between these terminals. Collector is open



Apply reverse bias between collector and base and measure capacitance between these terminals. Emitter is guarded.

Y PARAMETERS versus CURRENT
(f = 450 MHz)

COMMON BASE — V_{CB} = 10 Vdc ——— V_{CB} = 15 Vdc — — —

COMMON EMITTER — V_{CE} = 10 Vdc ——— V_{CE} = 15 Vdc — — —

FIGURE 25 – INPUT ADMITTANCE

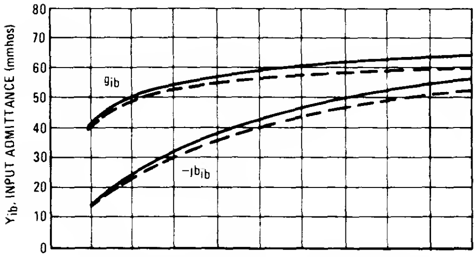


FIGURE 26 – INPUT ADMITTANCE

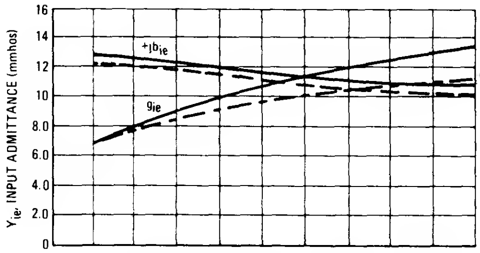


FIGURE 27 – FORWARD TRANSFER ADMITTANCE

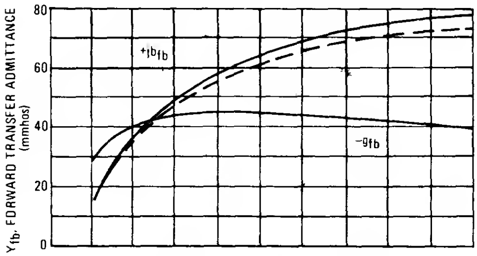


FIGURE 28 – FORWARD TRANSFER ADMITTANCE

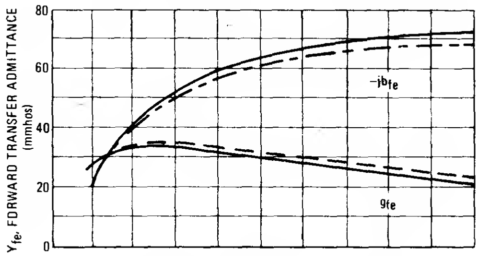


FIGURE 29 – OUTPUT ADMITTANCE

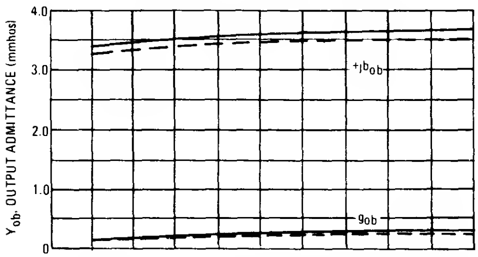


FIGURE 30 – OUTPUT ADMITTANCE

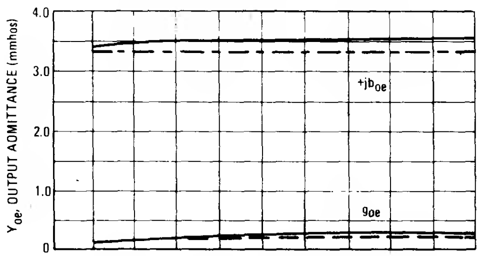


FIGURE 31 – REVERSE TRANSFER ADMITTANCE

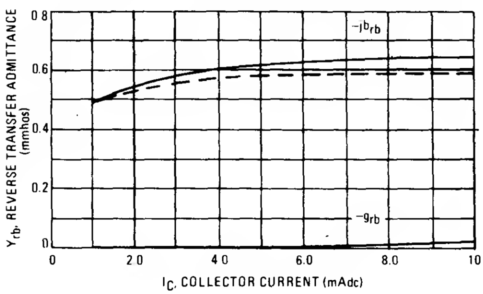
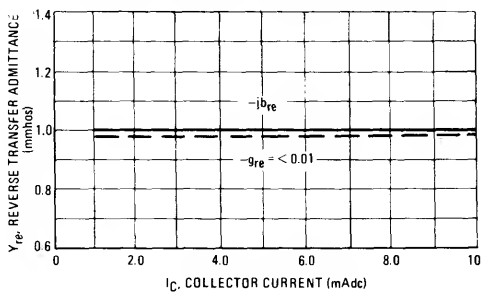


FIGURE 32 – REVERSE TRANSFER ADMITTANCE



COMMON BASE y PARAMETER VARIATIONS

(V_{CB} = 10 Vdc, I_C = 2.0 mAdc)

y PARAMETERS versus FREQUENCY

FIGURE 33 – y_{ib} INPUT ADMITTANCE

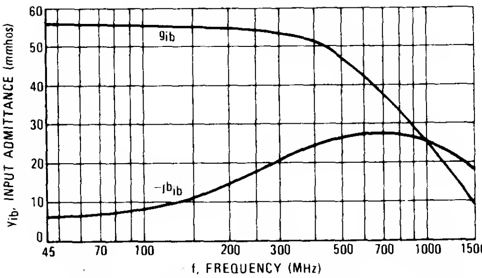


FIGURE 35 – y_{fb} FORWARD TRANSFER ADMITTANCE

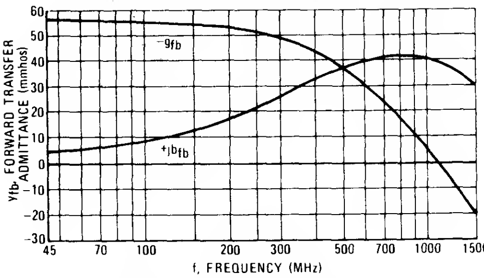


FIGURE 37 – y_{ob} OUTPUT ADMITTANCE

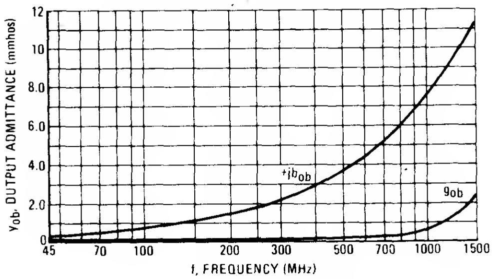
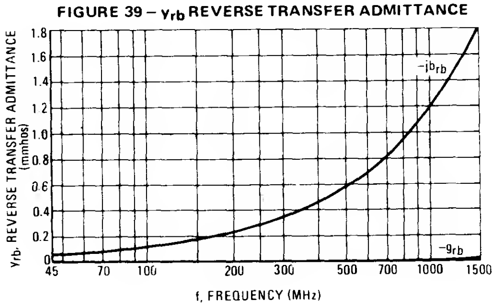


FIGURE 39 – y_{rb} REVERSE TRANSFER ADMITTANCE



POLAR y PARAMETERS versus FREQUENCY

FIGURE 34 – y_{ib} INPUT ADMITTANCE

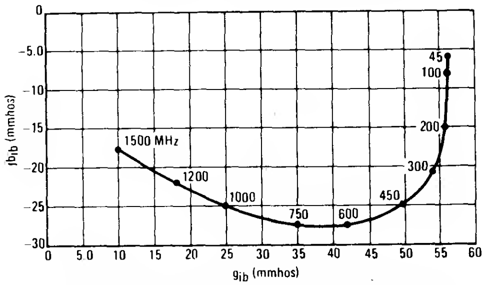


FIGURE 36 – y_{fb} FORWARD TRANSFER ADMITTANCE

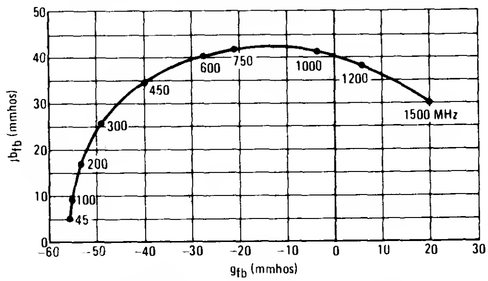


FIGURE 38 – y_{ob} OUTPUT ADMITTANCE

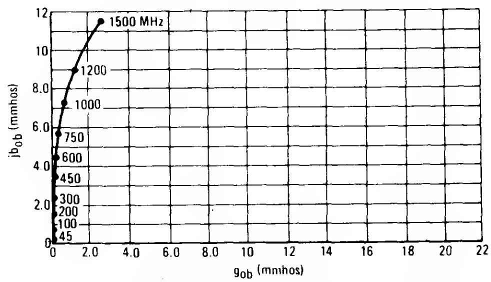
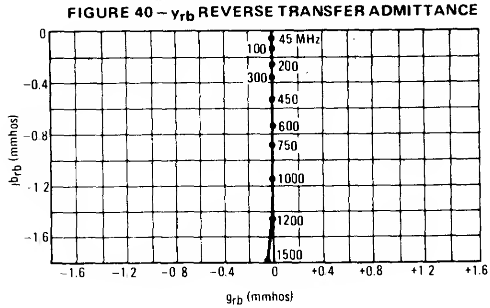


FIGURE 40 – y_{rb} REVERSE TRANSFER ADMITTANCE



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COMMON EMITTER y PARAMETER VARIATIONS

(V_{CE} = 10 Vdc, I_C = 2.0 mAdc)

y PARAMETERS versus FREQUENCY

FIGURE 41 – y_{ie} INPUT ADMITTANCE

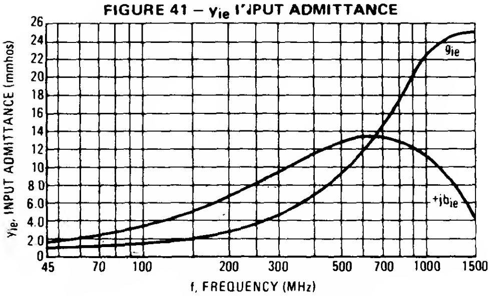


FIGURE 43 – y_{fe} FORWARD TRANSFER ADMITTANCE

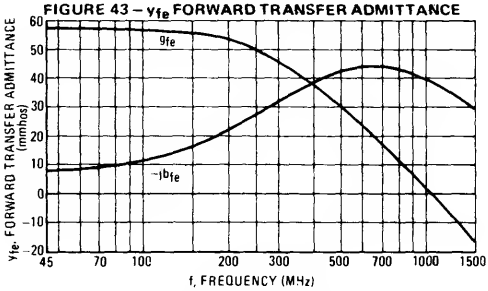


FIGURE 45 – y_{oe} OUTPUT ADMITTANCE

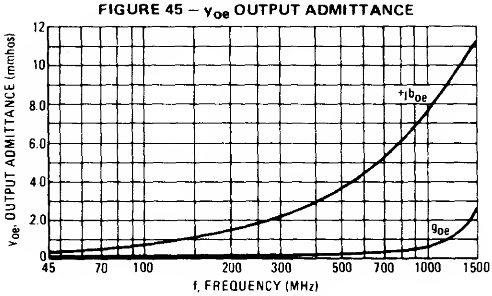
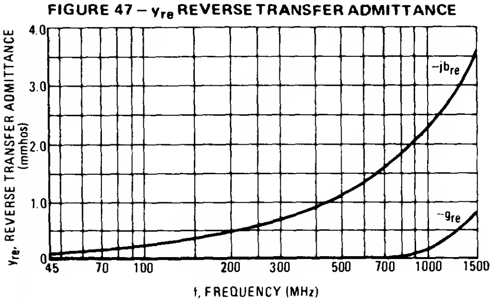


FIGURE 47 – y_{re} REVERSE TRANSFER ADMITTANCE



POLAR y PARAMETERS versus FREQUENCY

FIGURE 42 – y_{ie} INPUT ADMITTANCE

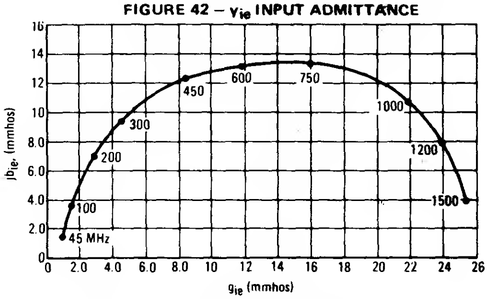


FIGURE 44 – y_{fe} FORWARD TRANSFER ADMITTANCE

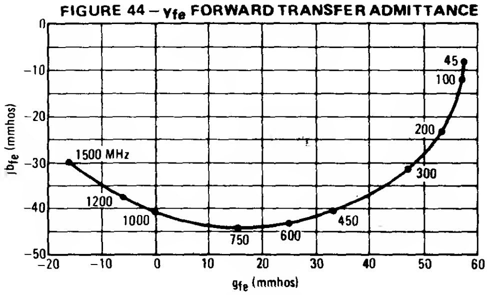


FIGURE 46 – y_{oe} OUTPUT ADMITTANCE

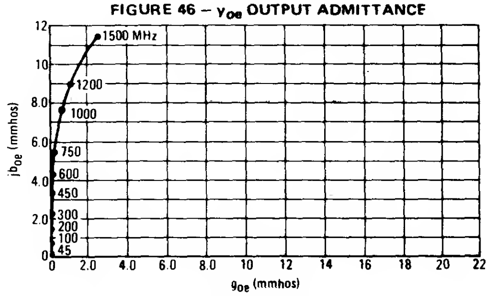
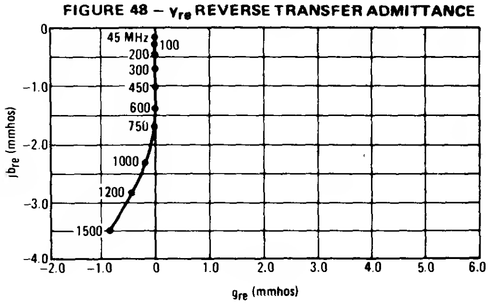


FIGURE 48 – y_{re} REVERSE TRANSFER ADMITTANCE



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