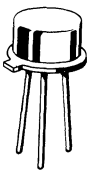
2N5859 (SILICON)

NPN SILICON ANNULAR SWITCHING TRANSISTOR

. . . designed for high-current, high-speed switching applications. Ideally suited for ferrite core and plated wire memory driver, hammer driver, or MOS translator applications.

- Excellent Current-Gain – Bandwidth Product –
  f_T = 250 MHz (Min) @ I_C = 50 mAdc
- Low Collector-Base Capacitance –
  C_{cb} = 7.0 pF (Max) @ V_{CB} = 10 Vdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.0 Adc
- Fast Switching Times @ I_C = 1.0 Adc
  t_{on} = 35 ns (Max)
  t_{off} = 60 ns (Max)

NPN SILICON SWITCHING TRANSISTOR



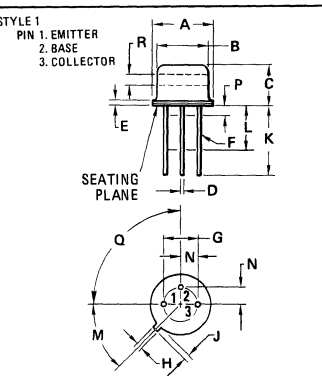
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.72	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	175	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	35	°C/W

*Indicates JEDEC Registered Data



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

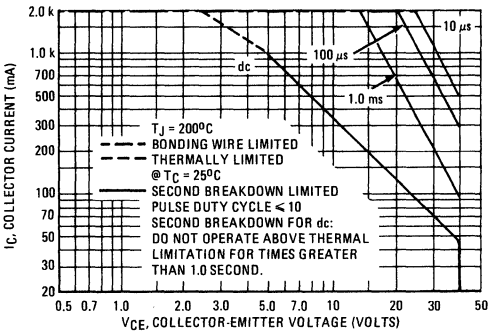
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	80	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current	I_{CEX}			μAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 2.0 Vdc)		–	0.2	
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_A = 75°C)		–	5.0	
Collector Cutoff Current	I_{CBO}			μAdc
(V_{CB} = 50 Vdc, I_E = 0)		–	0.25	
(V_{CB} = 50 Vdc, I_E = 0, T_A = 75°C)		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		30	120	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		15	100	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc, T_A = -55°C)		10	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)		–	0.4	
(I_C = 1.0 Adc, I_B = 100 mAdc)		–	0.7	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)		0.8	1.0	
(I_C = 1.0 Adc, I_B = 100 mAdc)		0.9	1.25	
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	250	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	7.0	pF
Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	60	pF
SWITCHING CHARACTERISTICS				
Turn-On Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, I_C = 1.0 Adc, I_{B1} = 100 mAdc) (Figures 8 and 10)	t_{on}	–	35	ns
Delay Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, I_C = 1.0 Adc, I_{B1} = 100 mAdc) (Figures 8 and 10)	t_d	–	6.0	ns
Rise Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, I_C = 1.0 Adc, I_{B1} = 100 mAdc) (Figures 8 and 10)	t_r	–	30	ns
Turn-Off Time (V_{CC} = 30 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (Figures 9 and 11)	t_{off}	–	60	ns
Storage Time (V_{CC} = 30 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (Figures 9 and 11)	t_s	–	35	ns
Fall Time (V_{CC} = 30 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (Figures 9 and 11)	t_f	–	35	ns

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL DC CHARACTERISTICS

FIGURE 2 – DC CURRENT GAIN

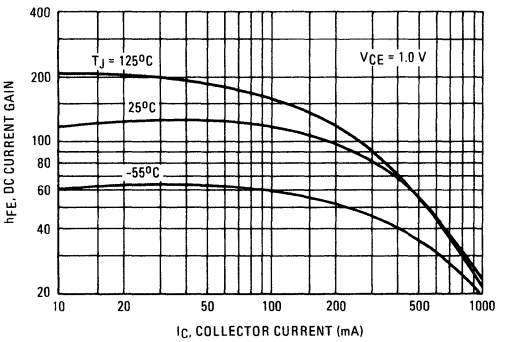


FIGURE 3 – "ON" VOLTAGES

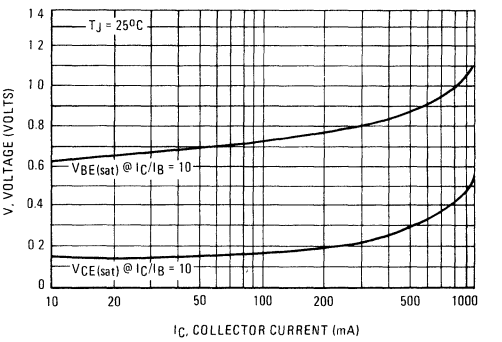


FIGURE 4 – COLLECTOR SATURATION REGION

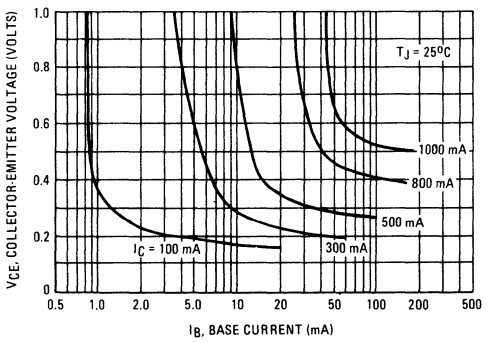
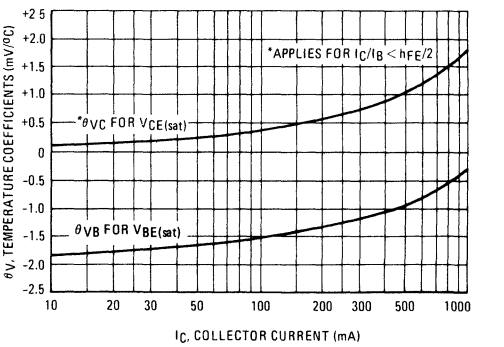


FIGURE 5 – TEMPERATURE COEFFICIENTS



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 6 – CURRENT-GAIN–BANDWIDTH PRODUCT

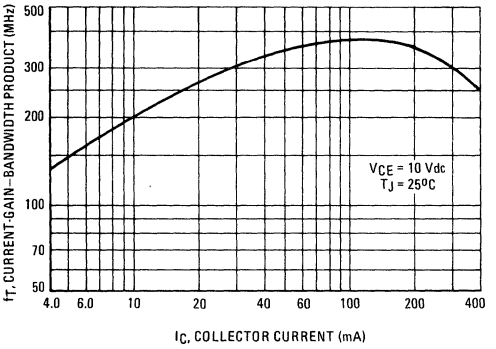


FIGURE 7 – CAPACITANCE

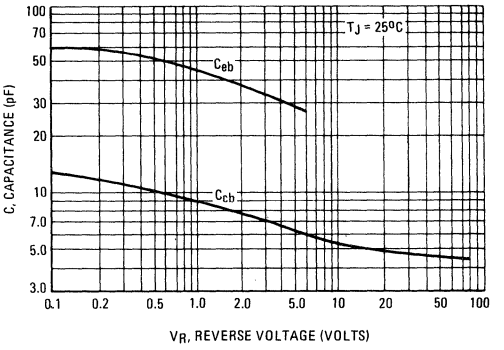


FIGURE 8 – TURN-ON TIME

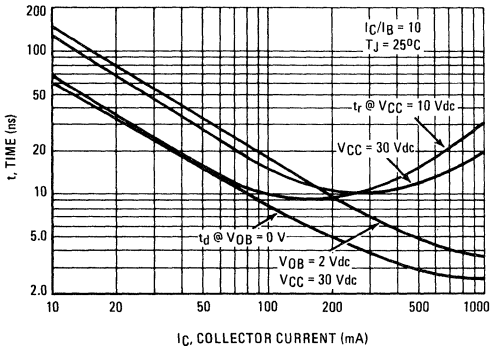


FIGURE 9 – TURN-OFF TIME

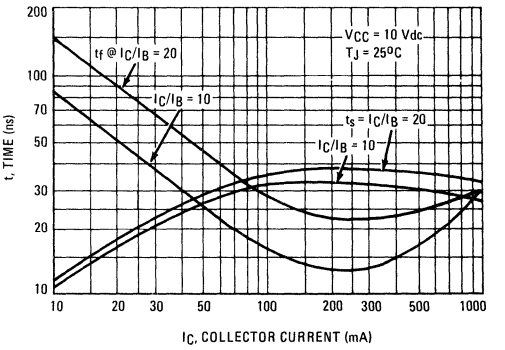


FIGURE 10 – TURN-ON TIME TEST CIRCUIT

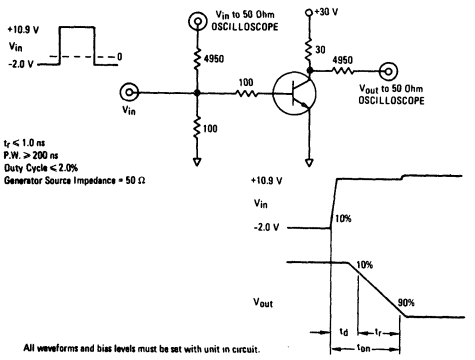


FIGURE 11 – TURN-OFF TIME TEST CIRCUIT