# 2N5861 (SILICON)

## NPN SILICON ANNULAR MEMORY DRIVER

. . . designed for medium-current, high-speed switching applications. Ideally suited for ferrite core memory driver circuits.

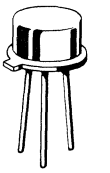
- Collector-Emitter Breakdown Voltage –
  $BV_{CEO}$ = 50 Vdc (Min) @ $I_C$ = 10 mAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ $I_C$ = 500 mAdc
- Low Collector-Base Capacitance –
  $C_{cb}$ = 7.0 pF (Max) @ $V_{CB}$ = 10 Vdc
- Fast Switching Times @ $I_C$ = 500 mAdc –
  $t_{on}$ = 25 ns (Max)
  $t_{off}$ = 60 ns (Max)

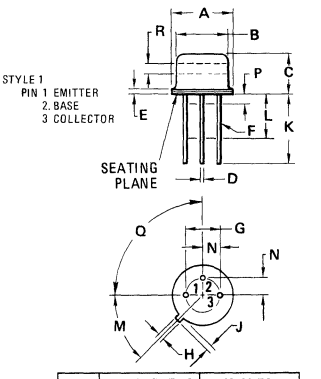
*MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | 50 | Vdc |
| Collector-Base Voltage | $V_{CB}$ | 100 | Vdc |
| Emitter-Base Voltage | $V_{EB}$ | 6.0 | Vdc |
| Collector Current – Continuous | $I_C$ | 2.0 | Adc |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 1.0<br>6.0 | Watts<br>mW/°C |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 5.0<br>28.6 | Watts<br>mW/°C |
| Operating and Storage Junction Temperature Range | $T_J$,$T_{stg}$ | -65 to +200 | °C |

*Indicates JEDEC Registered Data

## NPN SILICON MEMORY DRIVER TRANSISTOR






| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 8.89 | 9.40 | 0.350 | 0.370 |
| B | 8.00 | 8.51 | 0.315 | 0.335 |
| C | 6.10 | 6.60 | 0.240 | 0.260 |
| D | 0.406 | 0.533 | 0.016 | 0.021 |
| E | 0.229 | 3.18 | 0.009 | 0.125 |
| F | 0.406 | 0.483 | 0.016 | 0.019 |
| G | 4.83 | 5.33 | 0.190 | 0.210 |
| H | 0.711 | 0.864 | 0.028 | 0.034 |
| J | 0.737 | 1.02 | 0.029 | 0.040 |
| K | 12.70 | – | 0.500 | – |
| L | 6.35 | – | 0.250 | – |
| M | 45° NOM | | 45° NOM | |
| P | – | 1.27 | – | 0.050 |
| Q | 90° NOM | | 90° NOM | |
| R | 2.54 | – | 0.100 | – |

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

***ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Collector-Emitter Breakdown Voltage (1) ($I_C$ = 10 mAdc, $I_B$ = 0) | $BV_{CEO}$ | 50 | – | Vdc |
| Collector-Base Breakdown Voltage ($I_C$ = 100 μAdc, $I_E$ = 0) | $BV_{CBO}$ | 100 | – | Vdc |
| Emitter-Base Breakdown Voltage ($I_E$ = 10 μAdc, $I_C$ = 0) | $BV_{EBO}$ | 6.0 | – | Vdc |
| Collector Cutoff Current | $I_{CEV}$ | | | μAdc |
| ($V_{CE}$ = 50 Vdc, $V_{BE(off)}$ = 2.0 Vdc) | | – | 0.3 | |
| ($V_{CE}$ = 50 Vdc, $V_{BE(off)}$ = 2.0 Vdc, $T_A$ = 75°C) | | – | 10 | |
| Collector Cutoff Current | $I_{CBO}$ | | | μAdc |
| ($V_{CB}$ = 50 Vdc, $I_E$ = 0) | | – | 0.3 | |
| ($V_{CB}$ = 50 Vdc, $I_E$ = 0, $T_A$ = +75°C) | | – | 10 | |
| Emitter Cutoff Current ($V_{BE}$ = 5.0 Vdc, $I_C$ = 0) | $I_{EBO}$ | – | 0.1 | μAdc |
| **ON CHARACTERISTICS (1)** | | | | |
| DC Current Gain | $h_{FE}$ | | | – |
| ($I_C$ = 500 mAdc, $V_{CE}$ = 1.0 Vdc) | | 25 | 100 | |
| ($I_C$ = 500 mAdc, $V_{CE}$ = 1.0 Vdc, $T_A$ = -55°C) | | 10 | – | |
| Collector-Emitter Saturation Voltage ($I_C$ = 500 mAdc, $I_B$ = 50 mAdc) | $V_{CE(sat)}$ | – | 0.5 | Vdc |
| Base-Emitter Saturation Voltage ($I_C$ = 500 mAdc, $I_B$ = 50 mAdc) | $V_{BE(sat)}$ | 0.8 | 1.1 | Vdc |
| **DYNAMIC CHARACTERISTICS** | | | | |
| Current-Gain–Bandwidth Product ($I_C$ = 50 mAdc, $V_{CE}$ = 10 Vdc, f = 100 MHz) | $f_T$ | 200 | – | MHz |
| Collector-Base Capacitance ($V_{CB}$ = 10 Vdc, $I_E$ = 0, f = 100 kHz) | $C_{cb}$ | – | 7.0 | pF |
| Emitter-Base Capacitance ($V_{BE}$ = 0.5 Vdc, $I_C$ = 0, f = 100 kHz) | $C_{eb}$ | – | 60 | pF |
| **SWITCHING CHARACTERISTICS** | | | | |
| Turn-On Time | ($V_{CC}$ = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, $I_C$ = 500 mAdc, $I_{B1}$ = 50 mAdc) (Figure 5) | $t_{on}$ | – | 25 ns |
| Delay Time | | $t_d$ | – | 8.0 ns |
| Rise Time | | $t_r$ | – | 18 ns |
| Turn-Off Time | ($V_{CC}$ = 30 Vdc, $I_C$ = 500 mAdc, $I_{B1}$ = $I_{B2}$ = 50 mAdc) (Figure 6) | $t_{off}$ | – | 60 ns |
| Storage Time | | $t_s$ | – | 35 ns |
| Fall Time | | $t_f$ | – | 35 ns |

*Indicates JEDEC Registered Data.

**(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.**

## TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN–BANDWIDTH PRODUCT

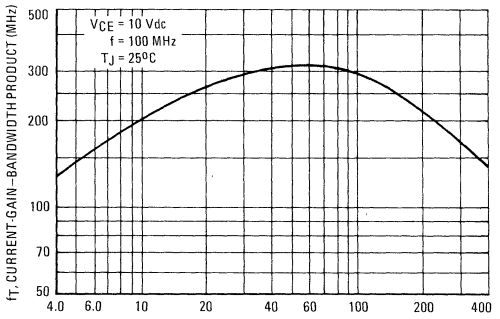
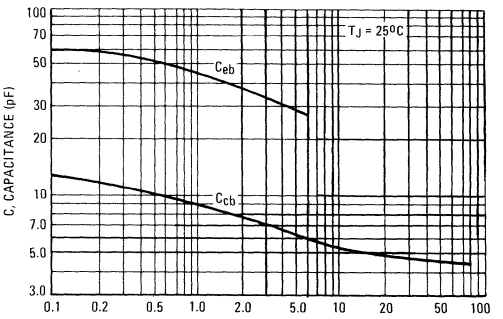



FIGURE 2 – CAPACITANCE



## TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 3 – TURN-ON TIME

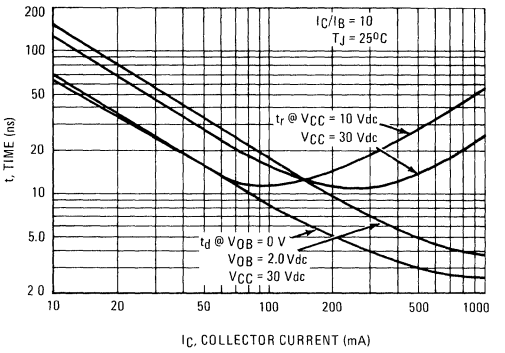



FIGURE 4 – TURN-OFF TIME

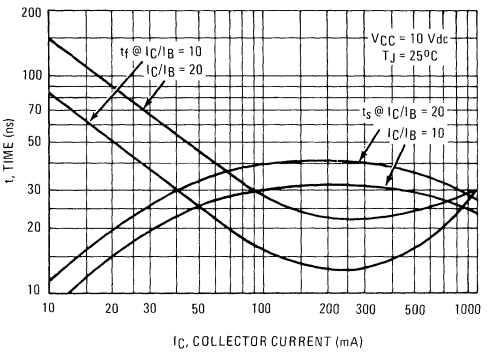
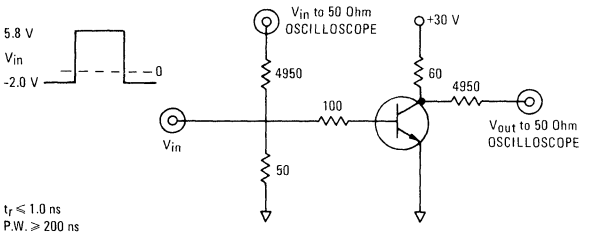
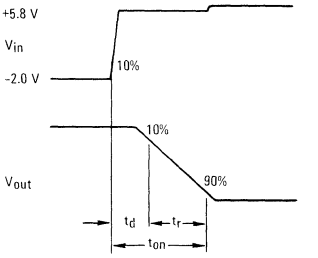



FIGURE 5 – TURN-ON TIME TEST CIRCUIT

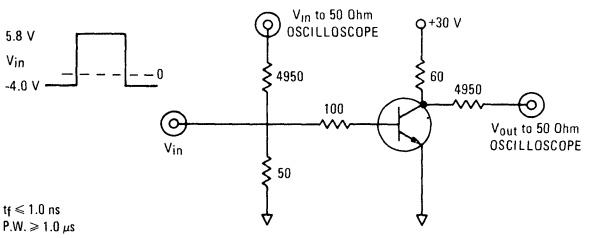



$t_r \leq 1.0$ ns
P.W. $\geq$ 200 ns
Duty Cycle $\leq$ 2.0%
Generator Source Impedance = 50 Ω
Pulse Generator: EH1421 Timing Unit and 1121 Pulse Driver
Oscilloscope: Tektronix 661 Sampling Scope

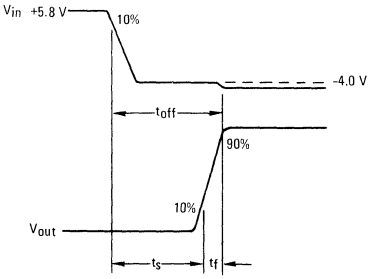



$V_{in}$ during $t_{on}$ interval must be +5.8 V.
All waveforms and bias levels must be set with unit in circuit.

FIGURE 6 – TURN-OFF TIME TEST CIRCUIT




$t_f \leq 1.0$ ns
P.W. $\geq 1.0$ μs
Duty Cycle $\leq$ 2.0%
Generator Source Impedance = 50 Ω
Pulse Generator: EH1421 Timing Unit and 1121 Pulse Driver
Oscilloscope: Tektronix 661 Sampling Scope




$V_{in}$ during $t_{off}$ interval must be -4.0 V.
All waveforms and bias levels must be set with unit in circuit.

**FIGURE 7 – DC CURRENT GAIN**

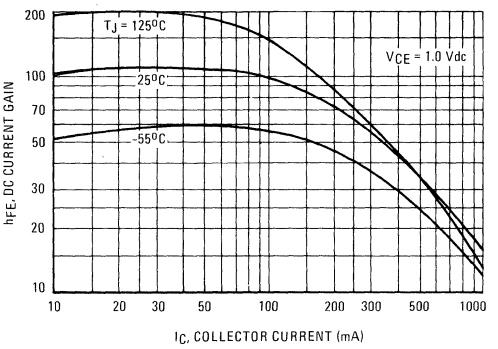



**FIGURE 8 – "ON" VOLTAGES**

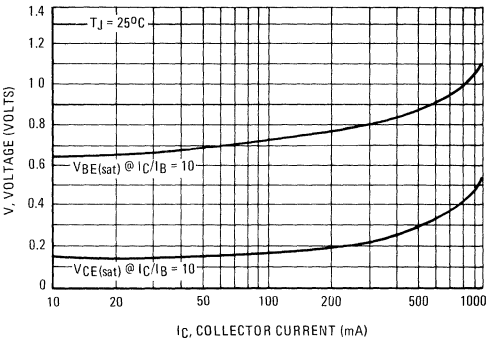
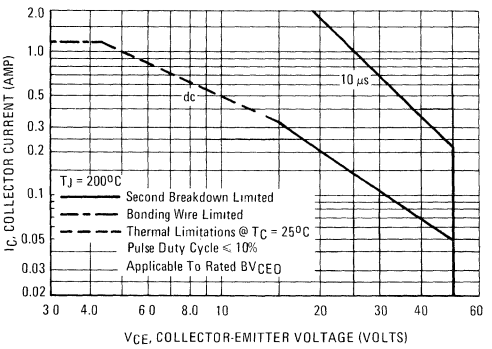



**FIGURE 9 – ACTIVE-REGION SAFE OPERATING AREA**




There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C$–$V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)}$ = 200°C; $T_C$ is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

**FIGURE 12 – TEMPERATURE COEFFICIENTS**